SM5309A

3-channel Video Buffer with Built-in wideband LPF

OVERVIEW

The SM5309A is a 3-channel video buffer with built-in 5th-order lowpass filters. The lowpass filter cutoff frequency range can adjust from 4MHz to 40MHz[*1] by 256 steps. The lowpass filter supports 480i to 1080i format, video signal equipment analog input/outputs. For video input systems, the device functions as a next-stage ADC system anti-aliasing filter. For video output systems, the filter reduces video DAC aliasing and external noise and can drive up to 300Ω load resistance. The cutoff frequency and signal input type can be controlled using an I²C-BUS[*2], and the I²C slave address can be set by ADS (3-state input) to allow up to three SM5309A on the same bus.

*1. When the resistor connected to ISET (R_{ISET}) is 1.8kΩ.
*2. I²C-BUS is a registered trademark of NXP B.V.

FEATURES

- Supply voltages
  - Analog: 4.75 to 5.25V
  - I²C-BUS interface: 3.0 to 5.5V
- Lowpass filter with adjustable cutoff frequency (256 steps)
  - Cutoff frequency range: 4MHz to 40MHz (R_{ISET} = 1.8kΩ)
- Filter bypass mode function for display specifications up to SXGA resolution
  - Passband: 80MHz (typ)
- Half fc mode switch function (CH-2, CH-3) suitable for component signals
- 2-system input multiplexer function (switchable using I²C-BUS or MUXSEL input)
- Video input pins can be independently set to sync-tip clamp/bias/direct inputs
- Up to 300Ω load resistance drive capability
- Output gain: 0dB
- Power-down function
  - ≤ 1mA current consumption when power-down
- I²C-BUS interface control
  - Slave address: 90h, 92h, or 94h (up to three devices can be used simultaneously, selected by ADS input)
  - Data transfer rate: Fast mode (up to 400kbit/s)
- Operating ambient temperature range: 0 to 70°C
- Package: 24-pin VSOP

APPLICATIONS

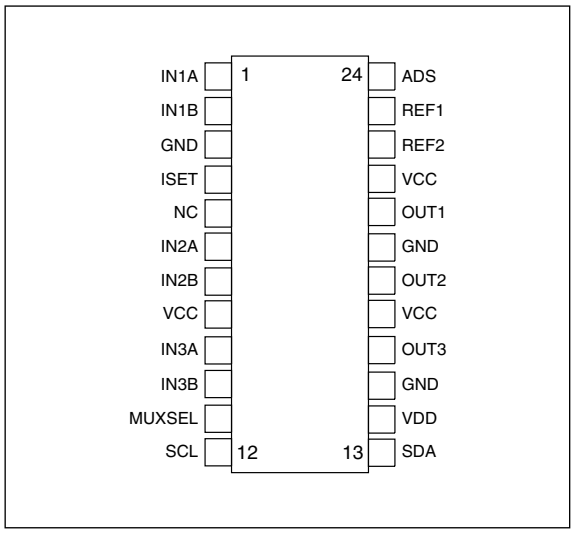
- HDTVs
- LCD TVs
- PDPs
- Projectors

ORDERING INFORMATION

Device	Package
SM5309AV	24-pin VSOP

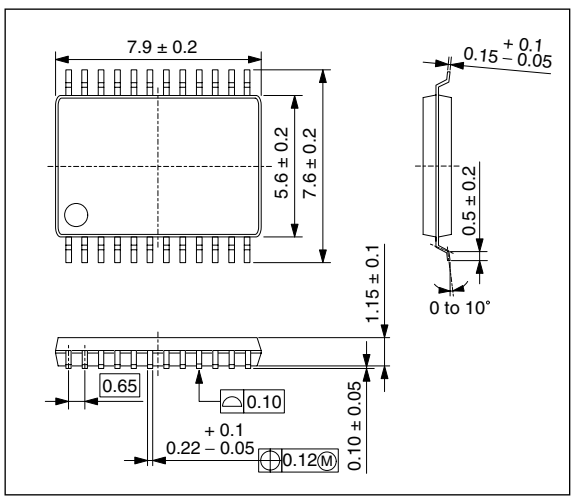
PINOUT

(Top view)

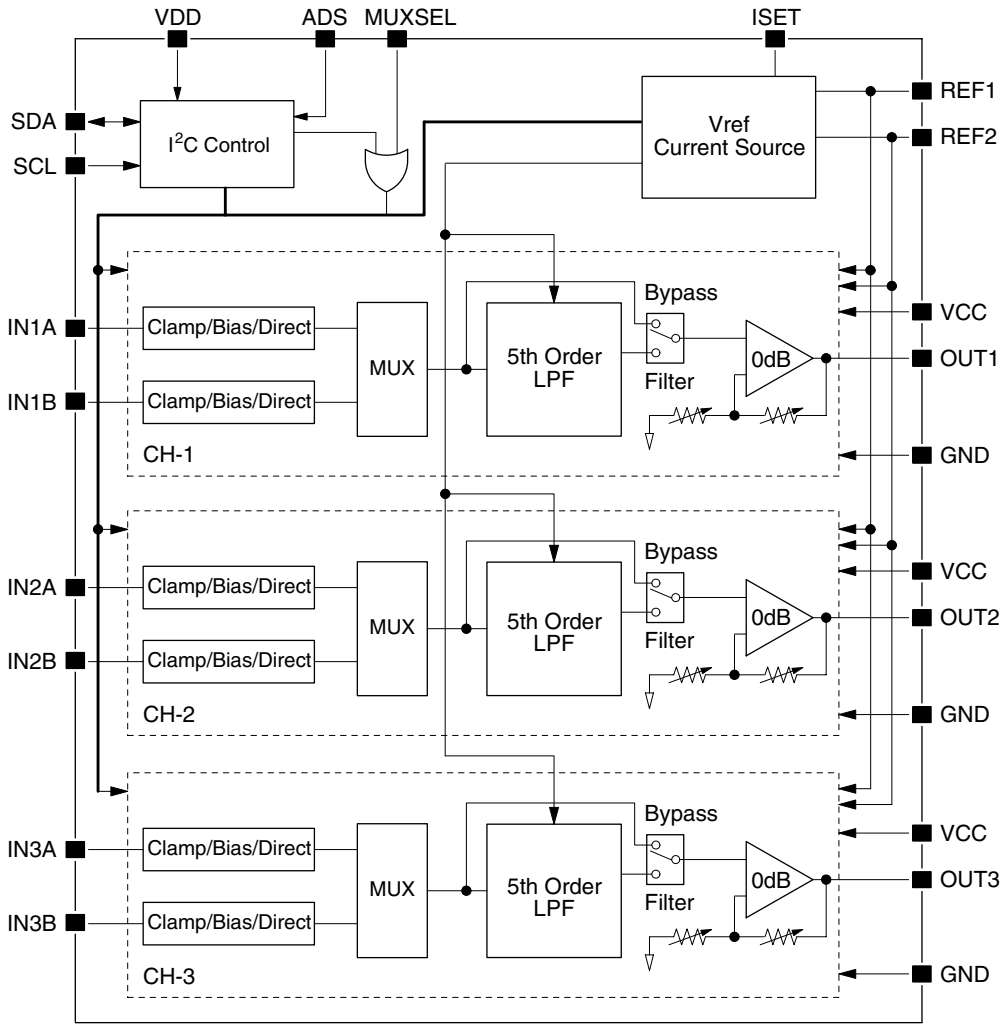


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



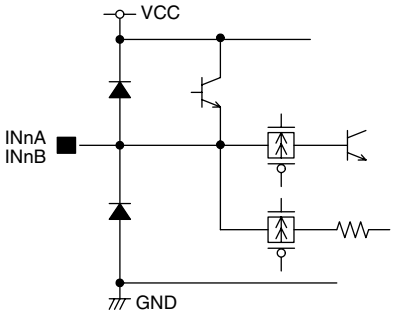
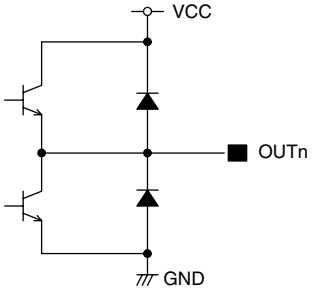
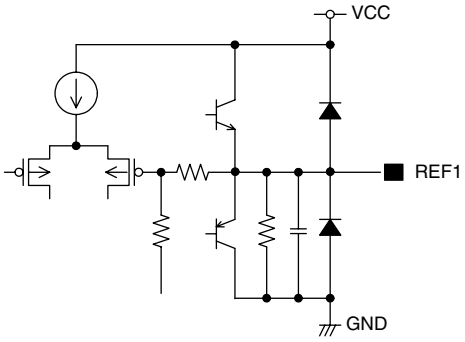
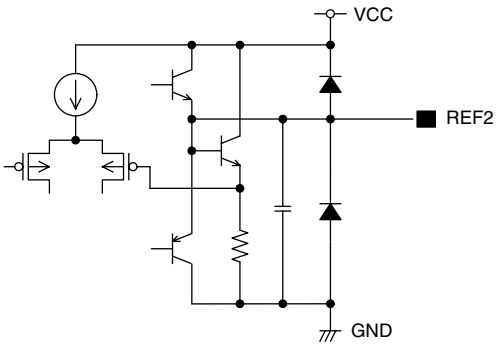
Note. The recommended value of the external resistor (R_{ISET}) connected to ISET is 1.8kΩ.

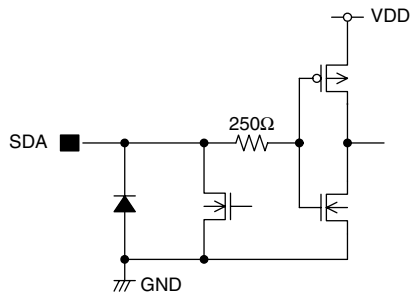
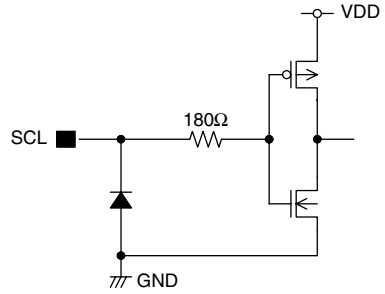
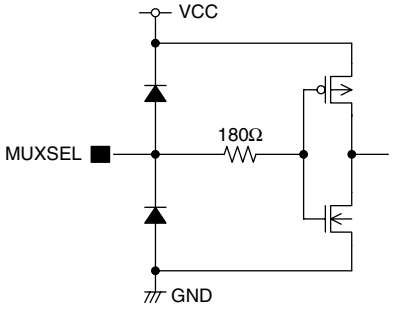
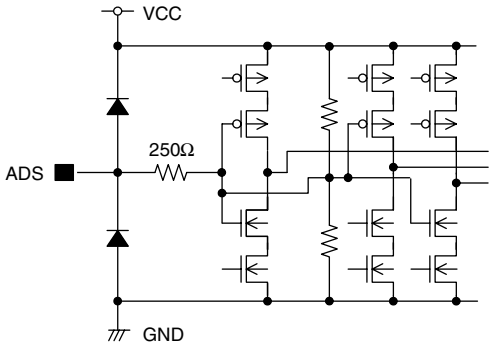
PIN DESCRIPTION

Number	Name	I/O*1	A/D*2	Description
1	IN1A	I	A	Video signal input (CH-1, input A)
2	IN1B	I	A	Video signal input (CH-1, input B)
3	GND	–	A	Ground
4	ISET	–	A	Internal current-setting resistor (R_{ISET}) connection (standard 1.8kΩ)
5	NC	–	–	No connection
6	IN2A	I	A	Video signal input (CH-2, input A)
7	IN2B	I	A	Video signal input (CH-2, input B)
8	VCC	–	A	Analog supply
9	IN3A	I	A	Video signal input (CH-3, input A)
10	IN3B	I	A	Video signal input (CH-3, input B)
11	MUXSEL	I	D	Input multiplexer switch control L (GND): INnA select H (VCC): INnB select
12	SCL	I	D	I^2C-BUS clock signal input
13	SDA	I/O	D	I^2C-BUS data signal input/output
14	VDD	–	D	I^2C-BUS interface supply
15	GND	–	A	Ground
16	OUT3	O	A	Video signal output (CH-3)
17	VCC	–	A	Analog supply
18	OUT2	O	A	Video signal output (CH-2)
19	GND	–	A	Ground
20	OUT1	O	A	Video signal output (CH-1)
21	VCC	–	A	Analog supply
22	REF2	O	A	Internal reference voltage 2
23	REF1	O	A	Internal reference voltage 1
24	ADS	I	D	I^2C-BUS slave address select (3-state input) L (GND): 90h H (VCC): 92h Open: 94h

*1. I: input, O: output
*2. A: analog, D: digital

PIN EQUIVALENT CIRCUITS

Number	Name	I/O*1	Equivalent circuit
1 2 6 7 9 10	IN1A IN1B IN2A IN2B IN3A IN3B	I	
20 18 16	OUT1 OUT2 OUT3	O	
23	REF1	O	
22	REF2	O	

Number	Name	I/O*1	Equivalent circuit
13	SDA	I/O	
12	SCL	I	
11	MUXSEL	I	
24	ADS	I	

*1. I: input, O: output

Note. Resistance values in the equivalent circuits indicate design values.

SPECIFICATIONS

Absolute Maximum Ratings

GND = 0V, VCC = VDD = V_{CC}

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	VCC, VDD	− 0.3 to 7.0	V
Input voltage	V_{IN}	ADS, SDA, SCL, INn (n = 1, 2, 3)	GND − 0.3 to V_{CC} + 0.3	V
Storage temperature range	T_{STG}		− 55 to + 125	°C
Power dissipation*1	P_D		1.1	W
Junction temperature*1	T_J		125	°C

*1. Ta = 80°C, when mounted on NPC's regulation substrate (110 × 65 × 1.6mm double layer glass-epoxy substrate with 160% wiring factor)

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage 1	V_{CC}	VCC	4.75 to 5.25	V
Supply voltage 2	V_{DD}	VDD	3.0 to 5.5	V
Operating ambient temperature	Ta		0 to 70	°C

Note. VCC should be applied simultaneously.

Electrical Characteristics

DC Characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 300Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

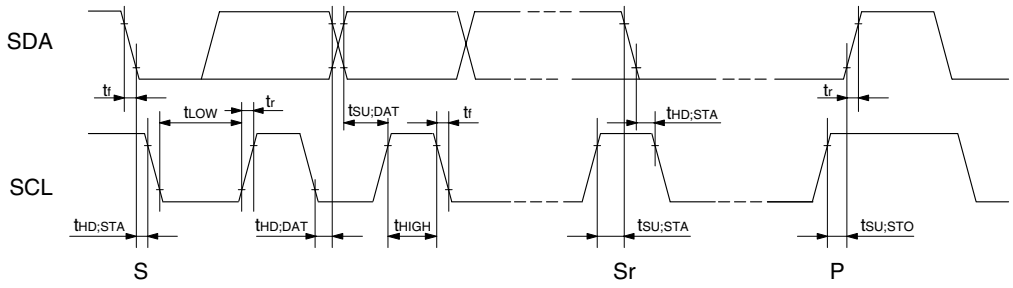
Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Current consumption 1*1	I_{CC1}	Filter mode, FCDATA = 0	–	65	90	mA	I
Current consumption 2*1	I_{CC2}	Filter mode, FCDATA = 255	–	80	115	mA	I
Current consumption 3*1	I_{CC3}	Filter bypass mode	–	50	75	mA	I
Current consumption 4*1	I_{CC4}	Power-down mode	–	–	1.0	mA	I
HIGH-level input voltage	V_{IH1}	SDA, SCL	0.7 V_{DD}	–	–	V	I
LOW-level Input voltage	V_{IL1}	SDA, SCL	–	–	0.3 V_{DD}	V	I
ADS, MUXSEL HIGH-level input voltage	V_{IH2}	ADS, MUXSEL	0.8 V_{CC}	–	–	V	I
ADS, MUXSEL LOW-level input voltage	V_{IL2}	ADS, MUXSEL	–	–	0.2 V_{CC}	V	I
ADS open-circuit input voltage	V_{OPEN}	ADS	V_{CC}/2 − 0.2	–	V_{CC}/2 + 0.2	V	I
LOW-level input leakage current	I_{LL}	SDA, SCL, V_{IN} = 0V	–	–	1.0	µA	I
HIGH-level input leakage current	I_{LH}	SDA, SCL, V_{IN} = V_{DD}	–	–	1.0	µA	I
SDA output voltage	V_{OL}	SDA = LOW output, Sink current = 3mA	0	–	0.4	V	I

*1. Total of current consumption of VCC and VDD, when no input signals.

AC Characteristics (I^2C-BUS)

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
SCL clock frequency	f_{SCL}		0	–	400	kHz	II
SCL hold time (start condition)	$t_{HD;STA}$		0.6	–	–	µs	II
SCL clock LOW-level pulsewidth	t_{LOW}		1.3	–	–	µs	II
SCL clock HIGH-level pulsewidth	t_{HIGH}		0.6	–	–	µs	II
SCL setup time (start condition)	$t_{SU;STA}$		0.6	–	–	µs	II
SDA data hold time	$t_{HD;DAT}$		0	–	0.9	µs	II
SDA data setup time	$t_{SU;DAT}$		100	–	–	ns	II
SDA, SCL rise time	t_r		–	–	300	ns	II
SDA, SCL fall time	t_f		–	–	300	ns	II
SCL setup time (stop condition)	$t_{SU;STO}$		0.6	–	–	µs	II
SDA, SCL input capacitance	C_i		–	–	10	pF	II



Note. S, Sr: start condition, P: stop condition

Analog Characteristics

Analog input characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 300Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted. Internal mode settings are shown in table 1 in "Mode Condition Settings".

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Clamp voltage	V_{CLMP}	Clamp input, no signal input	1.6	1.8	2.0	V	I
Bias voltage	V_{BIAS}	Bias input, no signal input	2.1	2.3	2.5	V	I
Input resistance	R_{BIAS}	Bias input	–	20	–	kΩ	II
Filter mode input voltage	V_{AI1}	Mode: b (bias), THD < 1.0%	–	–	1.4	Vp-p	I
	V_{AI2}	Mode: c (clamp), THD < 1.0%	–	–	1.4	Vp-p	I
Bypass mode input voltage	V_{AI3}	Mode: f (bias), THD < 1.0%	–	–	1.4	Vp-p	I
	V_{AI4}	Mode: g (clamp), THD < 1.0%	–	–	1.4	Vp-p	I
Direct mode input DC voltage range	V_{IDC}	Direct mode, THD < 1.5%, V_{IN} < 1.4Vp-p	1.5	–	3.2	V	I

Note. This item represents values of maximum input signal amplitude in which the output distortion rate shown in the condition column is filled. When the signal amplitude that exceeds this specification value is input, the output distortion rate is deteriorated. When using this device, the input signal level should be set not to exceed the standard value of the signal amplitude.

Filter mode and bypass mode frequency characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 300Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Cutoff frequency	F_{C1}	FCDATA = 0	–	4.00	–	MHz	II
	F_{C2}	FCDATA = 10	4.96	5.64	6.32	MHz	I
	F_{C3}	FCDATA = 227	28.95	32.90	36.85	MHz	I
	F_{C4}	FCDATA = 255	–	40.00	–	MHz	II
Half fc mode cutoff frequency ratio	R_{half1}	Half fc mode, FCDATA = 10	42	47	52	%	I
	R_{half2}	Half fc mode, FCDATA = 227	47.5	52.5	57.5	%	I
4fc attenuation	G_{SB}	fin ≥ 4fc, attenuation from fin = 100kHz	–	50	–	dB	II
Filter bypass mode passband	F_{BP}	V_{IN} = 1.0Vp-p, Gain = – 1dB	74.25	80	–	MHz	II

Analog output characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 300Ω, CH-1 set to clamp input, CH-2 and CH-3 set to bias input, FCDATA = 227, unless otherwise noted. Internal mode settings are shown in table 1 in "Mode Condition Settings".

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
Filter mode output gain	A_{VF}		– 0.5	0	0.5	dB	I
Filter bypass mode output gain	A_{VB}		– 0.5	0	0.5	dB	I
Filter bypass mode gain error	dA_{VBP}	Gain error between filter mode and bypass mode	–	± 0.2	–	dB	I
Channel to channel gain error	dA_{VCH}		–	–	± 0.2	dB	I
Maximum output voltage	V_{out}	Mode: b, c, THD < 1.0%	–	1.4	–	Vp-p	I
Output distortion	T_{HDB}	Mode: b, fin = 100kHz, V_{IN} = 1.4Vp-p	–	0.2	1.0	%	I
	T_{HDC}	Mode: c, fin = 100kHz, V_{IN} = 1.4Vp-p	–	0.2	1.0	%	I
Channel to channel crosstalk	X_{TLK1}	1.0Vp-p input, fin = 1MHz, between 2 channels	–	– 80	–	dB	II
MUX input to input crosstalk	X_{TLK2}	1.0Vp-p input, fin = 1MHz, between INnA and INnB	–	– 70	–	dB	II
Drive load resistance	R_L	1 load = 300Ω	–	–	1	load	I
I^2C response time	T_{IC}	Response time from ACK bit output when changing settings using I^2C-BUS	–	–	1	µs	II

Reference voltage characteristics

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	Test level
			min	typ	max		
REF output voltage	V_{R1}	REF1	–	3.35	–	V	II
	V_{R2}	REF2	–	2.45	–	V	II

Test level

The definition of “Test Level” shown in the electrical characteristic table is as follows.

I : 100% of products tested at Ta = + 25°C.

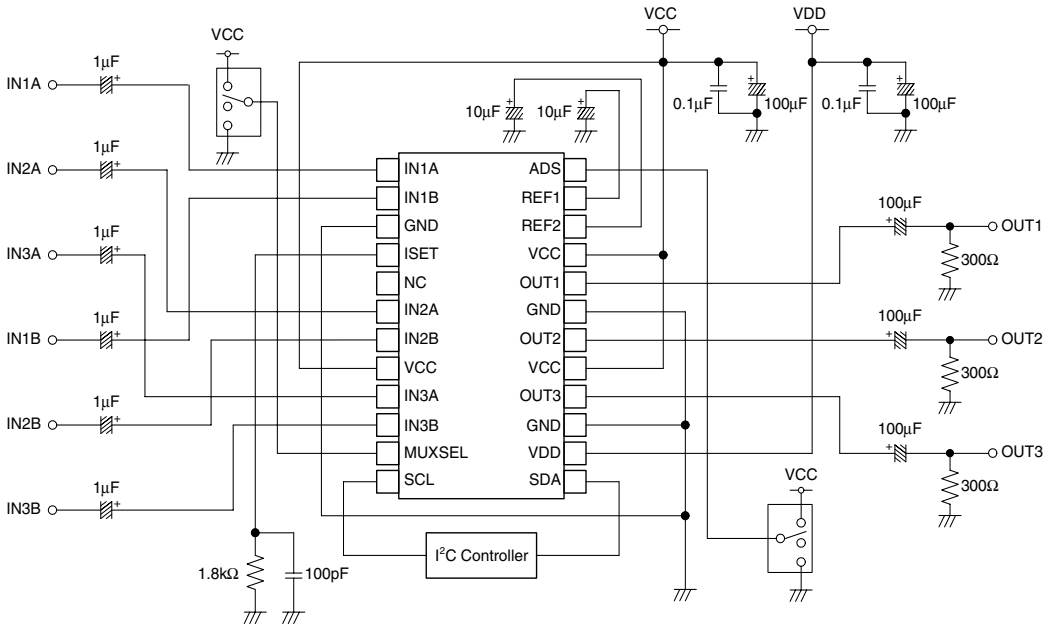
II : Guaranteed as result of design and characteristics evaluation.

Mode Condition Settings

Table 1. Mode settings

Mode setting	Input type			fc mode	Filter/Bypass mode
	CH-1	CH-2	CH-3		
a	Clamp	Bias	Bias	Standard	Filter
b	Bias				
c	Clamp				
d	Bias			Half	
e	Clamp				
f	Bias			–	Bypass
g	Clamp				
h	Direct			Standard	Filter
i				Half	
j				–	Bypass

Evaluation Circuit Diagram



FUNCTIONAL DESCRIPTION

I²C-BUS Control

The SM5309A uses an I²C BUS interface to set the following functions.

1) Cutoff frequency
2) Input multiplexer selection
3) fc mode switching (1/2 cutoff frequency switching)
4) Filter mode/filter bypass mode switching
5) Input type switching (sync-tip clamp, bias, direct)
6) Power-down function

The transfer rate of I²C-BUS corresponds to the fast-mode (up to 400kbit/s). Note that the SM5309A does not support a read function (IC is write only).

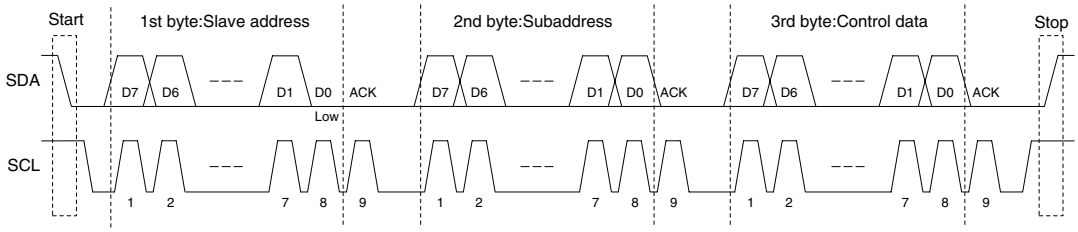
Basic cycle

I²C-BUS start/stop condition

The basic access cycle comprises the following elements.

1) Start condition
2) 1st byte: Slave address
3) 2nd byte: Subaddress
4) 3rd byte: Control data
5) Stop condition

If the input data does not match the slave address or the subaddress is incorrect, the corresponding ACK (acknowledge) bit is not output LOW. However, the ACK bit is output after 3rd byte irrespective of the byte data. Also note that the IC does not support a subaddress auto-increment function, hence each subaddress access requires all the basic cycle steps 1 to 5.



1st byte: slave address

The ADS pin can set one of three slave addresses. Note that D0 must be “0 (Write)”. The input circuit of ADS pin is placed in analog supply (VCC, GND) area.

ADS	1st byte: slave address								
	HEX	D7	D6	D5	D4	D3	D2	D1	D0
L: GND	90h	1	0	0	1	0	0	0	0 (W)
H: VCC	92h	1	0	0	1	0	0	1	0 (W)
Open	94h	1	0	0	1	0	1	0	0 (W)

2nd byte: subaddress

The 2nd byte sets the subaddress, selecting one of three registers.

Register name	2nd byte: subaddress								
	HEX	D7	D6	D5	D4	D3	D2	D1	D0
FCSET	01h	0	0	0	0	0	0	0	1
CONDITION1	02h	0	0	0	0	0	0	1	0
CONDITION2	03h	0	0	0	0	0	0	1	1

3rd byte: control data

The 3rd byte control data sets the register flags corresponding to the subaddress selected by 2nd byte. The flags assigned are shown in the following table.

Register name	3rd byte: control data							
	D7	D6	D5	D4	D3	D2	D1	D0
FCSET	FCM	FC6	FC5	FC4	FC3	FC2	FC1	FC0
CONDITION1	CB5	CB4	CB3	CB2	CB1	CB0	–	–
CONDITION2	PD	MUX	HALF	BYPASS	–	–	–	–

Flag settings

(1) Cutoff frequency

Register name: FCSET

Flag names: FCM, FC [6:0]

The FCSET register setting sets the cutoff frequency using one of two tuning adjustment functions, thus a total of 256 steps are possible.

FCDATA	FCSET	Flag name								Cutoff frequency [MHz]	Default
		FCM	FC6	FC5	FC4	FC3	FC2	FC1	FC0		
0	00h	0	0	0	0	0	0	0	0	4.00	○
1	01h	0	0	0	0	0	0	0	1	4.18	
2	02h	0	0	0	0	0	0	1	0	4.35	
:											
125	7Dh	0	1	1	1	1	1	0	1	21.66	
126	7Eh	0	1	1	1	1	1	1	0	21.79	
127	7Fh	0	1	1	1	1	1	1	1	21.92	
128	80h	1	0	0	0	0	0	0	0	7.51	
129	81h	1	0	0	0	0	0	0	1	7.82	
130	82h	1	0	0	0	0	0	1	0	8.11	
:											
253	FDh	1	1	1	1	1	1	0	1	39.46	
254	FEh	1	1	1	1	1	1	1	0	39.72	
255	FFh	1	1	1	1	1	1	1	1	40.00	

(2) Input type switching (sync-tip clamp, bias, direct)

Register name: CONDITION1

Flag names: CB [5:4], CB [3:2], CB [1:0]

These flags set the input type of CH-1, CH-2, and CH-3 to one of three types: sync-tip clamp input, bias input, or direct input.

Channel	Flag name		Input type	Default
CH-1 CH-2 CH-3	CB5 CB3 CB1	CB4 CB2 CB0		
	L	L	Sync-tip clamp input	○
	L	H	Bias input	
	H	Don't care	Direct input*1	

*1. An input coupling capacitor should not be connected when direct input is selected.

(3) Power-down mode select

Register name: CONDITION2

Flag name: PD

This flag selects standard/power-down for the analog block.

Flag name	Mode	Default
PD		
L	Standard (normal operation)	○
H	Power-down (no operation)	

(4) Input multiplexer selection

Register name: CONDITION2

Flag name: MUX

This flag selects the A or B input for all three channels (IN1×, IN2×, IN3×). Note that this flag is significant only when the MUXSEL input is LOW. See “Input Multiplexer Switching (MUXSEL)”.

Flag name	Input selection*1	Default
MUX		
L	INnA	○
H	INnB	

*1. n = 1, 2, 3

(5) fc mode switching (1/2 cutoff frequency switching)

Register name: CONDITION2

Flag name: HALF

This flag switches the cutoff frequency of CH-2 and CH-3 to divide the value set by the FCSET register into halves. Note that the CH-1 cutoff frequency cannot be switched to 1/2. This mode is suitable for systems where the sampling frequency varies due to Y, Cr, and Cb requirements, such as component signals.

Flag name	fc mode	Default
HALF		
L	Standard fc mode (CH-1, CH-2, CH-3 cutoff frequency is identical)	○
H	Half fc mode (CH-2, CH-3 cutoff frequency is 1/2 that of CH-1)	

(6) Filter bypass mode

Register name: CONDITION2

Flag name: BYPASS

This flag allows the internal lowpass filter in SM5309A to be bypassed. Even in filter bypass mode, the input type and multiplexer function can all be set just as in filter mode. However, the cutoff frequency and fc mode settings have no effect on the outputs.

Flag name	Filter	Default
BYPASS		
L	Filter mode (signals pass through lowpass filter)	○
H	Filter bypass mode (signals bypass lowpass filter)	

Lowpass Filter

The SM5309A has built-in 5th-order lowpass filters with variable cutoff frequency. The cutoff frequency range is set by the resistor (R_{ISET}) connected between ISET and GND, and the cutoff frequency setting is determined by FCDATA data. The cutoff frequency vs. FCDATA values are listed in table 2, and shown graphically in figure 1.

Table 2. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]	FCDATA	FCSET (hex)	Cutoff freq. [MHz]
0	00	4.00	64	40	13.61	128	80	7.51	192	C0	24.61
1	01	4.18	65	41	13.75	129	81	7.82	193	C1	24.86
2	02	4.35	66	42	13.89	130	82	8.11	194	C2	25.11
3	03	4.51	67	43	14.03	131	83	8.41	195	C3	25.35
4	04	4.67	68	44	14.17	132	84	8.69	196	C4	25.60
5	05	4.84	69	45	14.31	133	85	8.99	197	C5	25.85
6	06	5.00	70	46	14.44	134	86	9.28	198	C6	26.09
7	07	5.16	71	47	14.58	135	87	9.57	199	C7	26.34
8	08	5.32	72	48	14.72	136	88	9.85	200	C8	26.58
9	09	5.48	73	49	14.85	137	89	10.14	201	C9	26.82
10	0A	5.64	74	4A	14.99	138	8A	10.43	202	CA	27.07
11	0B	5.80	75	4B	15.12	139	8B	10.72	203	CB	27.32
12	0C	5.96	76	4C	15.26	140	8C	11.00	204	CC	27.56
13	0D	6.12	77	4D	15.40	141	8D	11.29	205	CD	27.80
14	0E	6.28	78	4E	15.53	142	8E	11.57	206	CE	28.04
15	0F	6.44	79	4F	15.67	143	8F	11.85	207	CF	28.28
16	10	6.58	80	50	15.80	144	90	12.11	208	D0	28.52
17	11	6.74	81	51	15.94	145	91	12.39	209	D1	28.76
18	12	6.89	82	52	16.07	146	92	12.67	210	D2	28.99
19	13	7.05	83	53	16.20	147	93	12.95	211	D3	29.24
20	14	7.20	84	54	16.34	148	94	13.22	212	D4	29.48
21	15	7.36	85	55	16.48	149	95	13.50	213	D5	29.72
22	16	7.51	86	56	16.61	150	96	13.78	214	D6	29.96
23	17	7.67	87	57	16.74	151	97	14.05	215	D7	30.21
24	18	7.82	88	58	16.88	152	98	14.32	216	D8	30.44
25	19	7.97	89	59	17.01	153	99	14.60	217	D9	30.66
26	1A	8.12	90	5A	17.14	154	9A	14.87	218	DA	30.89
27	1B	8.28	91	5B	17.28	155	9B	15.14	219	DB	31.12
28	1C	8.43	92	5C	17.42	156	9C	15.41	220	DC	31.36
29	1D	8.58	93	5D	17.55	157	9D	15.69	221	DD	31.59
30	1E	8.73	94	5E	17.68	158	9E	15.95	222	DE	31.81
31	1F	8.89	95	5F	17.81	159	9F	16.22	223	DF	32.04
32	20	9.01	96	60	17.93	160	A0	16.44	224	E0	32.23
33	21	9.16	97	61	18.06	161	A1	16.71	225	E1	32.45
34	22	9.31	98	62	18.19	162	A2	16.97	226	E2	32.68
35	23	9.46	99	63	18.31	163	A3	17.24	227	E3	32.90
36	24	9.61	100	64	18.44	164	A4	17.51	228	E4	33.17
37	25	9.76	101	65	18.58	165	A5	17.77	229	E5	33.42
38	26	9.90	102	66	18.71	166	A6	18.03	230	E6	33.68
39	27	10.05	103	67	18.84	167	A7	18.30	231	E7	33.93
40	28	10.20	104	68	18.97	168	A8	18.56	232	E8	34.19
41	29	10.35	105	69	19.10	169	A9	18.82	233	E9	34.44
42	2A	10.49	106	6A	19.23	170	AA	19.08	234	EA	34.69
43	2B	10.64	107	6B	19.36	171	AB	19.34	235	EB	34.94
44	2C	10.79	108	6C	19.49	172	AC	19.60	236	EC	35.20
45	2D	10.94	109	6D	19.62	173	AD	19.86	237	ED	35.44
46	2E	11.08	110	6E	19.75	174	AE	20.12	238	EE	35.70
47	2F	11.22	111	6F	19.88	175	AF	20.38	239	EF	35.96
48	30	11.36	112	70	20.01	176	B0	20.62	240	F0	36.20
49	31	11.51	113	71	20.13	177	B1	20.88	241	F1	36.45
50	32	11.65	114	72	20.26	178	B2	21.13	242	F2	36.70
51	33	11.80	115	73	20.39	179	B3	21.40	243	F3	36.96
52	34	11.94	116	74	20.52	180	B4	21.65	244	F4	37.20
53	35	12.08	117	75	20.64	181	B5	21.90	245	F5	37.45
54	36	12.23	118	76	20.77	182	B6	22.16	246	F6	37.70
55	37	12.37	119	77	20.90	183	B7	22.41	247	F7	37.96
56	38	12.51	120	78	21.03	184	B8	22.66	248	F8	38.20
57	39	12.65	121	79	21.15	185	B9	22.92	249	F9	38.44
58	3A	12.80	122	7A	21.28	186	BA	23.17	250	FA	38.70
59	3B	12.94	123	7B	21.41	187	BB	23.42	251	FB	38.95
60	3C	13.08	124	7C	21.54	188	BC	23.67	252	FC	39.21
61	3D	13.22	125	7D	21.66	189	BD	23.93	253	FD	39.46
62	3E	13.36	126	7E	21.79	190	BE	24.18	254	FE	39.72
63	3F	13.51	127	7F	21.92	191	BF	24.43	255	FF	40.00

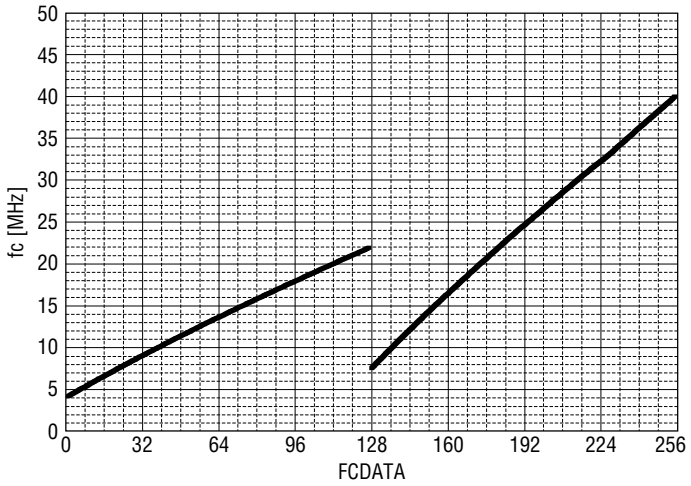


Figure 1. Cutoff frequency vs. FCDATA (R_{ISET} = 1.8kΩ)

R_{ISET}

R_{ISET} controls the internal current source, and its connection is essential. The recommended value (R_{ISET}) is 1.8kΩ. In power-down mode and filter bypass mode, no current flows into R_{ISET}.

Note. A value other than 1.8kΩ will change the current consumption of SM5309A. In the determination of resistance value, caution should be taken to ensure the power dissipation does not exceed the absolute maximum rating for the package.

Half fc Mode

In half fc mode, the CH-2 and CH-3 cutoff frequency is 1/2 that of the CH-1 cutoff frequency setting. Half fc mode is useful for systems where the sampling frequency varies due to luminance (Y) and color difference signal (Cr, Cb) requirements as in component signals.

Group Delay Characteristics

The group delay varies with the cutoff frequency setting. Note also that in half fc mode, the group delay between CH-1 and CH-2/CH-3 varies.

Filter Bypass Mode

In filter bypass mode, the internal lowpass filter in SM5309A is bypassed and the signal is input to the output buffer stage directly. In filter bypass mode, the input type and multiplexer function are set just as for filter mode. But the cutoff frequency setting and fc mode setting have no effect on the outputs. In this mode, the passband frequency is 80MHz (typ), which can support SXGA-class signals.

Input Multiplexer Switching (MUXSEL)

The input multiplexer setting can also be set using the MUXSEL input. When set using the I^2C-BUS, a certain amount of communication time is required, but the setting can be made using the MUXSEL input with arbitrary timing for high-speed switching. The input circuit of MUXSEL pin is placed in analog supply (VCC, GND) area.

MUXSEL pin	MUX flag	Multiplexer selection*1
L: GND	L	INnA
L: GND	H	INnB
H: VCC	L	INnB
H: VCC	H	INnB

*1. n = 1, 2, 3

Power-ON Reset

When power is applied, an internal power-ON reset circuit operates initializing the internal register flags to their default settings. At power-ON, all supplies should be applied simultaneously.

Reference Voltage (REF)

The REFn pins (n = 1, 2) are internal reference voltage outputs. A 10 µF capacitor connected between pin and ground is recommended for stability of movement. REF1 and REF2 are independent reference voltage outputs, and have no correspondence with settings of CH-1, CH-2, and CH-3.

USAGE PRECAUTIONS

Slave Address Setting

When slave address 92h is used, the ADS pin pull-up to VCC. When slave address 94h is used, the ADS input must be left open circuit. In this case, an external resistor should be connected as shown in figure 2 to reduce the risk of malfunction in the I^2C-BUS interface due to large spikes or other noise invaded from outside. The recommended value is 10kΩ.

Direct Input Mode

In direct input mode, the signal is connected to the input without an input capacitor. However, the input DC voltage range varies with the use situation, hence the signal must be appropriately biased for the use situation. If the input voltage exceeds “Direct mode input DC voltage range” (see “Analog input characteristics”), take care of harmonic distortion may occur in the output signal. (For defending device breakdown occur, input bottom voltage and top voltage should be set within the absolute maximum ratings.)

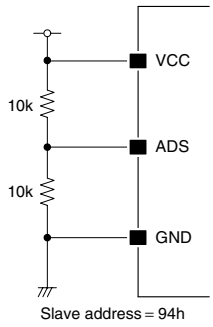


Figure 2. Slave address 94h setting

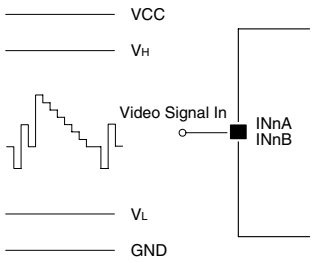


Figure 3. Direct input mode

Power Supply Invest Timing

The SM5309A uses 2-type power supply, analog one (VCC) and I^2C-BUS one (VDD). Therefore all power supply pins should be forced voltage at the same time power supply invested. In the case analog power supply and I^2C-BUS one are set up separately, composing system the time-lag to makes short time as standard under 1ms is need. And if voltage of I^2C-BUS interface power supply comes higher than one of analog power supply, it is necessary to set voltage of I^2C-BUS interface power supply to make potential difference bellow 250mV as compared with voltage of analog one.

TYPICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{DD} = 3.0 to 5.5V, Ta = 25°C, fin = 100kHz, V_{IN} = 1.0Vp-p, R_{ISET} = 1.8kΩ, R_L = 300Ω, unless otherwise noted.

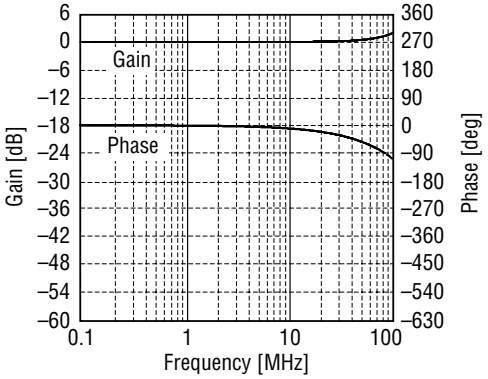


Figure 4. Gain and Phase characteristics (filter bypass mode)

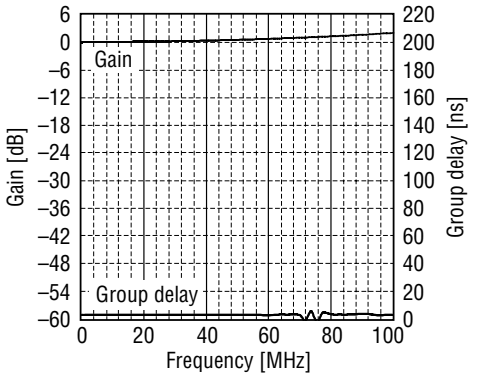


Figure 5. Gain and Group delay characteristics (filter bypass mode)

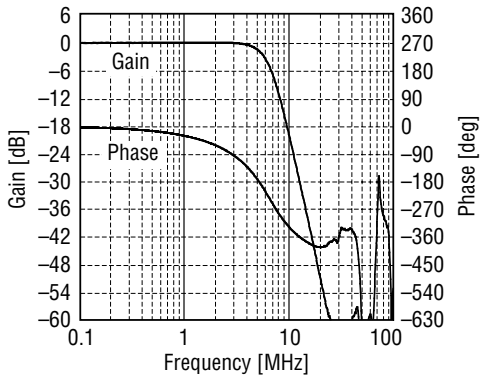


Figure 6. Gain and Phase characteristics (standard fc mode, FCDATA = 10)

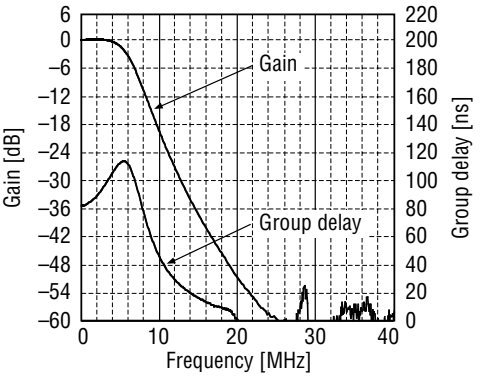


Figure 7. Gain and Group delay characteristics (standard fc mode, FCDATA = 10)

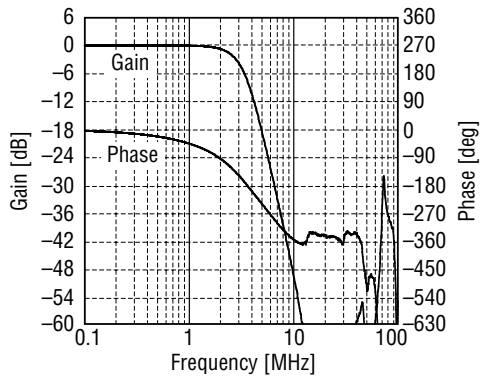


Figure 8. Gain and Phase characteristics (half fc mode, FCDATA = 10)

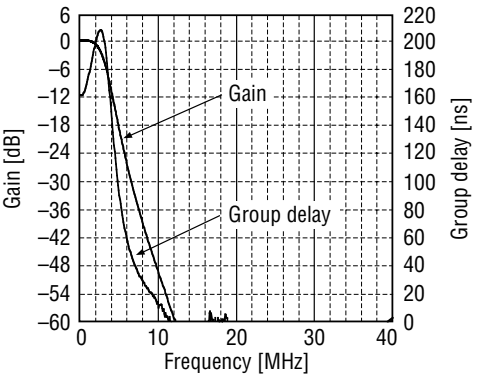


Figure 9. Gain and Group delay characteristics (half fc mode, FCDATA = 10)

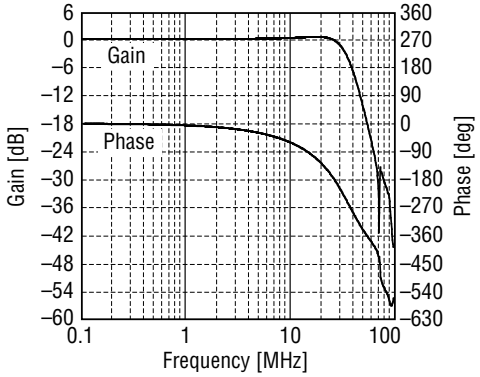


Figure 10. Gain and Phase characteristics
(standard fc mode, FCDATA = 227)

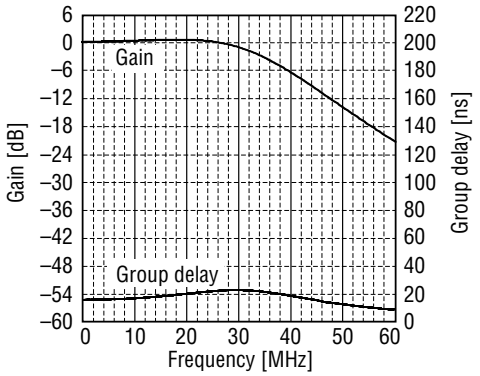


Figure 11. Gain and Group delay characteristics
(standard fc mode, FCDATA = 227)

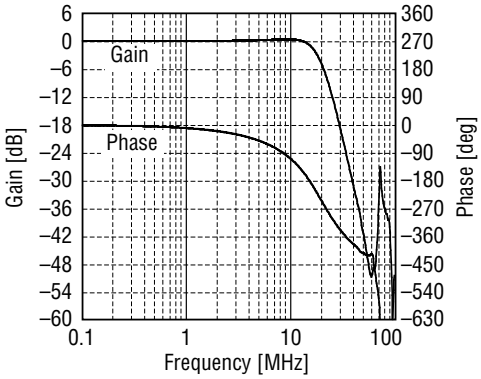


Figure 12. Gain and Phase characteristics
(half fc mode, FCDATA = 227)

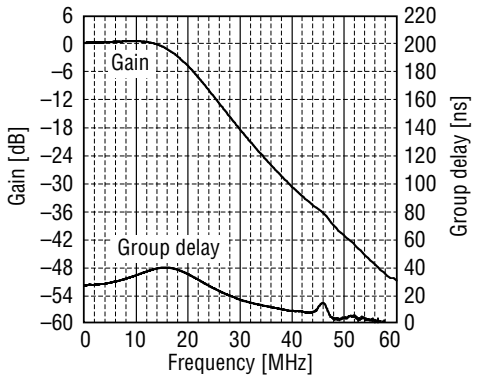


Figure 13. Gain and Group delay characteristics
(half fc mode, FCDATA = 227)

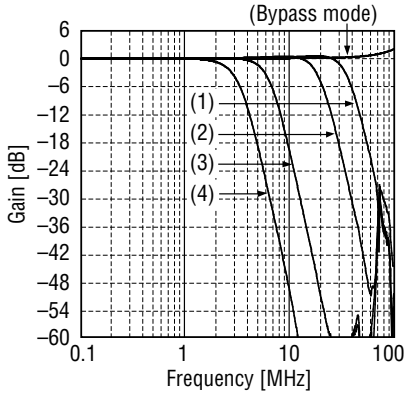


Figure 14. Gain vs. FCDATA, fc mode

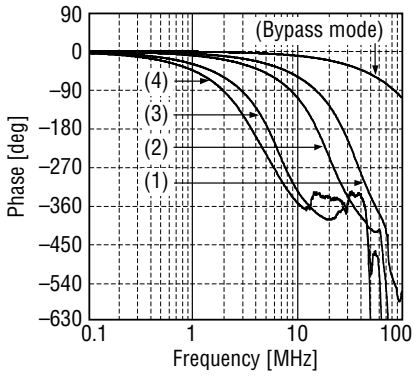


Figure 15. Phase vs. FCDATA, fc mode

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half

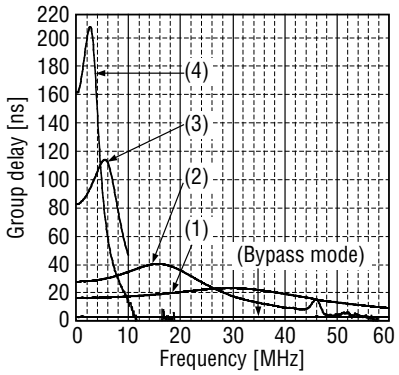
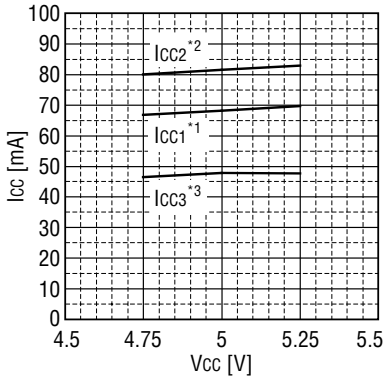


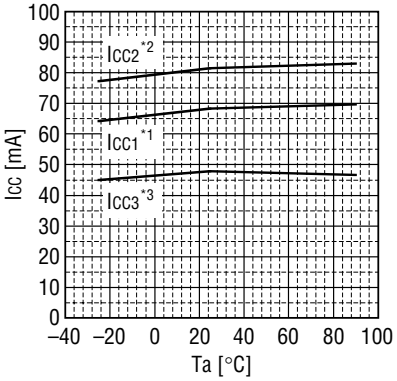
Figure 16. Group delay vs. FCDATA, fc mode

	FCDATA	fc mode
(1)	227	standard
(2)	227	half
(3)	10	standard
(4)	10	half



*1. filter mode, FCDATA = 0
*2. filter mode, FCDATA = 255
*3. filter bypass mode

Figure 17. $I_{CC1, 2, 3}$ vs. V_{CC}



*1. filter mode, FCDATA = 0
*2. filter mode, FCDATA = 255
*3. filter bypass mode

Figure 18. $I_{CC1, 2, 3}$ vs. Ta

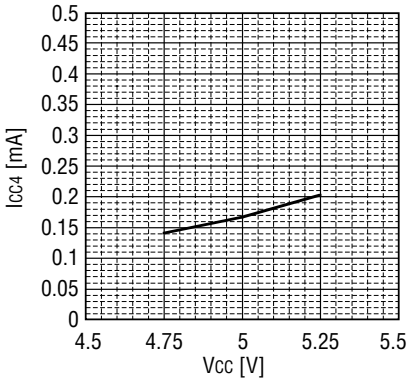


Figure 19. I_{CC4} vs. V_{CC}

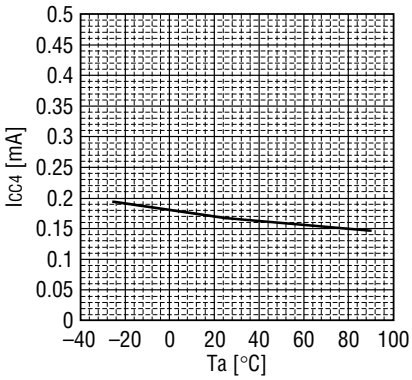


Figure 20. I_{CC4} vs. Ta

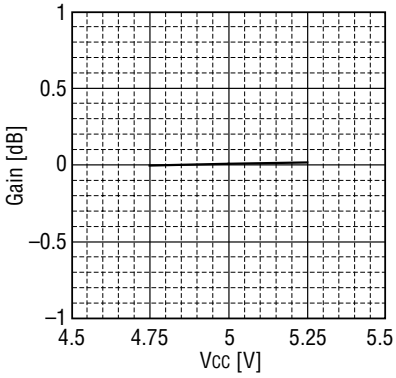


Figure 21. Gain vs. V_{CC}

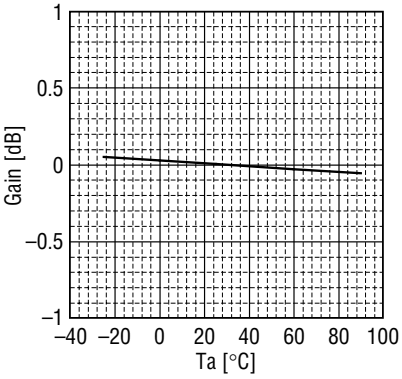


Figure 22. Gain vs. Ta

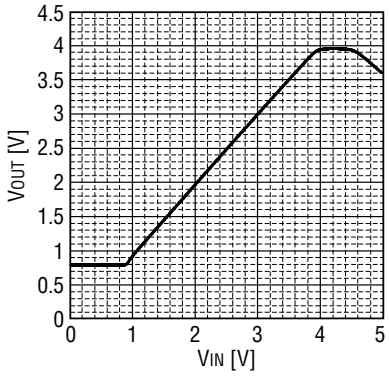


Figure 23. V_{IN} vs. V_{OUT}
(filter mode, direct mode)

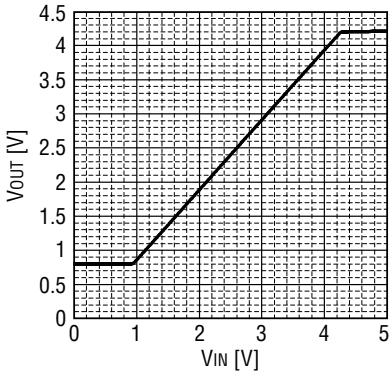


Figure 24. V_{IN} vs. V_{OUT}
(filter bypass mode, direct mode)

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NPC

SEIKO NPC CORPORATION

1-9-9, Hatchobori, Chuo-ku,
Tokyo 104-0032, Japan
Telephone: +81-3-5541-6501
Facsimile: +81-3-5541-6510
http://www.npc.co.jp/
Email: sales@npc.co.jp

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