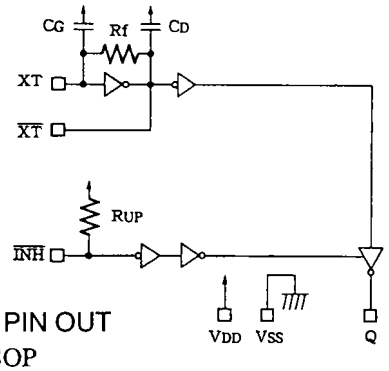
■ OVERVIEW

The SM5613 series are C-MOS ICs for quartz crystal oscillating module. Each IC has a high frequency oscillating circuit and an output buffer with low current consumption.
There are many kinds of type-capacitor for oscillation on chip or not, output level-TTL or CMOS, output drivability - 10TTL or 10LSTTL. (Refer to the SERIES TABLE).

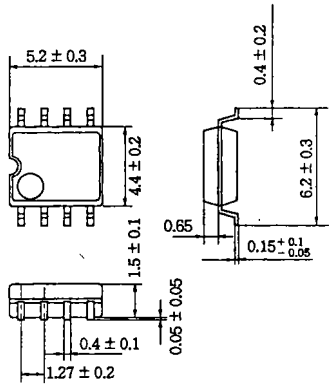
■ FEATURES

- Operating voltage (4.5 ~ 5.5V)
- Built-in feed back resistance of oscillating circuit
- 3-state function
- Available up to 50MHz
- Low current consumption
- Chip form, 8-pin SOP
- Molybdenum gate C-MOS
- For third overtone wave use

■ BLOCK DIAGRAM



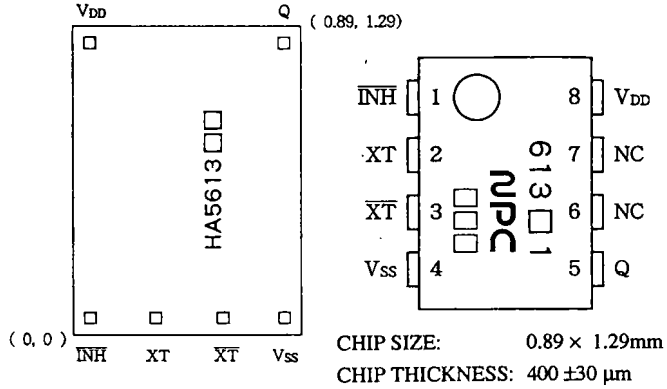
■ PACKAGE DIMENSION (UNIT: mm)



■ PIN OUT

• 8 PIN SOP

(TOP VIEW)



CHIP SIZE: 0.89 × 1.29mm
CHIP THICKNESS: 400 ±30 µm

■ PIN COORDINATES

UNIT: µm

NAME	X	Y
$\overline{INH}$	145	140
XT	345	140
$\overline{XT}$	545	140
V_{SS}	745	140
Q	745	1150
V_{DD}	145	1155

■ PIN DESCRIPTION

NAME	FUNCTION
XT	Input terminal for oscillating
$\overline{XT}$	Output terminal for oscillating
$\overline{INH}$	"L" ; High impedance On-chip pull-up resistance
V_{DD}	Power supply
V_{SS}	Ground
Q	Output (f_0)

f_0: Oscillating frequency

■ ABSOLUTE MAXIMUM RATING (V_{SS}=0V)

ITEM	SYMBOL	CONDITIONS	UNIT
Supply voltage	V_{DD}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V
Storage temperature	T_{STG1}	-65 to +150	°C
	T_{STG2}	-40 to +125	
Output current	I_{OUT}	H series 10 N, K series 25	mA
* Power dissipation	P_W	200	mW
* Soldering temperature	T_{SLD}	255	°C
* Soldering time	t_{SLD}	10	S

Note: * mark is useful at SOP package.

■ RECOMMENDED OPERATIONAL CONDITIONS

(V_{SS}=0V)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{DD}	4.0	5.0	6.0	V
Input voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating temperature	T_{OPR}	-40		+85	°C

■ ELECTRICAL CHARACTERISTICS

1. N series

(V_{SS}=0V, Ta=-40 to 85°C, unless otherwise noted)

ITEM	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
H-level output voltage	V_{OH}	Q pin, Fig. 1	V_{DD}=4.5V. I_{OH}=16.0mA	3.9	4.2		V
			V_{DD}=4.0V. I_{OH}=14.4mA	3.4	3.7		
L-level output voltage	V_{OL}	Q pin, Fig. 1	V_{DD}=4.5V. I_{OL}=16.0mA		0.3	0.4	V
			V_{DD}=4.0V. I_{OL}=14.4mA		0.3	0.4	
Output leak current	I_Z	Q pin, Fig. 1, $\overline{INH}$="L", V_{DD}=6.0V	V_{OH}=V_{DD}			10	µA
			V_{OL}=V_{SS}			10	
H-level input voltage	V_{IH}	$\overline{INH}$ pin	V_{DD}=5±0.5V	2.0			V
			V_{DD}=5±1.0V	2.2			
L-level input voltage	V_{IL}	$\overline{INH}$ pin	V_{DD}=5±1.0V			0.8	V
Current consumption	I_{DD1}	Load circuit 1, Fig. 2, $\overline{INH}$=OPEN, CL=15pF	V_{DD}=5V, Ta=25°C		25	28	mA
			V_{DD}=5.5V			40	
			V_{DD}=6.0V			45	
	I_{DD2}	Load circuit 1, Fig. 2, $\overline{INH}$=OPEN, CL=50pF	V_{DD}=5V, Ta=25°C		35	38	
			V_{DD}=5.5V			50	
$\overline{INH}$ pin pull-up resistance	R_{UP}	Fig. 3		50		250	kΩ
Feedback resistance	R_f	Fig. 4	V_{DD}=5±0.5V	1.0		5.0	MΩ
			V_{DD}=5±1.0V	0.9		5.5	
Internal capacitor	C_G	Design value		8.5	12	15.5	pF
	C_D			12	17	22	

2. K series

(V_{SS}=0V, Ta=-40 to 85°C, unless otherwise noted)

ITEM	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
H-level output voltage	V_{OH}	Q pin, Fig. 1	V_{DD}=4.5V. I_{OH}=16.0mA	3.9	4.2		V
			V_{DD}=4.0V. I_{OH}=14.4mA	3.4	3.7		
L-level output voltage	V_{OL}	Q pin, Fig. 1	V_{DD}=4.5V. I_{OL}=16.0mA		0.3	0.4	V
			V_{DD}=4.0V. I_{OL}=14.4mA		0.3	0.4	
Output leak current	I_Z	Q pin, Fig. 1, $\overline{INH}$="L", V_{DD}=6.0V	V_{OH}=V_{DD}			10	μA
			V_{OL}=V_{SS}			10	
H-level input voltage	V_{IH}	$\overline{INH}$ pin	V_{DD}=5±0.5V	2.0			V
			V_{DD}=5±1.0V	2.2			
L-level input voltage	V_{IL}	$\overline{INH}$ pin	V_{DD}=5±1.0V			0.8	V
Current consumption	I_{DD1}	Load circuit 1, Fig. 2, $\overline{INH}$=OPEN, CL=15pF	V_{DD}=5V, Ta=25°C		25	28	mA
			V_{DD}=5.5V			40	
			V_{DD}=6.0V			45	
$\overline{INH}$ pin pull-up resistance	R_{UP}	Fig. 3		50		250	kΩ
Feedback resistance	R_f	Fig. 4	V_{DD}=5±0.5V	1.0		5.0	MΩ
			V_{DD}=5±1.0V	0.9		5.5	
Internal capacitor	C_G	Design value		8.5	12	15.5	pF
	C_D			12	17	22	

3. H series

(V_{SS}=0V, Ta=-40 to 85°C, unless otherwise noted)

ITEM	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
H-level output voltage	V_{OH}	Q pin, Fig. 1	V_{DD}=4.5V. I_{OH}=4.0mA	3.9	4.2		V
			V_{DD}=4.0V. I_{OH}=3.6mA	3.4	3.7		
L-level output voltage	V_{OL}	Q pin, Fig. 1	V_{DD}=4.5V. I_{OL}=4.0mA		0.3	0.5	V
			V_{DD}=4.0V. I_{OL}=3.6mA		0.3	0.5	
Output leak current	I_Z	Q pin, Fig. 1, $\overline{INH}$="L", V_{DD}=6.0V	V_{OH}=V_{DD}			10	μA
			V_{OL}=V_{SS}			10	
H-level input voltage	V_{IH}	$\overline{INH}$ pin	V_{DD}=5±0.5V	2.0			V
			V_{DD}=5±1.0V	2.2			
L-level input voltage	V_{IL}	$\overline{INH}$ pin	V_{DD}=5±1.0V			0.8	V
Current consumption	I_{DD1}	Load circuit 1, Fig. 2, $\overline{INH}$=OPEN, CL=15pF	V_{DD}=5V, Ta=25°C		20	25	mA
			V_{DD}=5.5V			35	
			V_{DD}=6.0V			40	
$\overline{INH}$ pin pull-up resistance	R_{UP}	Fig. 3		50		250	kΩ
Feedback resistance	R_f	Fig. 4	V_{DD}=5±0.5V	1.0		5.0	MΩ
			V_{DD}=5±1.0V	0.9		5.5	
Internal capacitor	C_G	Design value		8.5	12	15.5	pF
	C_D			12	17	22	

■ SWITCHING CHARACTERISTICS

1. N series

V_{SS} = 0V, Ta= -40 to +85°C unless otherwise noted.

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{r1}	Load circuit 1, Fig. 2 0.1V_{DD} to 0.9V_{DD}	C_L=15pF	V_{DD}=5±0.5V		2.0	4.0	ns
				V_{DD}=5±1.0V			4.6	
	T_{r2}		C_L=50pF	V_{DD}=5±0.5V		4.0	8.0	
				V_{DD}=5±1.0V			9.5	
Output fall time	T_{f1}	Load circuit 1, Fig. 2 0.9V_{DD} to 0.1V_{DD}	C_L=15pF	V_{DD}=5±0.5V		2.0	4.0	ns
				V_{DD}=5±1.0V			4.6	
	T_{f2}		C_L=50pF	V_{DD}=5±0.5V		4.0	8.0	
				V_{DD}=5±1.0V			9.5	
Output duty cycle	DUTY	Load circuit 2, Fig. 2, C_L=50pF, Ta=25°C, V_{DD}=5.0V			45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V, Load C_L≤50pF					100	ns
Output enable delay time	T_{PZL}						100	
Maximum operating frequency	f_{MAX1}	Load circuit 1, Fig. 2	C_L=15pF	V_{DD}=5±1.0V	50			MHz
	f_{MAX2}		C_L=50pF	V_{DD}=5±0.5V	50			
Minimum operating frequency	f_{MIN}	Load circuit 1, Fig. 2, C_L=50pF, V_{DD}=5±1.0V					30	MHz

2. K series

V_{SS} = 0V, Ta= -40 to +85°C unless otherwise noted.

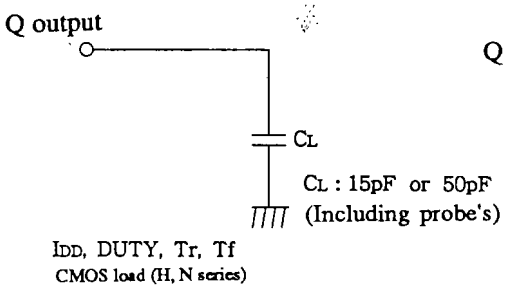
ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{r1}	Load circuit 2, Fig. 2 0.4V_{DD} to 2.4V_{DD}	C_L=15pF	V_{DD}=5±0.5V		1.5	3.0	ns
				V_{DD}=5±1.0V			3.5	
	T_{r2}		C_L=50pF	V_{DD}=5±0.5V		3.0	6.0	
				V_{DD}=5±1.0V			7.0	
Output fall time	T_{f1}	Load circuit 2, Fig. 2 2.4V_{DD} to 0.4V_{DD}	C_L=15pF	V_{DD}=5±0.5V		1.5	3.0	ns
				V_{DD}=5±1.0V			3.5	
	T_{f2}		C_L=50pF	V_{DD}=5±0.5V		3.0	6.0	
				V_{DD}=5±1.0V			7.0	
Output duty cycle	DUTY	Load circuit 2, Fig. 2, C_L=15pF, Ta=25°C, V_{DD}=5.0V			45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V, Load C_L≤50pF					100	ns
Output enable delay time	T_{PZL}						100	
Maximum operating frequency	f_{MAX}	Load circuit 2, Fig. 2, V_{DD}=5±1.0V			50			MHz
Minimum operating frequency	f_{MIN}	Load circuit 2, Fig. 2, V_{DD}=5±1.0V					30	MHz

3. H series

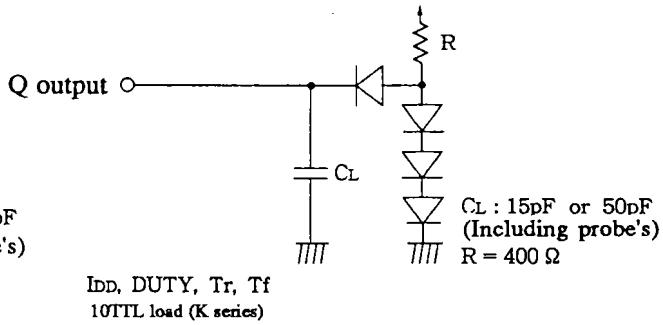
V_{SS} = 0V, Ta= -40 to +85°C unless otherwise noted.

ITEM	SYMBOL	CONDITIONS			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Output rise time	T_{r1}	Load circuit 1, Fig. 2 0.1V_{DD} to 0.9V_{DD}	C_L=15pF	V_{DD}=5±0.5V		5.0	10	ns
				V_{DD}=5±1.0V			12	
	T_{r2}		C_L=50pF	V_{DD}=5±0.5V		13	26	
				V_{DD}=5±1.0V			30	
Output fall time	T_{f1}	Load circuit 1, Fig. 2 0.9V_{DD} to 0.1V_{DD}	C_L=15pF	V_{DD}=5±0.5V		5.0	10	ns
				V_{DD}=5±1.0V			12	
	T_{f2}		C_L=50pF	V_{DD}=5±0.5V		13	26	
				V_{DD}=5±1.0V			30	
Output duty cycle	DUTY	Load circuit 1, Fig. 2, C_L=15pF, Ta=25°C, V_{DD}=5.0V			45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, Ta=25°C, V_{DD}=5±1.0V, Load C_L≤50pF					100	ns
Output enable delay time	T_{PZL}						100	
Minimum operating frequency	f_{MAX}	Load circuit 1, Fig. 2, V_{DD}=5±1.0V			50			MHz
Maximum operating frequency	f_{MIN}	Load circuit 1, Fig. 2, V_{DD}=5±1.0V					30	MHz

■ LOAD CIRCUIT



Load Circuit 1 (H, N versions)



Load Circuit 2 (K versions)

■ TEST CIRCUIT

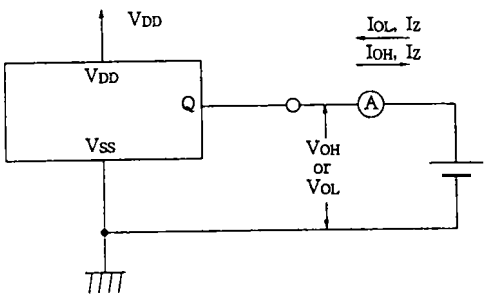


Fig. 1

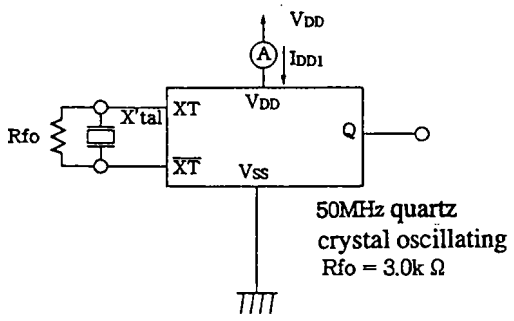


Fig. 2

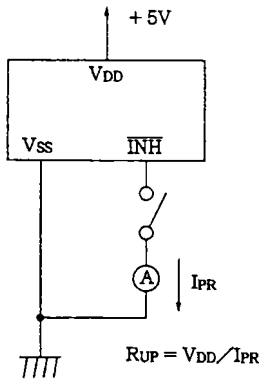


Fig. 3

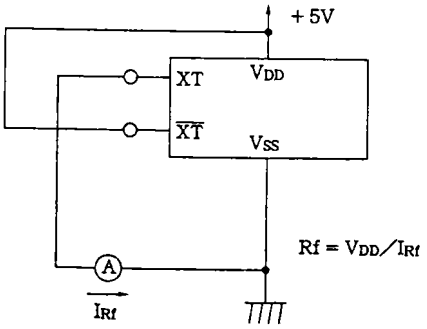
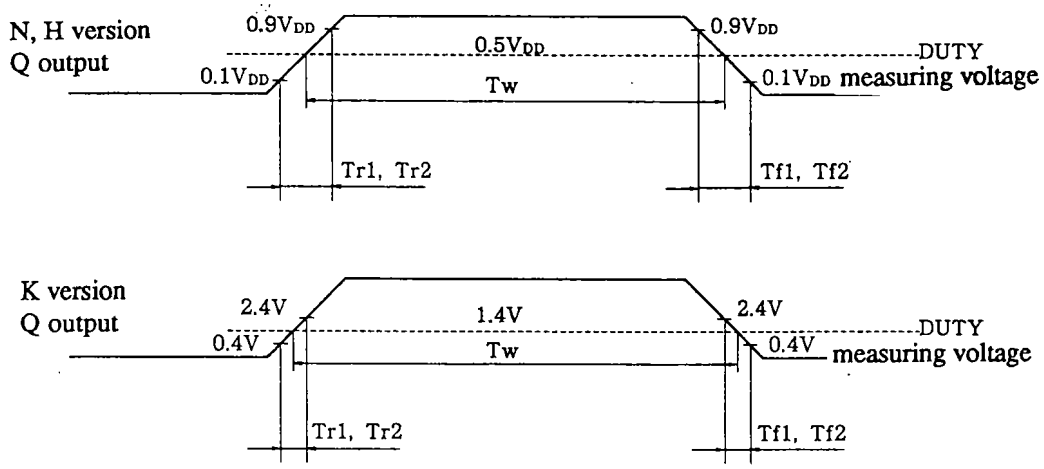
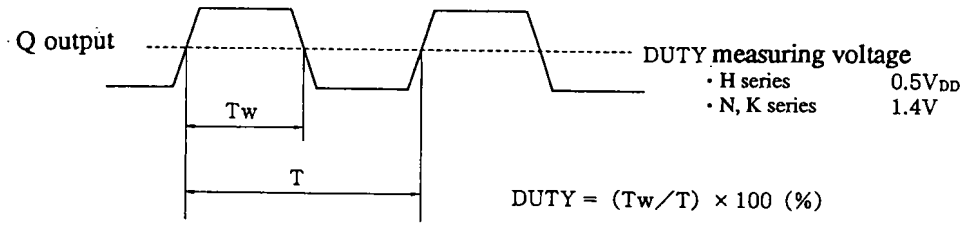


Fig. 4

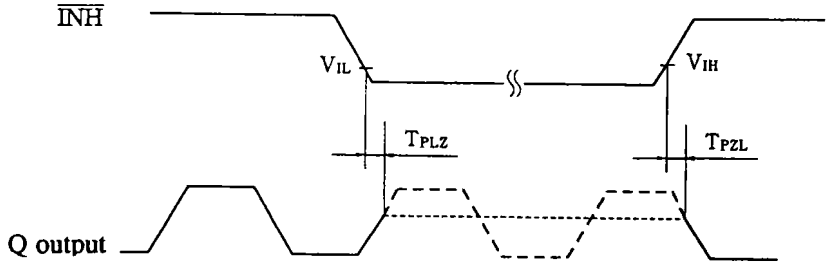
■ WAVEFORMS FOR SWITCHING TIME



■ DUTY FACTOR



■ OUTPUT DISABLE TIME



■ SERIES TABLE

Versions	Output frequency	Built-in capacity	Output current (mA)	Fan out (TTL)	Input level	Output level	Delivery Form
SM5613N1	f_o	○	16	10	TTL	CMOS	Chip
N1S	f_o	○	16	10	TTL	CMOS	8Pin SOP
K1	f_o	○	16	10	TTL	TTL	Chip
K1S	f_o	○	16	10	TTL	TTL	8Pin SOP
H1	f_o	○	4	10LS	TTL	CMOS	Chip
H1S	f_o	○	4	10LS	TTL	CMOS	8Pin SOP

■ FUNCTION

CONTROL	OUTPUT TERMINAL
$\overline{INH}$	Q
H (OPEN)	Output (f_o)
L	High impedance

f_o : Oscillating frequency