

■ OVERVIEW

The SM5623N Series is a range of quartz oscillator ICs fabricated using NPC's original molybdenum-gate CMOS technology. Each IC consists of a high-frequency, low-current oscillator circuit and output buffer. The IC incorporates a high-precision, thin-film feedback resistor and oscillation capacitors having excellent frequency characteristics, and thus ensures stable third overtone oscillation with no load.

■ FEATURES

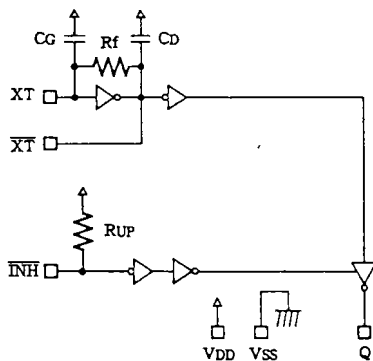
- Up to 100 MHz frequency
- Triple wave
- Built-in feedback resistor in inverter amplifier
- Built-in oscillation capacitors CG and CD
- Output tristate function
- Input TTL compatible
- Low current consumption
- Operating voltage
  - 3 V operation ( $33\text{MHz} \leq f_o < 70\text{MHz}$ )
  - 5 V operation ( $45\text{MHz} \leq f_o \leq 100\text{MHz}$ )
- Chip form
- Molybdenum-gate® CMOS construction

■ PIN DESCRIPTION

Name	Function
XT	Oscillation input
$\overline{\text{XT}}$	Oscillation output
INH	"L": output high impedance. Internal pull-up resistor.
V <sub>DD</sub>	Supply voltage
V <sub>SS</sub>	Ground
Q	Output ( $f_o$ )

$f_o$ : fundamental frequency

■ BLOCK DIAGRAM

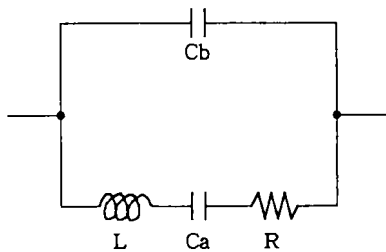


## ■ SERIES LINEUP

Version Name	Frequency range (MHz)		Output duty level	Output current (mA)	Internal capacitor (pF)		Rf (kΩ)
	3 V operation	5 V operation			C <sub>G</sub>	C <sub>D</sub>	
SM5623NA	33 to 44	45 to 62	CMOS	16	12	17	4.7
NB	37 to 48	50 to 67	CMOS	16	12	17	3.9
NC	41 to 52	55 to 72	CMOS	16	12	17	3.3
ND	45 to 56	60 to 77	CMOS	16	12	17	2.7
NE	50 to 63	65 to 82	CMOS	16	10	10	3.3
NF	54 to 68	72 to 90	CMOS	16	10	10	2.7
NG	60 to 70	81 to 100	CMOS	16	10	10	2.2

The recommended operating frequency of each version is the data of the NPC's quartz crystal.

### NPC's correlation quartz crystal data



f (MHz)	R (Ω)	L (mH)	Ca (fF)	Cb (pF)
30	18.62	16.24	1.733	5.337
40	20.53	11.34	1.396	3.989
50	22.17	7.40	1.370	4.105
60	22.20	5.05	1.388	4.226
70	25.42	4.18	1.254	5.170
80	24.24	4.12	1.270	5.183
100	16.60	3.56	0.726	5.394

## ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5	V
Output voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5	V
Storage temperature	T <sub>STG</sub>	-65 to +150	°C
Output current	I <sub>OUT</sub>	25	mA

## ■ RECOMMENDED OPERATING CONDITIONS

### • 3 V operation

(V<sub>SS</sub> = 0V)

Item	Symbol	MIN	TYP	MAX	Unit
Operating supply voltage	f ≤ 50MHz	V <sub>DD</sub>	2.7	3.6	V
	50MHz < f ≤ 70MHz		3.0	3.6	
Input voltage	V <sub>IN</sub>	V <sub>SS</sub>		V <sub>DD</sub>	V
Operating temperature	T <sub>OPR</sub>	-20		+80	°C

### • 5 V operation

(V<sub>SS</sub> = 0V)

Item	Symbol	MIN	TYP	MAX	Unit
Operating supply voltage	V <sub>DD</sub>	4.5		5.5	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub>		V <sub>DD</sub>	V
Operating temperature	T <sub>OPR</sub>	-20		+80	°C

## ELECTRICAL CHARACTERISTICS

In the recommended operating conditions and  $V_{SS} = 0$  V unless otherwise specified.

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
INH pin, pull-up resistance	$R_{UP}$	Measuring circuit 3	50		250	k $\Omega$	
Feedback resistance	$R_f$	Measuring circuit 4	SM5623NA	4.23	4.7	5.17	k $\Omega$
			SM5623NB	3.51	3.9	4.29	
			SM5623NC, NE	2.97	3.3	3.63	
			SM5623ND, NF	2.43	2.7	2.97	
			SM5623NG	1.98	2.2	2.42	
Internal capacitance	$C_G$	*1 Design value	SM5623NA, NB, NC, ND	10.8	12	13.2	pF
	$C_D$			15.3	17	18.7	
	$C_G$			9	10	11	
	$C_D$			9	10	11	

\*1 Guaranteed with wafer monitor pattern.

Not all devices are measured.

### • 3 V operation

In the recommended operating conditions and  $V_{SS} = 0$  V unless otherwise specified.

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
H-level output voltage	$V_{OH}$	Q pin, measuring circuit 1, $V_{DD}=2.7$ V, $I_{OH}=8$ mA	2.2	2.4		V
L-level output voltage	$V_{OL}$	Q pin, measuring circuit 1, $V_{DD}=2.7$ V, $I_{OL}=8$ mA		0.3	0.4	V
Output leak current	$I_Z$	Q pin, measuring circuit 1, $V_{DD}=3.6$ V, $\overline{INH}="L"$	$V_{OH}=V_{DD}$		7	$\mu$ A
			$V_{OL}=V_{SS}$		7	
H-level input voltage	$V_{IH}$	$\overline{INH}$ pin	2.0			V
L-level input voltage	$V_{IL}$	$\overline{INH}$ pin			0.5	V
Current consumption	$I_{DD}$	Measuring circuit 5, load circuit 1, $\overline{INH}=\text{OPEN}$ , $C_L=15$ pF, $f=70$ MHz		17	28	mA

### • 5 V operation

In the recommended operating conditions and  $V_{SS} = 0$  V unless otherwise specified.

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
H-level output voltage	$V_{OH}$	Q pin, measuring circuit 1, $V_{DD}=4.5$ V, $I_{OH}=16$ mA	4.0	4.2		V
L-level output voltage	$V_{OL}$	Q pin, measuring circuit 1, $V_{DD}=4.5$ V, $I_{OL}=16$ mA		0.3	0.4	V
Output leak current	$I_Z$	Q pin, measuring circuit 1, $V_{DD}=3.6$ V, $\overline{INH}="L"$	$V_{OH}=V_{DD}$		10	$\mu$ A
			$V_{OL}=V_{SS}$		10	
H-level input voltage	$V_{IH}$	$\overline{INH}$ pin	2.0			V
L-level input voltage	$V_{IL}$	$\overline{INH}$ pin			0.8	V
Current consumption	$I_{DD}$	Measuring circuit 5, load circuit 1, $\overline{INH}=\text{OPEN}$ , $C_L=15$ pF, $f=100$ MHz		44	71	mA

## ■ SWITCHING CHARACTERISTICS

### • 3V operation

In the recommended operating conditions and VSS = 0V unless otherwise specified.

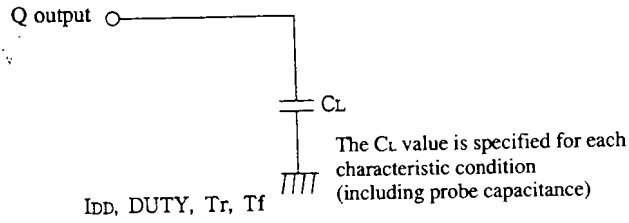
ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Output rise time	$T_r$	Measuring circuit 2, load circuit 1, $C_L=15pF$ , $0.1V_{DD}$ to $0.9V_{DD}$		2	4	ns
Output fall time	$T_f$	Measuring circuit 2, load circuit 1, $C_L=15pF$ , $0.9V_{DD}$ to $0.1V_{DD}$		2	4	ns
Output duty cycle	DUTY	Measuring circuit 2, load circuit 1, $T_a=25^\circ C$ , $V_{DD}=3.3V$ , *1	40		60	%
Output disable delay time	$T_{PLZ}$	Measuring circuit 2, load circuit 1, $T_a=25^\circ C$ , $V_{DD}=3.0V$ , load $C_L \leq 15pF$			150	ns
Output enable delay time	$T_{PZL}$				150	

### • 5V operation

In the recommended operating conditions and VSS = 0V unless otherwise specified.

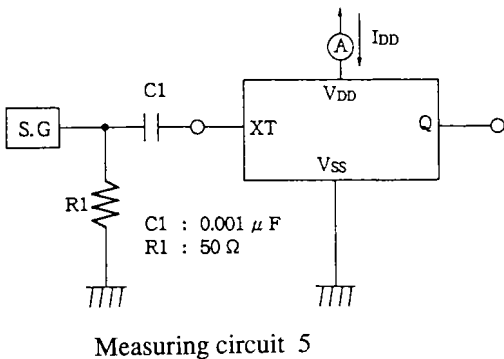
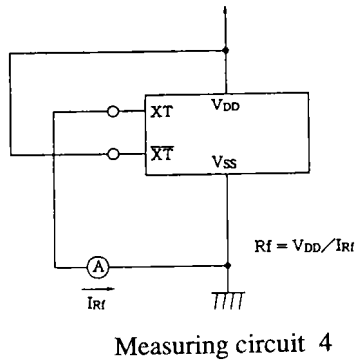
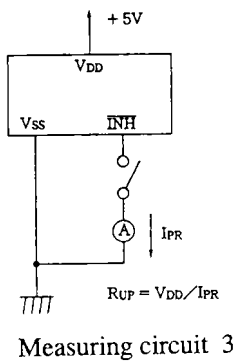
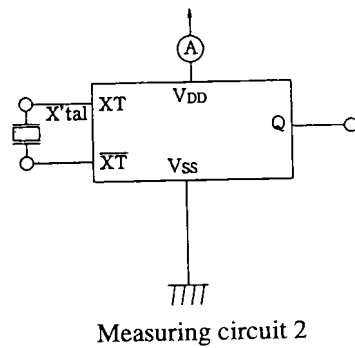
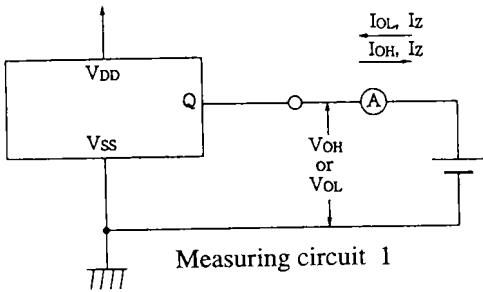
ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
Output rise time	$T_r$	Measuring circuit 2, load circuit 1, $0.1V_{DD}$ to $0.9V_{DD}$	$C_L=15pF$		1.5	3	ns
			$C_L=50pF$		3.5	7	
Output fall time	$T_f$	Measuring circuit 2, load circuit 1, $0.9V_{DD}$ to $0.1V_{DD}$	$C_L=15pF$		1.5	3	ns
			$C_L=50pF$		3.5	7	
Output duty cycle	DUTY	Measuring circuit 2, load circuit 1, $T_a=25^\circ C$ , $V_{DD}=5.0V$ , *1 $C_L=50pF$ ( $f \leq 50MHz$ ), $C_L=15pF$ ( $f \leq 100MHz$ ),	45		55	%	
Output disable delay time	$T_{PLZ}$	Measuring circuit 2, $T_a=25^\circ C$ , $V_{DD}=5.0V$ , load $C_L \leq 15pF$			100	ns	
Output enable delay time	$T_{PZL}$				100		

LOAD CIRCUIT



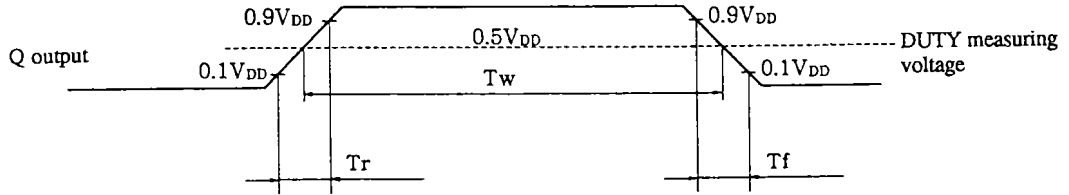
Load circuit 1

MEASURING CIRCUIT

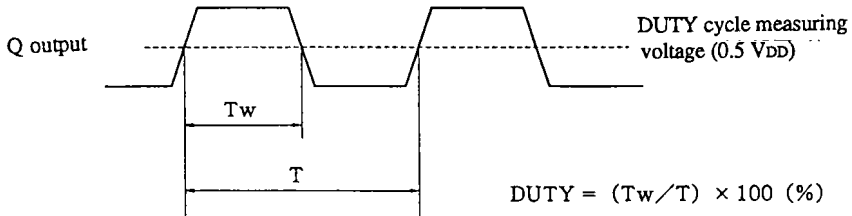


3 V operation -- input signal 2.1 V<sub>p-p</sub>, 70 MHz, sine wave  
5 V operation -- input signal 3.5 V<sub>p-p</sub>, 100 MHz, sine wave

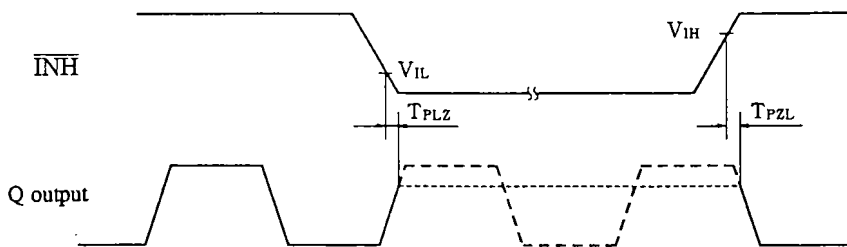
■ SWITCHING TIME WAVEFORM



■ OUTPUT DUTY CYCLE TIME



■ OUTPUT DISABLE TIME

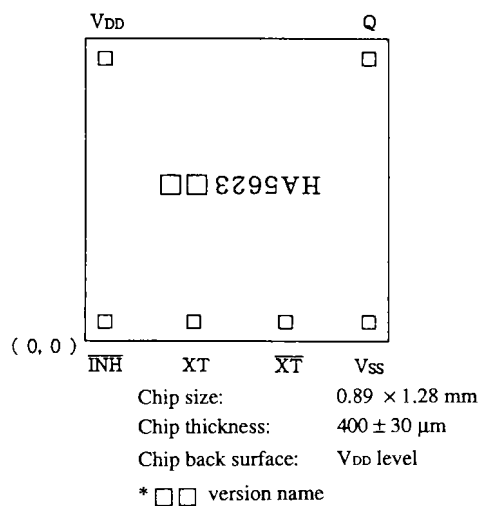


$\overline{INH}$  input waveform  $T_r = T_f$  10 ns or less

## FUNCTIONAL DESCRIPTION

H (open)	fo
L	High impedance

## PAD LAYOUT



## PAD COORDINATES (Unit: μm)

Pin name	X	Y
$\overline{\text{INH}}$	170	183
XT	360	183
$\overline{\text{XT}}$	550	183
V <sub>SS</sub>	740	183
Q	743	1133
V <sub>DD</sub>	136	1133