

■ OVERVIEW

The SM5624N Series is a range of quartz oscillator module ICs fabricated using NPC's original molybdenum-gate CMOS technology. Each IC consists of a low-voltage, low-current oscillator circuit and output buffer. The ICs incorporate oscillation capacitors having excellent frequency characteristics, and thus ensures stable oscillation of a quartz fundamental wave without connecting any external components.

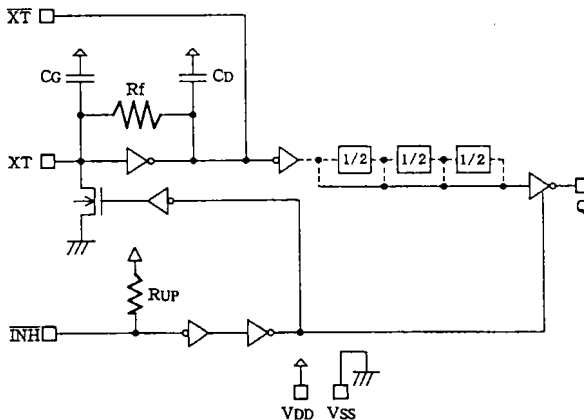
■ FEATURES

- Up to 30 MHz frequency
- Fundamental wave
- Design optimized for a supply voltage of 2.7 to 3.6 V (operating voltage 2.7 to 5.5V)
- Built-in feedback resistor in inverter amplifier
- Chip form
- Molybdenum-gate CMOS construction
- Low current consumption
- Built-in oscillation capacitors CG and CD
- Output tristate function
- Low current consumption
- Standby function (Standby: oscillation stop, output high impedance).

■ PIN DESCRIPTION

Name	Function
XT	Oscillation input
$\bar{X}T$	Oscillation output
$\bar{I}NH$	"L": oscillation stop, output high impedance, internal pull-up resistor (Pull-up resistance changes to limit the standby current)
V <sub>DD</sub>	Supply voltage
V <sub>SS</sub>	Ground
Q	Output pin

■ BLOCK DIAGRAM



## ■ SERIES LINEUP

Version	Output
SM5624 N1	$f_0$
N3	$f_0/2$
N5	$f_0/4$
N7	$f_0/8$

$f_0$ : fundamental frequency

## ■ ABSOLUTE MAXIMUM RATINGS

( $V_{SS} = 0V$ )

Item	Symbol	Rating	Unit
Supply voltage	$V_{DD}$	-0.5 to +7.0	V
Input voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$	V
Output voltage	$V_{OUT}$	-0.5 to $V_{DD} + 0.5$	V
Storage temperature	$T_{STG}$	-65 to +150	°C
Output current	$I_{OUT}$	25	mA

## ■ RECOMMENDED OPERATING CONDITIONS

( $V_{SS} = 0V$ )

Item	Symbol	MIN	TYP	MAX	Unit
Supply voltage	$V_{DD}$	2.7		3.6	V
Input voltage	$V_{IN}$	$V_{SS}$		$V_{DD}$	V
Operating temperature	$T_{OPR}$	-20		+80	°C

## ■ ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 2.7 to 5.5V, V<sub>SS</sub> = 0 V and Ta = -20 to +80°C unless otherwise noted.)

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
H-level output voltage	V <sub>OH</sub>	Q pin, Fig. 1	V <sub>DD</sub> =4.5V, I <sub>OH</sub> =16.0mA	4.0	4.2		V
			V <sub>DD</sub> =2.7V, I <sub>OH</sub> =8mA	2.2	2.4		
L-level output voltage	V <sub>OL</sub>	Q pin, Fig. 1	V <sub>DD</sub> =4.5V, I <sub>OL</sub> =16.0mA		0.3	0.4	V
			V <sub>DD</sub> =2.7V, I <sub>OL</sub> =8mA		0.3	0.4	
H-level input voltage	V <sub>IH</sub>	INH pin		0.7V <sub>DD</sub>			V
L-level input voltage	V <sub>IL</sub>	NH pin				0.3V <sub>DD</sub>	V
Current consumption	I <sub>DD1</sub>	Fig. 2 INH=OPEN C <sub>L</sub> =15pF, f=30MHz, V <sub>DD</sub> =3±0.3V	SM5624N1		6	12	mA
			SM5624N3		4	8	
			SM5624N5		3	6	
			SM5624N7		2	4	
		Fig. 2 INH=OPEN C <sub>L</sub> =15pF, f=30MHz, V <sub>DD</sub> =5±0.5V	SM5624N1		12	24	
			SM5624N3		8	16	
			SM5624N5		6	12	
			SM5624N7		5	10	
Standby current	I <sub>ST</sub>	Fig. 2, INH="L"	V <sub>DD</sub> =3±0.3V		1.5	6	μA
			V <sub>DD</sub> =5±0.5V		4	15	
INH pin pull-up resistance	R <sub>UP1</sub>	Fig. 3	INH=V <sub>SS</sub> , V <sub>DD</sub> =3.6V	2		15	MΩ
	R <sub>UP2</sub>		INH=2.7V, V <sub>DD</sub> =3.6V	50		300	kΩ
Feedback resistance	R <sub>f</sub>	Fig. 4		1.0		10	MΩ
Internal capacitor	C <sub>G</sub>	Design value		18	20	22	pF
	C <sub>D</sub>			18	20	22	

## ■ SWITCHING CHARACTERISTICS

V<sub>SS</sub> = 0V and Ta = -20 to +80°C unless otherwise noted.

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT		
				MIN	TYP	MAX			
Output rise time	T <sub>r1</sub>	Fig. 5	V <sub>DD</sub> =5±0.3V, C <sub>L</sub> =15pF		2	4	ns		
	T <sub>r2</sub>			0.1V <sub>DD</sub>		1.5		3	
	T <sub>r3</sub>			to	V <sub>DD</sub> =5±0.3V, C <sub>L</sub> =30pF			3	6
	T <sub>r4</sub>			0.9V <sub>DD</sub>	V <sub>DD</sub> =5±0.5V, C <sub>L</sub> =50pF			4	8
Output fall time	T <sub>f1</sub>	Fig. 5	V <sub>DD</sub> =5±0.3V, C <sub>L</sub> =15pF		2	4	ns		
	T <sub>f2</sub>			0.9V <sub>DD</sub>		1.5		3	
	T <sub>f3</sub>			to	V <sub>DD</sub> =5±0.3V, C <sub>L</sub> =30pF			3	6
	T <sub>f4</sub>			0.1V <sub>DD</sub>	V <sub>DD</sub> =5±0.5V, C <sub>L</sub> =50pF			4	8
Output duty cycle	DUTY	Fig. 5, C <sub>L</sub> =15pF f=30MHz, Ta=25°C	V <sub>DD</sub> =3.0V	45		55	%		
			V <sub>DD</sub> =5.0V	40		60			
Output disable delay time	T <sub>PLZ</sub>	Fig. 5, Ta=25°C, V <sub>DD</sub> =3.0V, load C <sub>L</sub> ≤30pF				150	ns		
Output enable delay time	T <sub>PZL</sub>					150			
Operating frequency	f	Fig. 5, C <sub>L</sub> =15pF, V <sub>DD</sub> =2.7V to 5.5V,*1		30			MHz		

\* 1: Guaranteed by the lot monitoring

■ MEASURING CIRCUIT

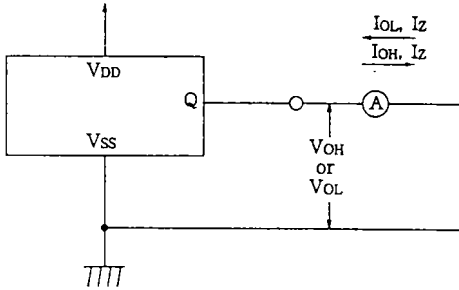


Figure 1

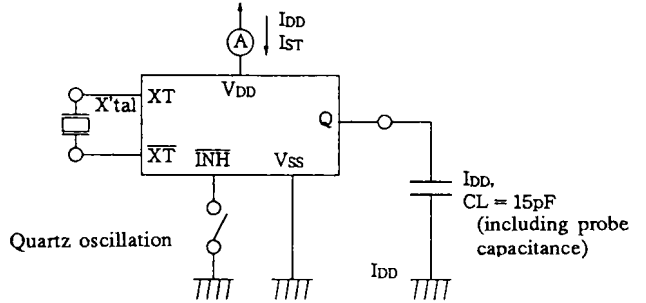


Figure 2

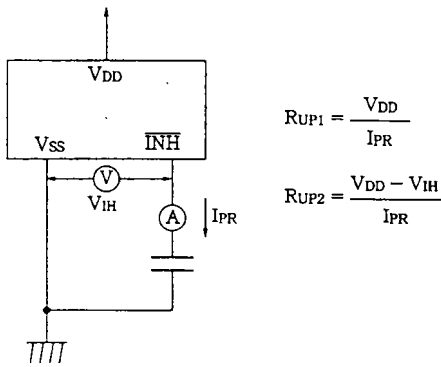


Figure 3

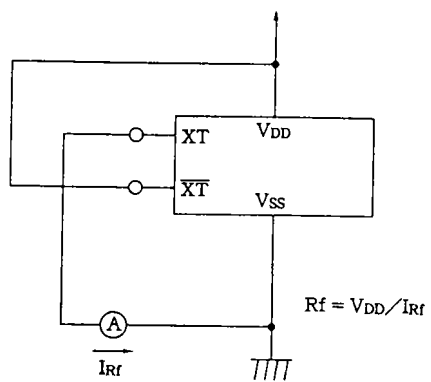


Figure 4

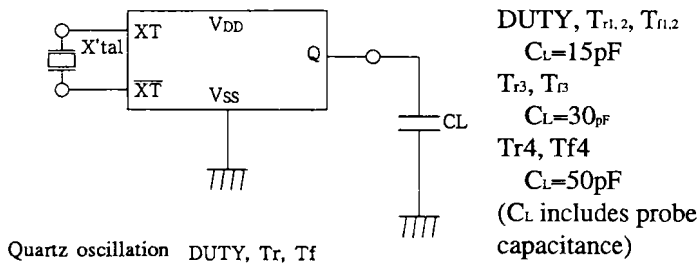
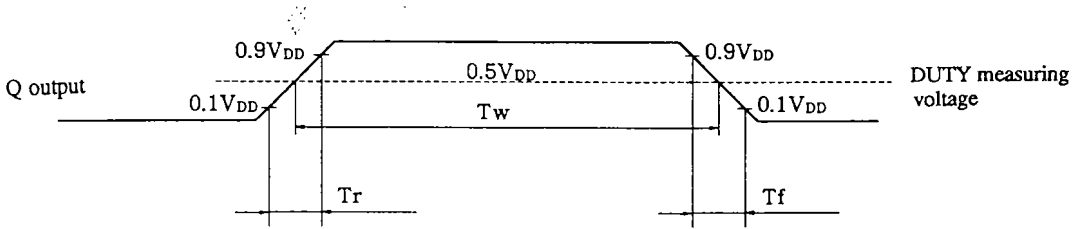
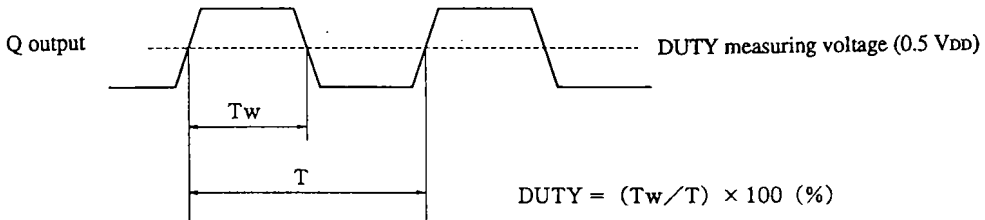


Figure 5

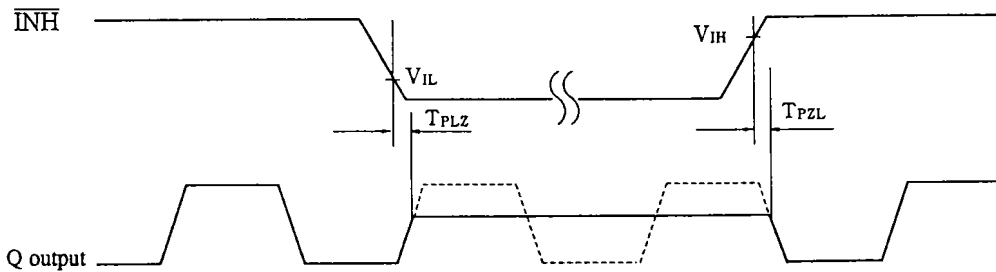
■ SWITCHING TIME MEASURING WAVEFORM



■ OUTPUT DUTY CYCLE TIME

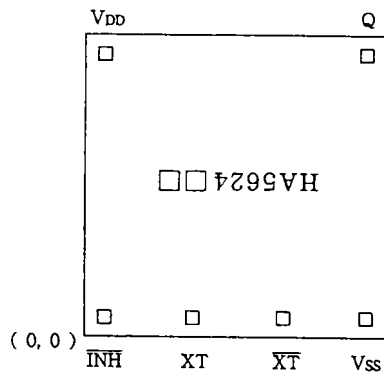


■ OUTPUT DISABLE DELAY TIME, OUTPUT ENABLE DELAY TIME



$\overline{\text{INH}}$  input waveform Tr=Tf 10 ns or less

## ■ PAD LAYOUT



Chip size:  $0.89 \times 1.28\text{mm}$

Chip thickness:  $400 \pm 30 \mu\text{m}$

Check back surface:  $V_{DD}$  level

\* □ □ version name

## ■ PAD COORDINATES (Unit: $\mu\text{m}$ )

Pin name	X	Y
$\overline{\text{INH}}$	170	183
XT	360	183
$\overline{\text{XT}}$	550	183
$V_{SS}$	740	183
Q	743	1133
$V_{DD}$	136	1133