NIPPON PRECISION CIRCUITS INC.

SM5838AS

5120 × 8-bit Synchronous FIFO

OVERVIEW

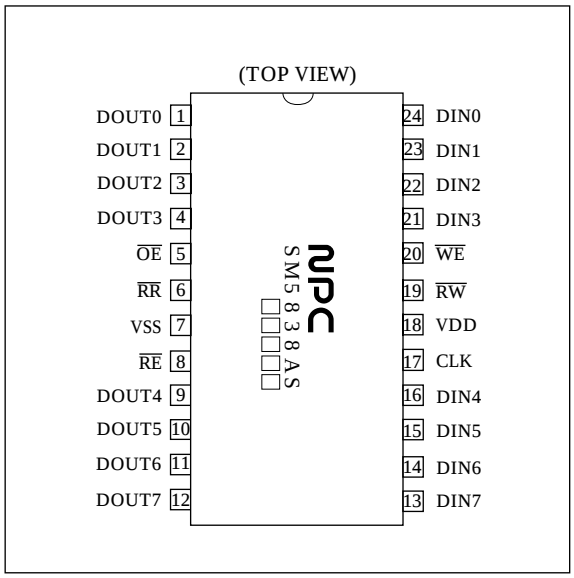
The SM5838AS is a 5120 × 8-bit synchronous FIFO (first in, first out) high-speed line buffer. Internally, it employs static CMOS circuits which mean that it effectively has limitless data hold times. It can operate at speeds up to 33.3 MHz (normal-voltage specification).

The SM5838AS can be used to easily realize a 1-line delay in high-speed facsimile machines and digital copiers.

FEATURES

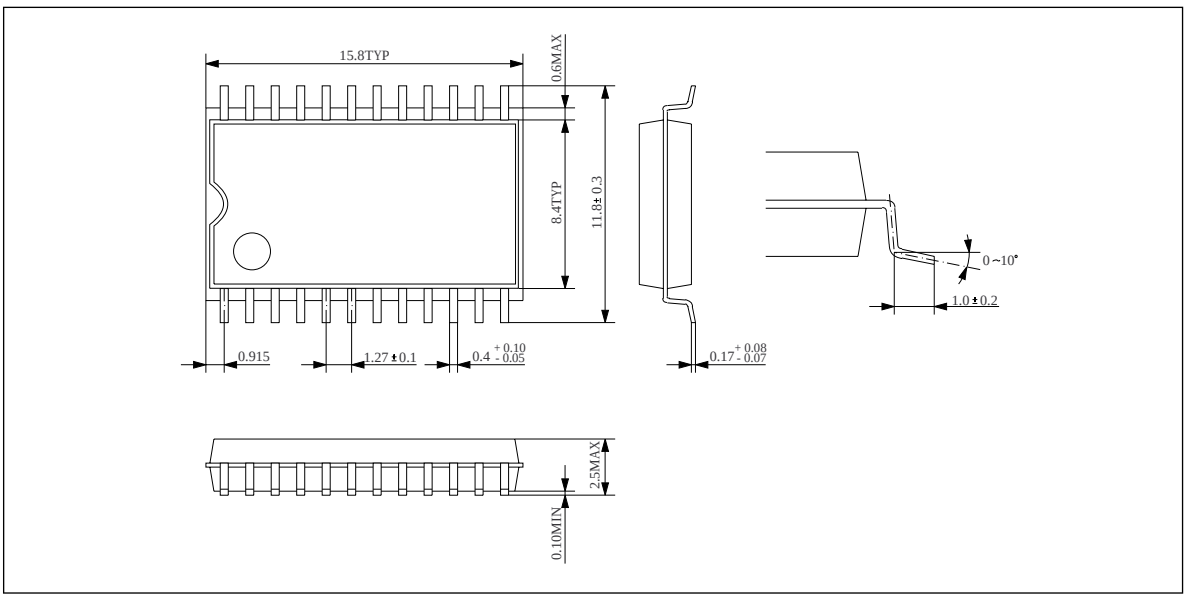
- 5120 × 8-bit structure
- Variable-length delay (21 to 5120 bits)
- 33.3 MHz high-speed operation (normal-voltage specification)
- All input/outputs TTL compatible
- Independent read enable and output enable pins, allowing read address pointer increment in output data hold and output high-impedance states
- Supply voltage
  - 4.5 to 5.5 V (normal-voltage specification)
  - 3.0 to 4.5 V (low-voltage specification)
- 24-pin SOP package
- Molybdenum-gate CMOS process
- A3-paper 1-line (16 dots/mm) compatible

PINOUT

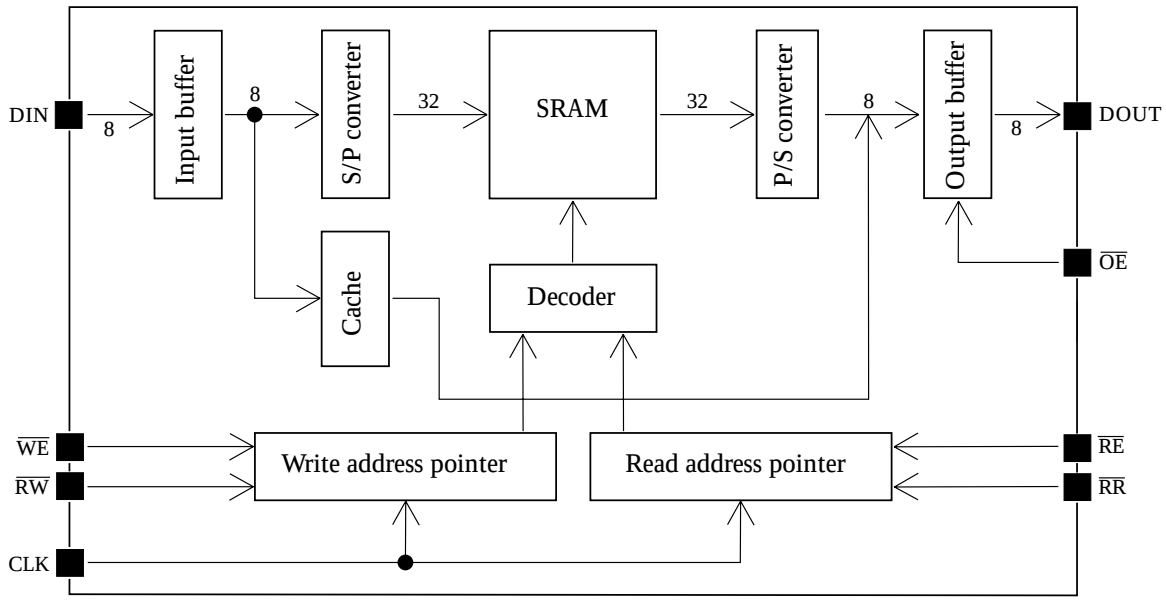


PACKAGE DIMENSIONS

24-pin SOP (Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Function
1	DOUT0	O	Read data output bit 0
2	DOUT1	O	Read data output bit 1
3	DOUT2	O	Read data output bit 2
4	DOUT3	O	Read data output bit 3
5	$\overline{OE}$	I	Output enable input
6	$\overline{RR}$	I	Reset read input
7	VSS	–	Ground (0 V) pin
8	$\overline{RE}$	I	Read enable input (read address pointer)
9	DOUT4	O	Read data output bit 4
10	DOUT5	O	Read data output bit 5
11	DOUT6	O	Read data output bit 6
12	DOUT7	O	Read data output bit 7
13	DIN7	I	Write data input bit 7
14	DIN6	I	Write data input bit 6
15	DIN5	I	Write data input bit 5
16	DIN4	I	Write data input bit 4
17	CLK	I	Clock input
18	VDD	–	Supply pin
19	$\overline{RW}$	I	Reset write input
20	$\overline{WE}$	I	Write enable input (write address pointer)
21	DIN3	I	Write data input bit 3
22	DIN2	I	Write data input bit 2
23	DIN1	I	Write data input bit 1
24	DIN0	I	Write data input bit 0

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.3 to 7.0	V
Input voltage range	V_{IN}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}		–40 to 125	°C
Power dissipation	P_D		500	mW
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage range	V_{DD}	Normal-voltage specification	4.5	5.0	5.5	V
		Low-voltage specification	3.0	3.3	4.5	V
Operating temperature	T_{opr}		–20	–	70	°C

DC Characteristics

Parameter	Symbol	Condition	5 V supply			3 V supply			Unit
			min	typ	max	min	typ	max	
Operating current consumption	I_{DD}	No output load[1]	–	75	90	–	22	30	mA
Standby current consumption	I_{ST}		–	–	50	–	–	50	µA
Input leakage current[2]	I_{LH}	$V_{IN} = V_{DD}$	–	–	1	–	–	1	µA
Input leakage current[3]	I_{LL}	V_{IN} = 0 V	–	–	1	–	–	1	µA
Input voltage[2]	V_{IH}		2.4	–	–	2.0	–	–	V
Input voltage[3]	V_{IL}		–	–	0.5	–	–	0.5	V
Output high-impedance leakage current[4]	I_{ZH}	$\overline{OE}$ = HIGH, $V_{OUT} = V_{DD}$	–	–	5	–	–	5	µA
	I_{ZL}	$\overline{OE}$ = HIGH, V_{OUT} = 0 V	–	–	5	–	–	5	
Output voltage[4]	V_{OH}	I_{OH} = –1 mA	2.5	–	–	2.0	–	–	V
	V_{OL}	I_{OH} = 2 mA	–	–	0.4	–	–	0.8	

1. Normal-voltage specification (CLK = 33.3 MHz); Low-voltage specification (CLK = 20 MHz, V_{DD} = 3.3 ± 0.3 V)
2. Pins CLK, $\overline{RR}$ and $\overline{RE}$.
3. Pins DIN0 to DIN7, $\overline{RW}$, $\overline{WE}$ and $\overline{OE}$.
4. Pins DOUT0 to DOUT7.

Input/Outputs

Ta = 25°C, f = 1 MHz

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input capacitance	C_I		–	–	10	pF
Output capacitance	C_O		–	–	10	pF

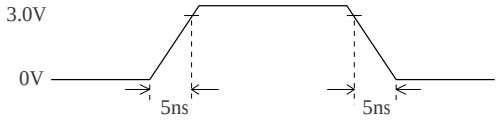
AC Characteristics

Input timing

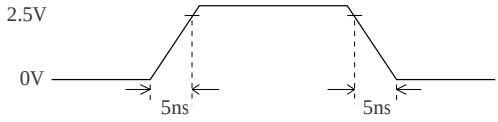
Parameter	Symbol	Condition	5 V supply			3 V supply			Unit
			min	typ	max	min	typ	max	
Clock cycle time	t_{CK}		30	–	–	50	–	–	ns
Clock pulsewidth	t_{CKW}		13	–	–	23	–	–	ns
Input data setup time	t_{DS}		7	–	–	10	–	–	ns
Input data hold time	t_{DH}		3	–	–	4	–	–	ns
$\overline{RW}$ and $\overline{RR}$ setup time	t_{RS}		10	–	–	17	–	–	ns
$\overline{RW}$ and $\overline{RR}$ hold time	t_{RH}		0	–	–	0	–	–	ns
$\overline{WE}$ setup time	t_{WES}		13	–	–	23	–	–	ns
$\overline{WE}$ hold time	t_{WEH}		0	–	–	0	–	–	ns
$\overline{RE}$ setup time	t_{RES}		13	–	–	23	–	–	ns
$\overline{RE}$ hold time	t_{REH}		0	–	–	0	–	–	ns
$\overline{OE}$ setup time	t_{OES}		10	–	–	17	–	–	ns
$\overline{OE}$ hold time	t_{OEH}		0	–	–	0	–	–	ns
Rise and fall transition times	t_f		–	–	30	–	–	30	ns

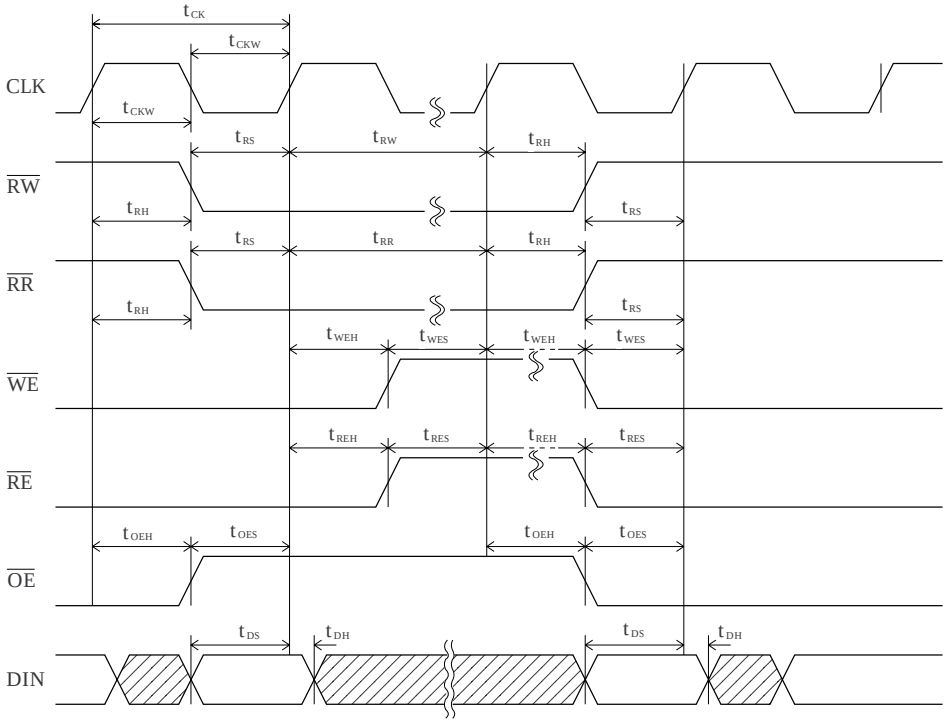
1. All voltages measured with relative to V_{SS}.
2. Input timing input voltage levels are V_{IL} = 0 V and V_{IH} = 3.0/2.5 V (5/3 V supply). Transition time is measured between V_{IH} and V_{IL}.
3. Input signal reference level is V_{TH} = 1.5 V.
4. Input timing ratings measured with t_f = 5 ns.

Normal-voltage (5 V) specification



Low-voltage (3 V) specification



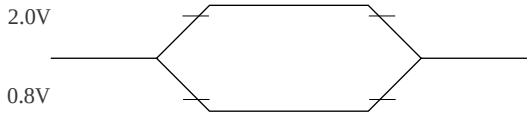


Output timing

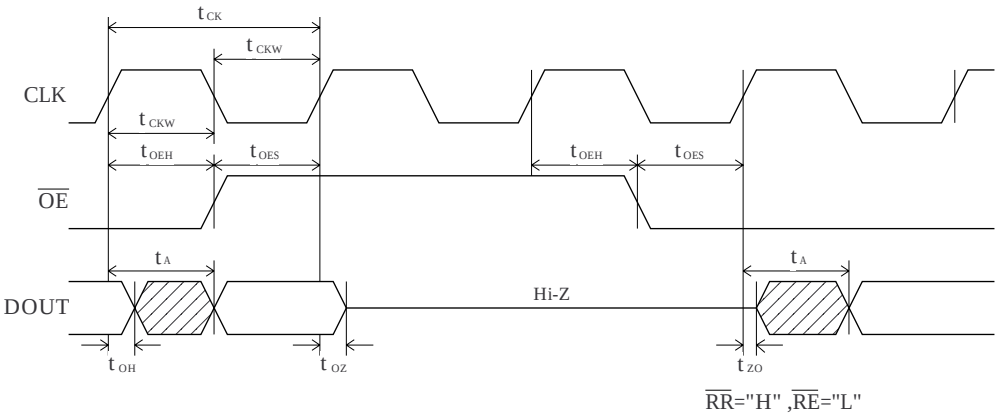
Parameter	Symbol	Condition	5 V supply			3 V supply			Unit
			min	typ	max	min	typ	max	
Access time	t_A	"Load circuit 1"	–	–	20	–	–	40	ns
Output hold time	t_{OH}		5	–	–	5	–	–	ns
Output enable delay time[1]	t_{ZO}	"Load circuit 2"	5	–	27	5	–	40	ns
Output disable delay time[1]	t_{OZ}		5	–	27	5	–	40	ns

1. t_{ZO} and t_{OZ} are measured with ±200 mV tolerance.

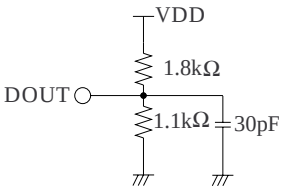
Normal-voltage (5 V) specification



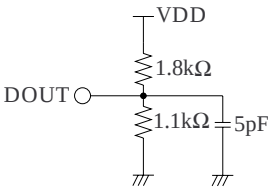
Low-voltage (3 V) specification



Load circuit 1



Load circuit 2



FUNCTIONAL DESCRIPTION

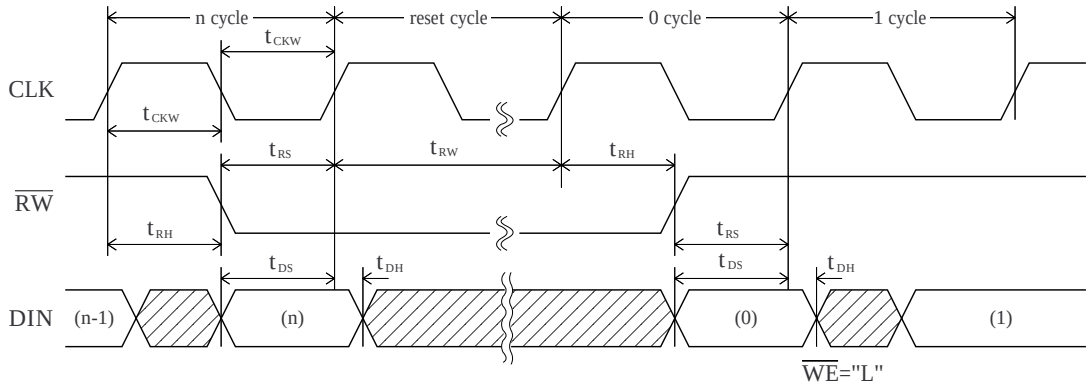
At power-ON reset, device operation can become irregular during the interval when the control circuits are being reset. After power-ON reset is released, this can take up to several 10s of ms in some cases.

Write Reset Cycle, Read Reset Cycle

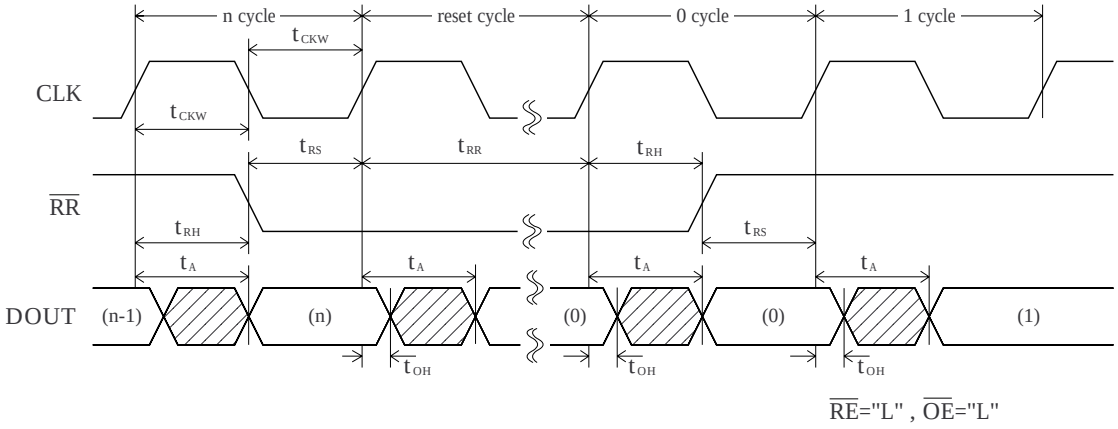
After power-ON, the write address pointer and read address pointer positions are undefined. Accordingly, it is necessary to initialize the pointers using a write reset cycle and read reset cycle, respectively.

A write reset cycle (read reset cycle) is valid when $\overline{RW}$ ($\overline{RR}$) goes LOW for an interval that satisfies both the CLK rising edge setup time (t_{RS}) and hold time (t_{RH}). Note that a write reset cycle (read reset cycle) can occur simultaneously with a write cycle (read cycle). If the cycles are not simultaneous, then the write reset cycle (read reset cycle) is completed at the start of the next write cycle (read cycle).

Write reset cycle



Read reset cycle

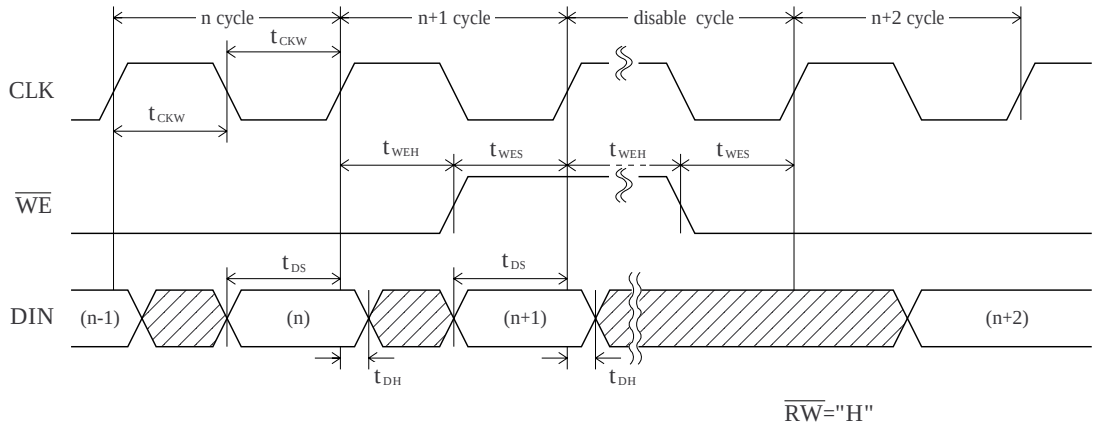


Note the even if a reset period (t_{RW}, t_{RR}) is zero length in the write reset and read reset cycles, the reset operation does take place.

Write Cycle

The input data address is determined by the write address pointer position. The write address pointer is reset by $\overline{RW}$ (write reset cycle), and is incremented on the rising edge of CLK whenever $\overline{WE}$ is LOW. Data input occurs on the rising edge of CLK at the end of the write cycle.

When $\overline{WE}$ goes HIGH, write operation is disabled and the write address pointer stops.

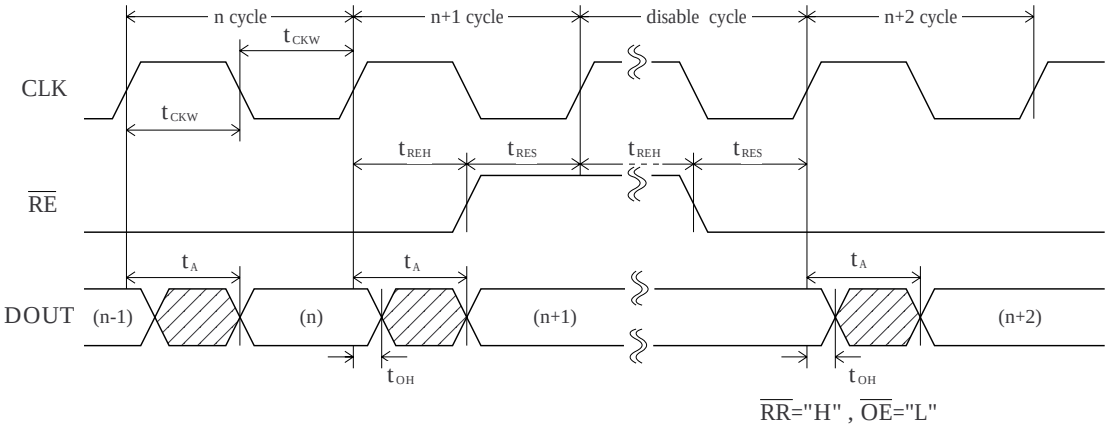


Read Cycle

The output data address is determined by the read address pointer position. The read address pointer is reset by $\overline{RR}$ (read reset cycle), and is incremented on the rising edge of CLK whenever $\overline{RE}$ is LOW. Data output starts t_A (max) after the rising edge of CLK at the start of the read cycle and continues until t_{OH} (min) after the next rising edge of CLK.

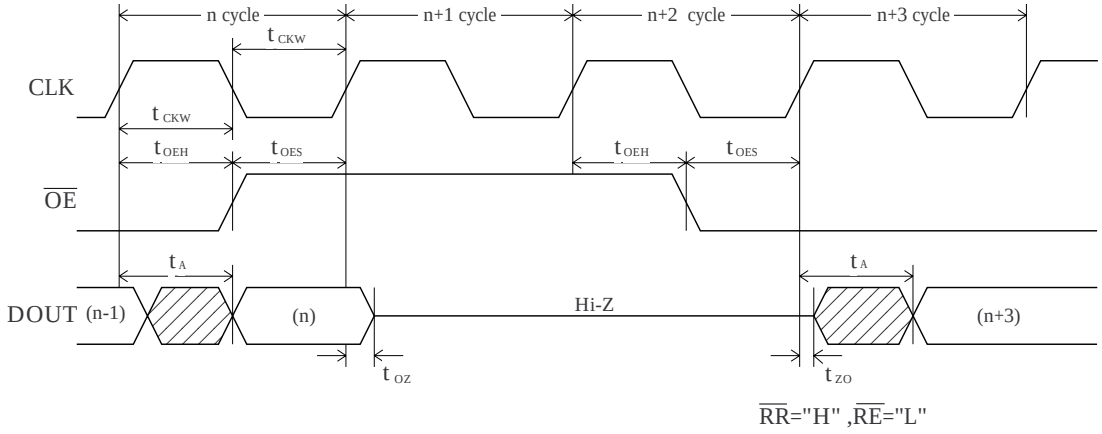
When $\overline{RE}$ goes HIGH, read operation is disabled and the read address pointer stops.

Note that data being read was written at least 20 write cycles previously (FIFO minimum delay). Therefore, if (write address pointer) – (read address pointer) = 1 to 19, then a possibility exists that data from the preceding line is output instead.



Output Enable

When $\overline{OE}$ is HIGH, DOUT0 to DOUT7 become high impedance. Note that because $\overline{RE}$ operation is independent of $\overline{OE}$ operation, the read address pointer can be incremented even when the outputs are high impedance.



TYPICAL APPLICATIONS

Note that at power-ON, the write address pointer and read address pointer positions are undefined. Accordingly, $\overline{RW}$ and $\overline{RR}$ reset cycles are required.

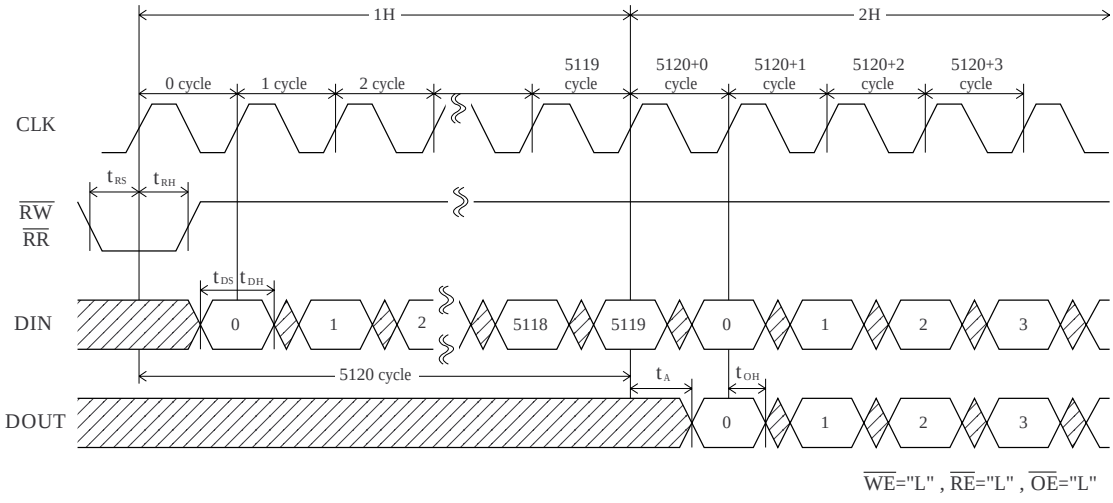
1H Delay Line

A 5120-word delay line can be realized by performing simultaneous write reset and read reset at power-ON.

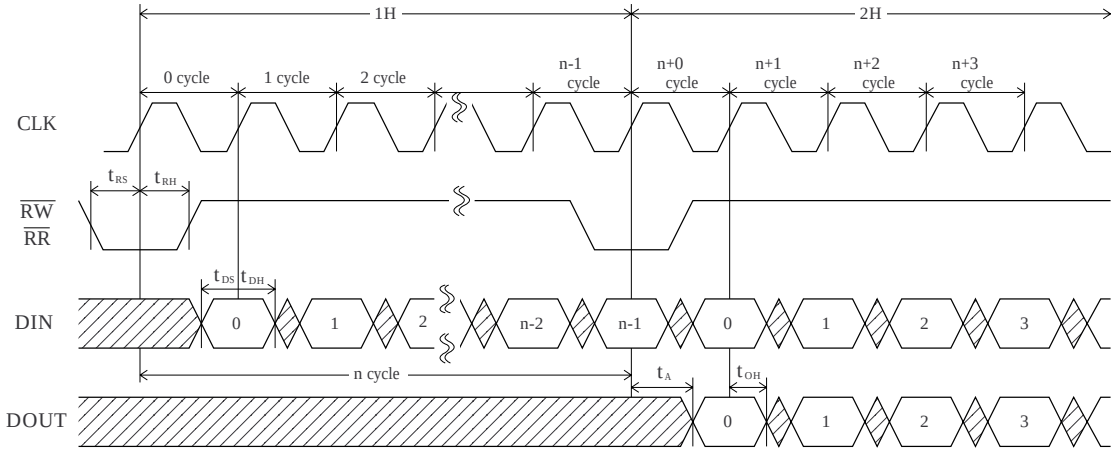
An n-word delay line (21 to 5210-word) can be realized using any of the following methods.

1. Perform reset in sync with desired delay length.
2. Stagger RW and RR timing to desired delay length.
3. Manipulate the write or read address pointer using WE or RE to disable incrementing to maintain sync with desired delay length.

1H (5120-word) delay line timing

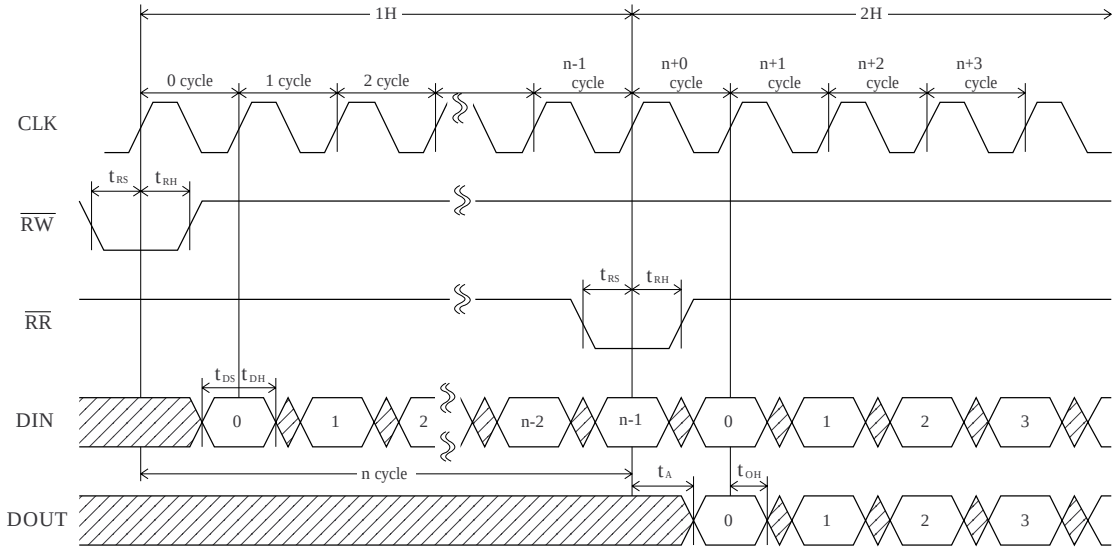


n-word delay line timing 1



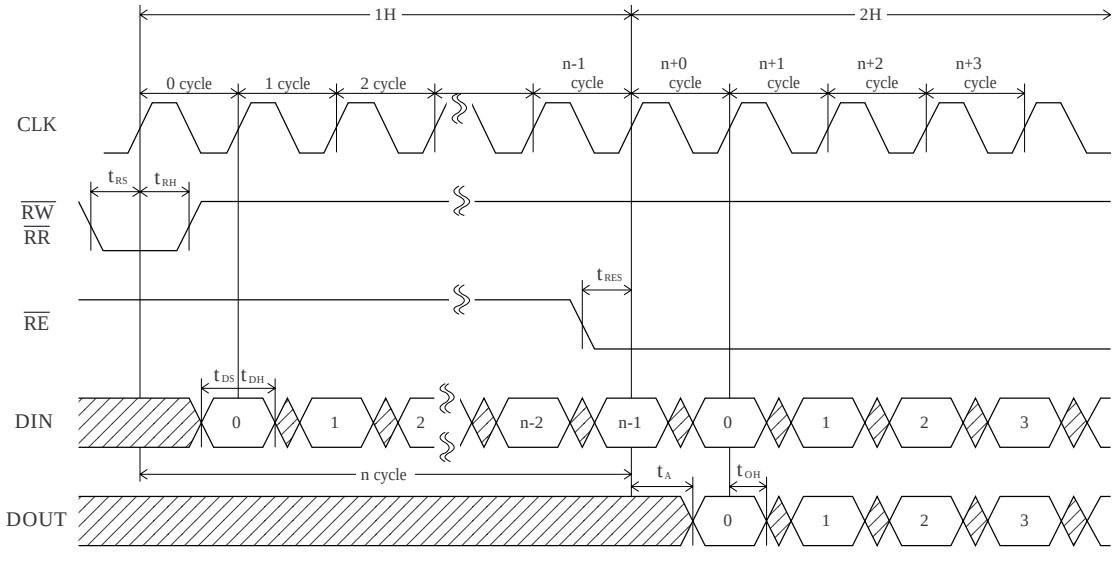
$\overline{WE}$="L" , $\overline{RE}$="L" , $\overline{OE}$="L"

n-word delay line timing 2



$\overline{WE}$="L" , $\overline{RE}$="L" , $\overline{OE}$="L"

n-word delay line timing 3



$\overline{WE}$="L" , $\overline{RE}$="L" , $\overline{OE}$="L"

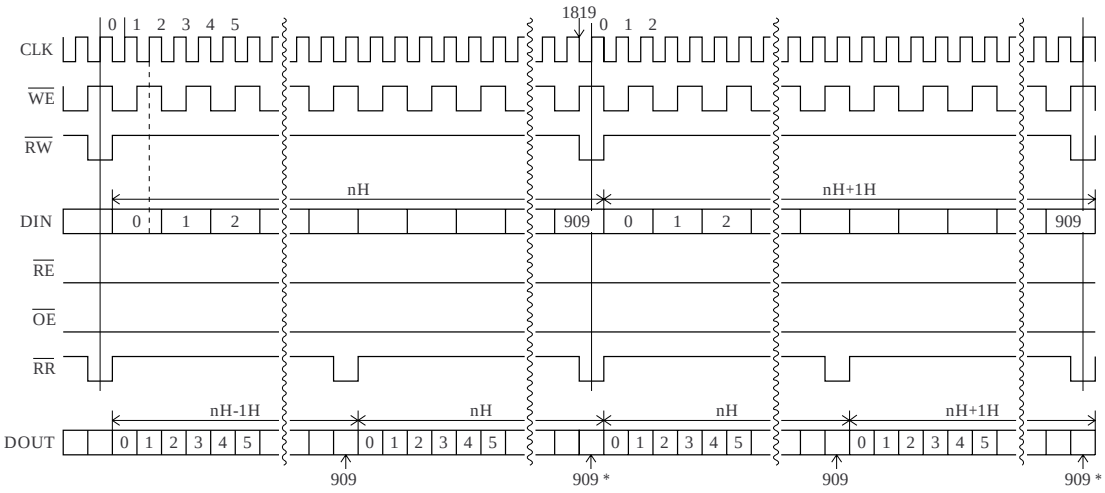
High-speed Conversion

For example, an NTSC signal interlace-to-noninterlace conversion. If interpolated line data can be assumed to be similar to the preceding line data and the write data rate is 14.3 MHz ($4f_{SC}$), then conversion can be realized by reading twice at 28.6 MHz ($8f_{SC}$).

Furthermore, interpolated line data, with appropriate signal processing separation, can be read out line-by-line by alternating between 2 SM5838AS devices (1 line/device).

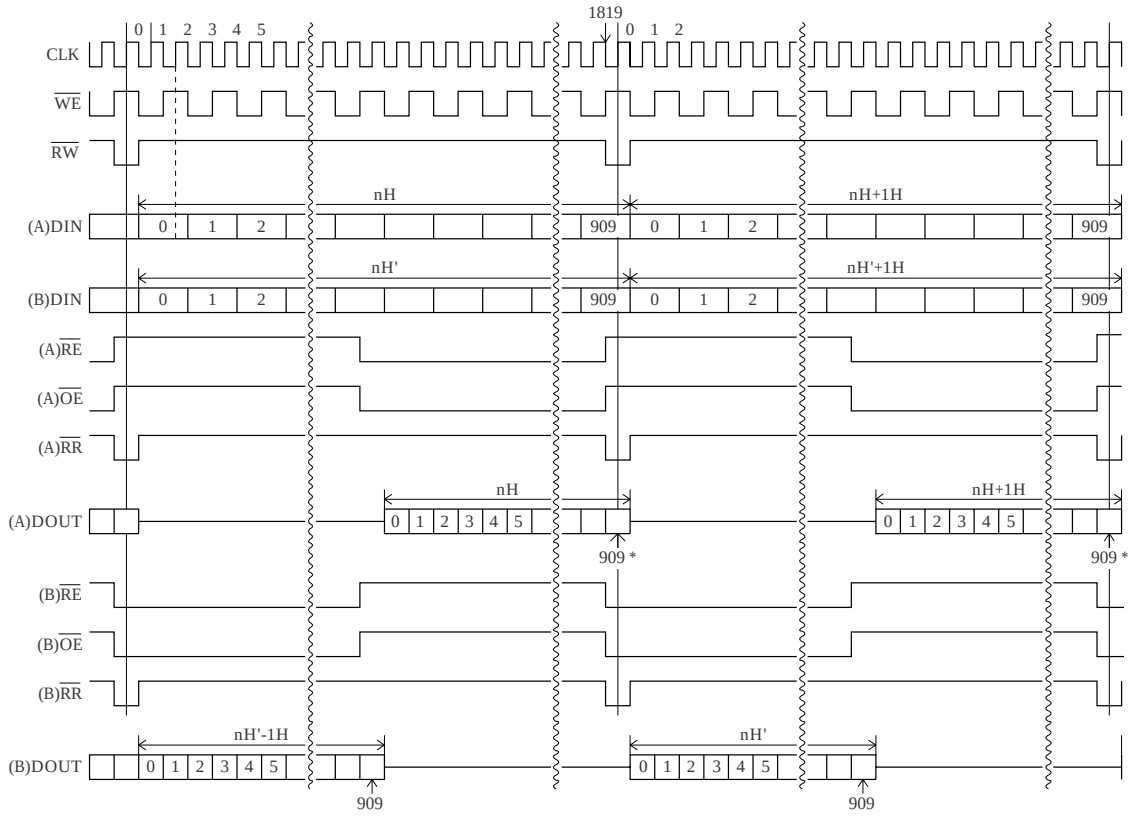
In reality, however, double the number of devices are required for luminance signal (Y) and color difference signal (C) systems. And triple the number of devices are required for RGB signal systems.

Preceding line data used as interpolated line



*Output data 867 to 909 forms the preceding 1H data.

Interpolated data used as interpolated line



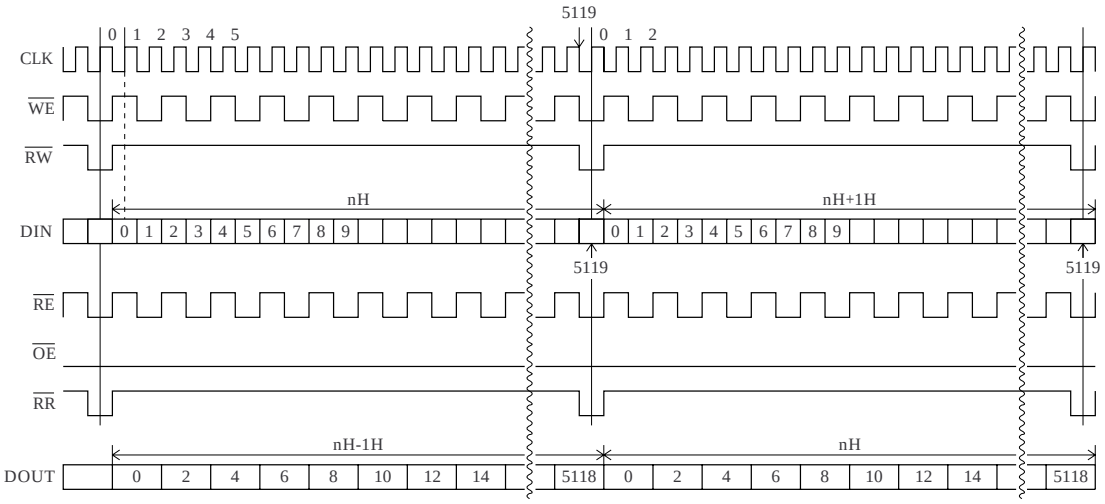
*Output data 867 to 909 forms the preceding 1H data.

1/2 Data Reduction

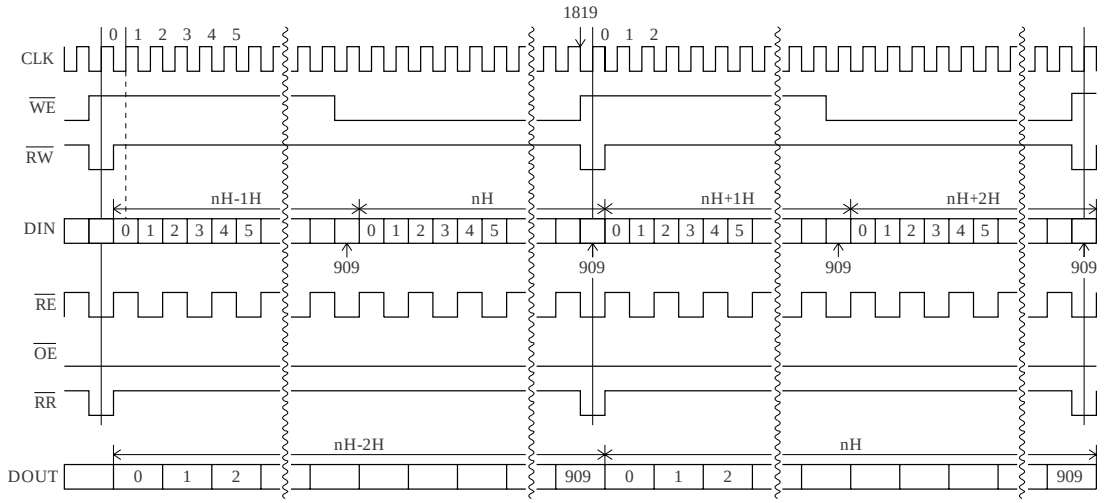
Input data rate reduction by half can be realized by taking $\overline{WE}$ and $\overline{RE}$ simultaneously HIGH only once every two clock cycles.

Noninterlace-to-interlace conversions line extraction can be realized by switching $\overline{WE}$ LOW/HIGH in line units and $\overline{RE}$ LOW/HIGH in word units.

1/2 data reduction



1/2 line extraction (noninterlace-to-interlace conversion)

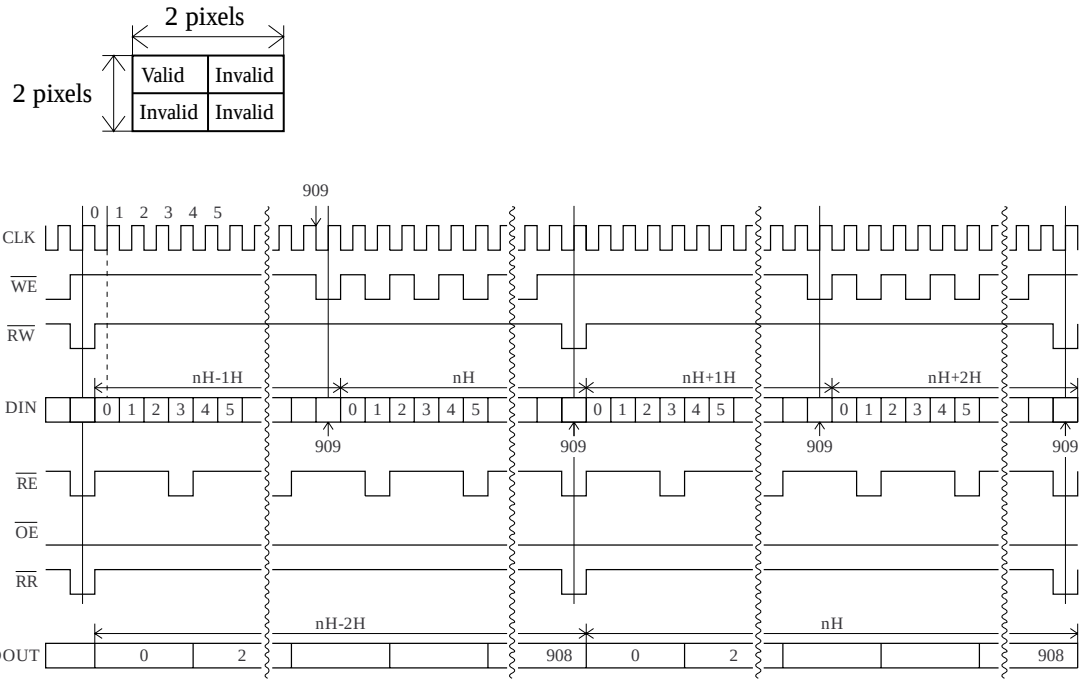


1/2n data reduction (n × n pixel reduction)

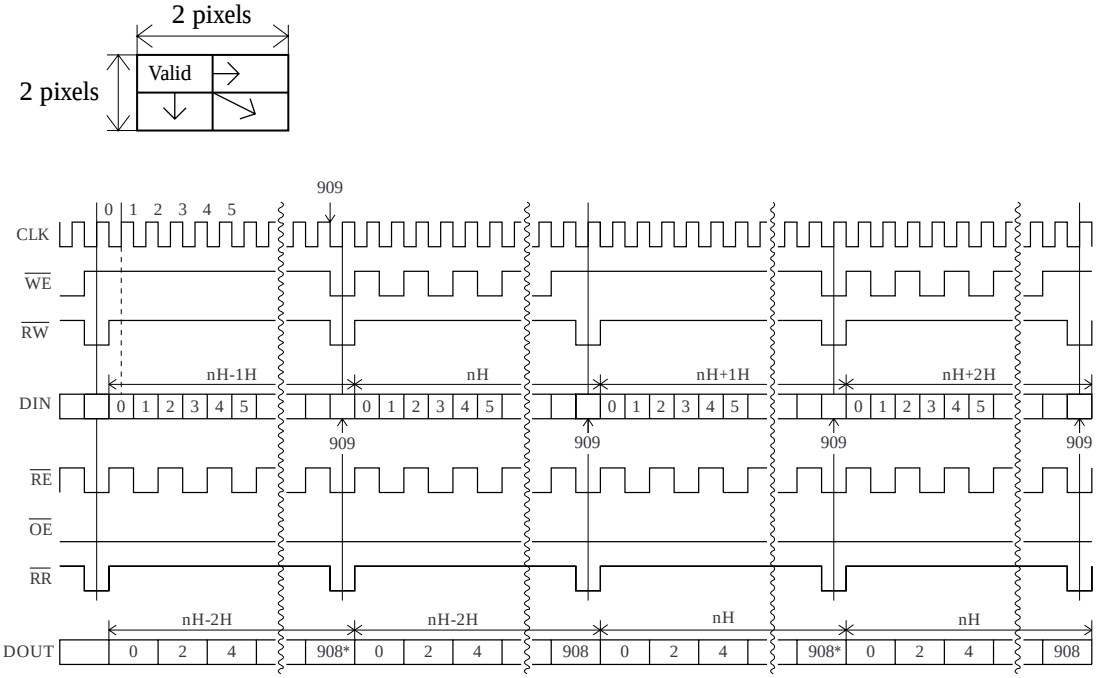
Screen resolution reduction, or 2 × 2 pixel reduction, can be realized by combining both 1/2 data reduction and 1/2 line extraction schemes. Furthermore, n × n pixel reduction (for integer n) can be realized by changing the $\overline{WE}$ and $\overline{RE}$ disable intervals and the $\overline{RW}$ and $\overline{RR}$ reset timing.

Also, if the same data is repeatedly read out in place of other data that has been discarded, the screen resolution can be reduced without changing the data rate to realize a mosaic filter function.

2 × 2 pixel reduction (1/4 reduction)



2 × 2 pixel reduction (mosaic)

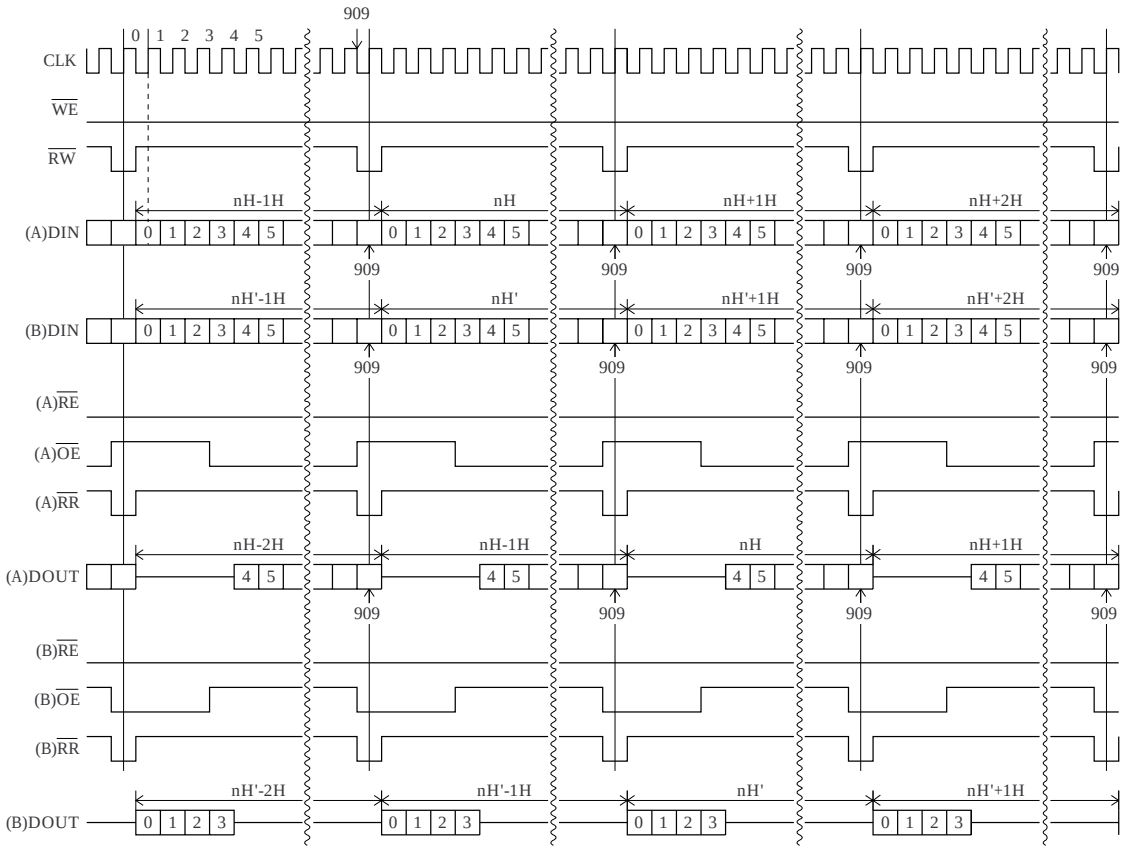


*Output date 902 to 908 forms the preceding 1H data.

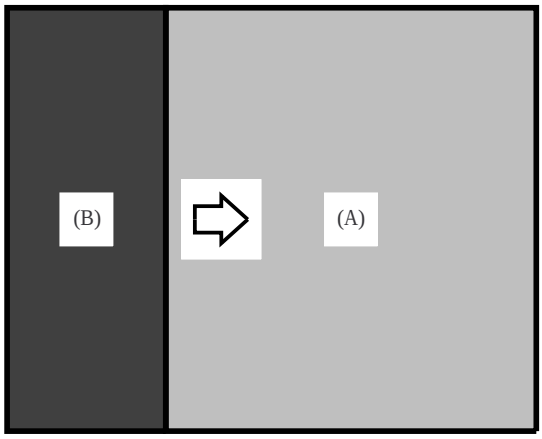
Wipe Function (Screen Switching)

Because $\overline{RE}$ and $\overline{OE}$ operate independently, a screen wipe function can be realized using 2 SM5838AS devices by switching $\overline{OE}$ LOW/HIGH in field units.

Screen wipe ($\overline{OE}$ changes in field units)



Screen wipe image (left to right)



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