NIPPON PRECISION CIRCUITS LTD.

SM5844AF

Asynchronous Sample Rate Converter

OVERVIEW

The SM5844AF is a digital audio signal, asynchronous sample rate converter LSI. It reads 16 or 20-bit word length input data, and writes 16, 18, or 20-bit word length output data. It also features a built-in digital deemphasis filter and digital attenuator.

The SM5844AF operates from a 5 V supply, and is available in 44-pin QFPs.

FEATURES

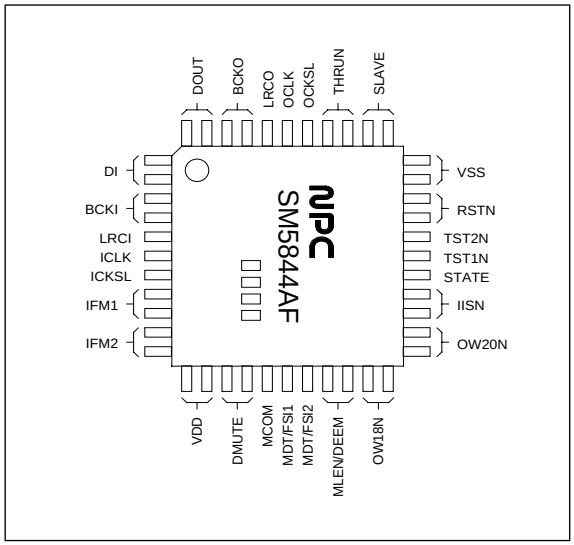
Functions

- Left/right-channel processing (stereo)
- Input sample rate (fsi) ranges
  - 24 to 48 kHz (256fsi mode)
  - 27 to 55 kHz (384fsi mode)
- Output sample rate (fso) range
  - 20 to 100 kHz
- Sample rate conversion ratio (fso/fsi)
  - 0.5 to 2.0 times
- Asynchronous input and output timing (clock inputs)
- System clock inputs (input and output clocks independent)
  - 256fsi or 384fsi input system clock
  - 256fso or 384fso output system clock
- Deemphasis filter
  - IIR-type filter
  - 44.1, 48 or 32 kHz
- Digital attenuator
  - 11-bit data for 1025 levels
  - Smooth, incremental attenuation change
  - +12 dB gain shift function
- Direct mute function
- Through mode operation
  - Input to output direct
- Output data clocks (LRCO, BCKO)
  - External input (slave mode)
  - Output system clock generated internally (master mode)
- CMOS-level input/outputs
- 5 V (standard) single supply
- 44-pin QFP
- Molybdenum-gate CMOS process

APPLICATIONS

- Digital audio equipment, sample rate conversion (audiovisual amplifiers, CD-R, DAT, MD and 8 mm VTRs)
- Commercial recording/editing equipment, sample rate conversion
- Input data jitter elimination

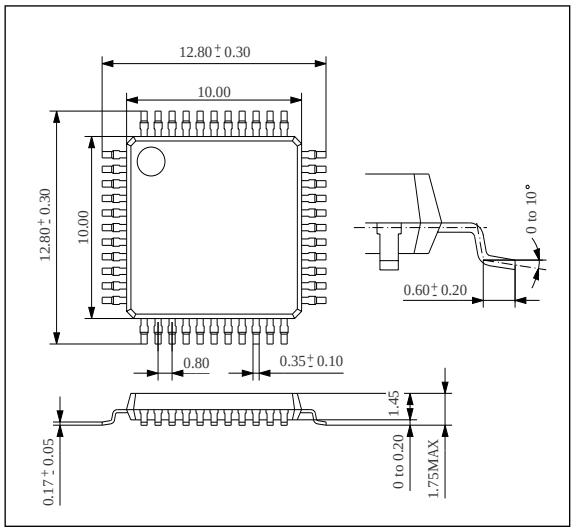
PINOUT



PACKAGE DIMENSIONS

Unit: mm

44-pin QFP



Filter Characteristics and Converter Efficiency

- 20-bit internal data word length
- Deemphasis filter characteristics (IIR filter)
  - ±0.03 dB gain deviation from ideal filter characteristics
- Converter noise levels
  - ≤ −110 dB internally-generated noise
  - −98 dB (16-bit output), −110 dB (18-bit output) and −122 dB (20-bit output) word rounding noise
- Anti-aliasing LPF characteristics (4 FIR filters) with automatic output/input sample rate conversion ratio selection
  - Up converter LPF (1.0 to 2.0 times)
  - Down converter LPF 1 (48.0 to 44.1 kHz or 0.92 times)
  - Down converter LPF 2 (44.1 to 32.0 kHz or 0.73 times)
  - Down converter LPF 3 (48.0 to 32.0 kHz or 0.67 times)
- Output S/N ratio (theoretical values)

Output signal word length	S/N ratio	
	16-bit input word length	20-bit input word length
16 bits	94.8 dB	97 dB
18 bits	97.5 dB	106 dB
20 bits	97.7 dB	109 dB

Interfaces

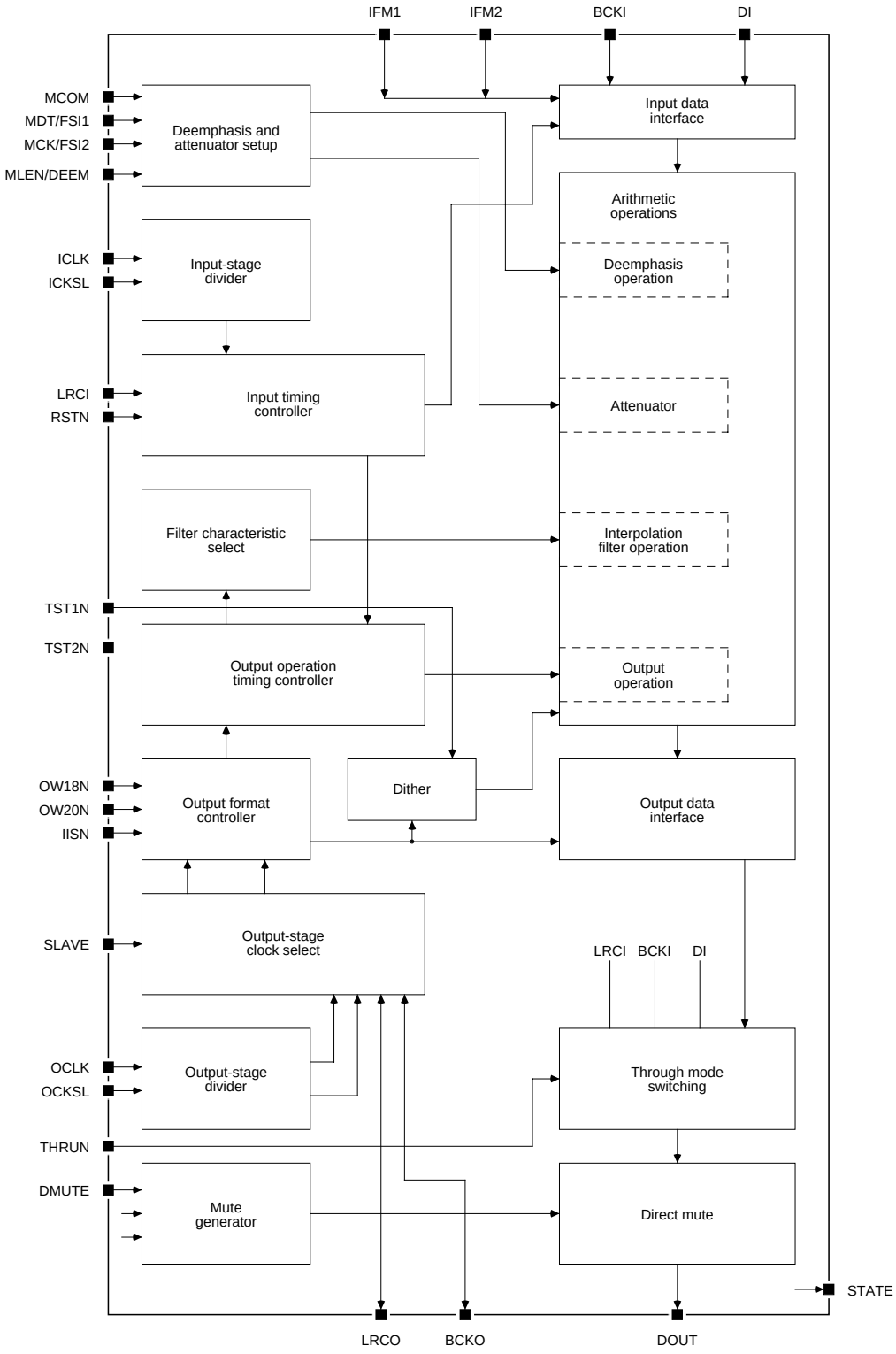
- Input data format
  - 2s-complement, L/R alternating, serial
  - Normal format (non IIS)

Mode	Word length	Front/rear packing	Data sequence
1	16 bits	Rear	MSB first
2	20 bits		
3		Front	
4		Rear	LSB first

- Output data format
  - 2s-complement, MSB first, L/R alternating, serial
  - Continuous bit clock

Mode	Word length	IIS selection	Front/rear packing
1	16 bits	Normal (non IIS)	Rear
2	18 bits		
3	20 bits		
4	20 bits		Front
5	16 bits	IIS	
6	18 bits		
7	20 bits		

BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Number[1]</th><th>Name</th><th>I/O[2]</th><th>Description</th></tr>
<tr><td>1, 2</td><td>DI</td><td>Ip</td><td>Data input</td></tr>
<tr><td>3, 4</td><td>BCKI</td><td>Ip</td><td>Input bit clock</td></tr>
<tr><td>5</td><td>LRCI[3]</td><td>Ip</td><td>Input word clock (fsi)</td></tr>
<tr><td>6</td><td>ICLK</td><td>I</td><td>Input system clock input</td></tr>
<tr><td>7</td><td>ICKSL</td><td>Ip</td><td>Input system clock (ICLK) select. 384fsi when HIGH, and 256fsi when LOW.</td></tr>
<tr><td>8, 9</td><td>IFM1</td><td>Ip</td><td rowspan="2">Input format select
<table>
<tr><th>IFM1</th><th>IFM2</th><th>Word length</th><th>Data sequence</th><th>Data position</th></tr>
<tr><td>LOW</td><td>LOW</td><td>16 bits</td><td rowspan="3">MSB first</td><td rowspan="2">Rear packed</td></tr>
<tr><td>LOW</td><td>HIGH</td><td rowspan="3">20 bits</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>Front packed</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>LSB first</td><td>Rear packed</td></tr>
</table></td></tr>
<tr><td>10, 11</td><td>IFM2</td><td>Ip</td></tr>
<tr><td>12, 13</td><td>VDD</td><td>–</td><td>5 V supply pin</td></tr>
<tr><td>14, 15</td><td>DMUTE</td><td>Ip</td><td>Direct mute pin</td></tr>
<tr><td>16</td><td>MCOM</td><td>Ip</td><td>Interface switch control pin. MDT, MCK and MLEN control when HIGH. FSI1, FSI2 and DEEM control when LOW.</td></tr>
<tr><td>17</td><td>MDT/FSI1</td><td>Ip</td><td>When MCOM is HIGH: Microcontroller interface data input (MDT)</td><td rowspan="2">When MCOM is LOW: Deemphasis frequency set pins
<table>
<tr><th>FSI1</th><th>FSI2</th><th>fsi</th></tr>
<tr><td>LOW</td><td>HIGH</td><td>48.0 kHz</td></tr>
<tr><td>×</td><td>LOW</td><td>44.1 kHz</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>32.0 kHz</td></tr>
</table></td></tr>
<tr><td>18</td><td>MCK/FSI2</td><td>Ip</td><td>When MCOM is HIGH: Microcontroller interface bit clock (MCK)</td></tr>
<tr><td>19, 20</td><td>MLEN/DEEM</td><td>Ip</td><td colspan="2">When MCOM is HIGH: Microcontroller data word latch clock (MLEN)
When MCOM is LOW: Deemphasis ON/OFF control (DEEM)</td></tr>
<tr><td>21, 22</td><td>OW18N</td><td>Ip</td><td colspan="2">Output format select
When IISN = HIGH (normal mode)
<table>
<tr><th>OW20N</th><th>OW18N</th><th>Word length</th><th>Data position</th></tr>
<tr><td>LOW</td><td>LOW</td><td rowspan="2">20 bits</td><td>Front packed</td></tr>
<tr><td>LOW</td><td>HIGH</td><td rowspan="3">Rear packed</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>18 bits</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>16 bits</td></tr>
</table></td></tr>
<tr><td>23, 24</td><td>OW20N</td><td>Ip</td><td colspan="2">When IISN = LOW (IIS mode)
<table>
<tr><th>OW20N</th><th>OW18N</th><th>Word length</th><th>Data position</th></tr>
<tr><td>LOW</td><td>LOW</td><td rowspan="2">20 bits</td><td rowspan="3">IIS mode
Front packed</td></tr>
<tr><td>LOW</td><td>HIGH</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>18 bits</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>16 bits</td></tr>
</table></td></tr>
<tr><td>25, 26</td><td>IISN</td><td>Ip</td><td colspan="2">IIS output mode select. Normal mode when HIGH, and IIS mode when LOW.</td></tr>
<tr><td>27</td><td>STATE</td><td>O</td><td colspan="2">Internal operation status output (for operation check)</td></tr>
<tr><td>28</td><td>TST1N</td><td>Ip</td><td colspan="2">Output dither control. Dither ON when LOW, and OFF when HIGH.</td></tr>
<tr><td>29</td><td>TST2N</td><td>Ip</td><td colspan="2">Test pin. Test mode when LOW. Normal operating mode when HIGH.</td></tr>
</table>

Number[1]	Name	I/O[2]	Description
30, 31	RSTN	Ip	Reset pin
32, 33	VSS	–	0 V ground pin
34, 35	SLAVE	Ip	BCKO and LRCO mode set. Outputs (master mode) when LOW, and inputs (slave mode) when HIGH.
36, 37	THRUN	Ip	DOUT through mode set. Normal mode when HIGH, and through mode when LOW.
38	OCKSL	Ip	Output system clock (OCLK) select. 384fso when HIGH, and 256fso when LOW.
39	OCLK	I	Output system clock input
40	LRCO[3]	I/O	Output word clock input/output (fso). Input/output mode set by the level on SLAVE.
41, 42	BCKO	I/O	Output bit clock input/output. Input/output mode set by the level on SLAVE.
43, 44	DOUT	O	Data output

1. Pins which have the same name are connected internally. Accordingly, circuit connections can be made to either pin or to both pins.
2. I = input, Ip = Input with pull-up resistor (HIGH-level pins can be left open), O = output, I/O = input/output
3. fsi is the input word clock (LRCI) frequency, and fso is the output word clock (LRCO) frequency.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	550	m W
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.75 to 5.5	V
Operating temperature range	T_{opr}	–20 to 70	°C

DC Electrical Characteristics

V_{DD} = 4.75 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 5.0 V[1]	–	–	80	mA
HIGH-level input voltage[2,3]	V_{IH}		0.7V_{DD}	–	–	V
LOW-level input voltage[2,3]	V_{IL}		–	–	0.3V_{DD}	V
AC-coupled input voltage[2]	V_{ACI}		0.3V_{DD}	–	–	V_{p-p}
HIGH-level output voltage[4]	V_{OH}	I_{OH} = –1.0 mA	V_{DD} – 0.5	–	–	V
LOW-level output voltage[4]	V_{OL}	I_{OL} = 1.0 mA	–	–	0.4	V
HIGH-level input current[2]	I_{IH}	V_{IN} = V_{DD}	–	10	20	µA
LOW-level input current[2,3]	I_{IL}	V_{IN} = 0 V	–	10	20	µA
Input leakage current[3]	I_{LH}	V_{IN} = V_{DD}	–	–	1.0	µA
Pull-up resistance[3]	R_{IH}		250	500	1000	kΩ

1. ICKSL = LOW, OCKSL = LOW, f_{ICLK} = 13.0 MHz, f_{OCLK} = 13.0 MHz, no output load
2. Pins ICLK and OCLK.
3. Pins DI, BCKI, LRCI, ICKSL, IFM1, IFM2, DMUTE, MCOM, MDT/FSI1, MCK/FSI2, MLEN/DEEM, OW18N, OW20N, IISN, TST1N, TST2N, RSTN, THRUN, OCKSL and SLAVE.
4. Pins DOUT, BCKO, LRCO and STATE.

AC Electrical Characteristics

V_{DD} = 4.75 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

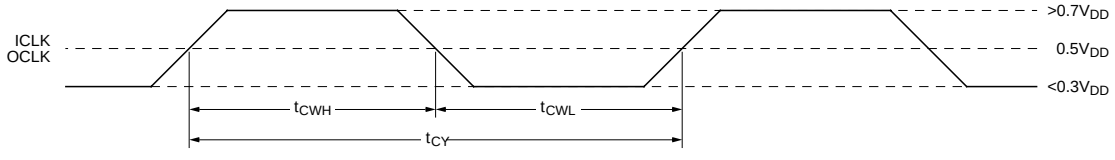
ICLK input

Parameter	Symbol	Condition		Rating			Unit
		ICKSL	System clock	min	typ	max	
LOW-level clock pulsewidth	t_{CWL}	LOW	256fsi	30	–	–	ns
		HIGH	384fsi	10	–	–	
HIGH-level clock pulsewidth	t_{CWH}	LOW	256fsi	30	–	–	ns
		HIGH	384fsi	10	–	–	
Clock pulse cycle	t_{CY}	LOW	256fsi	80	–	162	ns
		HIGH	384fsi	47	–	106	

OCLK input

Parameter	Symbol	Condition		Rating			Unit
		OCKSL	System clock	min	typ	max	
LOW-level clock pulsewidth	t_{CWL}	LOW	256fso	15	–	–	ns
		HIGH	384fso	10	–	–	
HIGH-level clock pulsewidth	t_{CWH}	LOW	256fso	15	–	–	ns
		HIGH	384fso	10	–	–	
Clock pulse cycle	t_{CY}	LOW	256fso	39	–	200	ns
		HIGH	384fso	26	–	130	

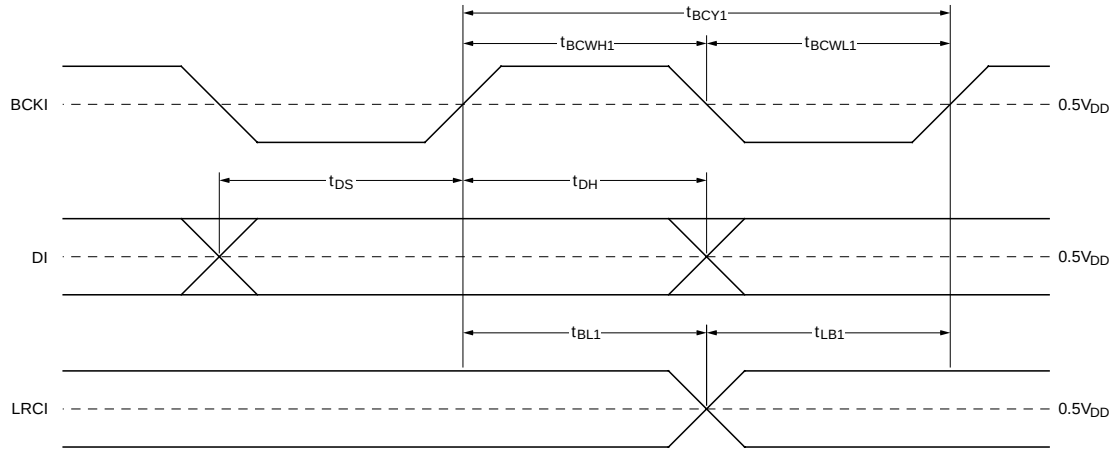
ICLK and OCLK timing



BCKI, DI, LRCI inputs

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI LOW-level pulsewidth	t_{BCWL1}	50	–	–	ns
BCKI HIGH-level pulsewidth	t_{BCWH1}	50	–	–	ns
BCKI pulse cycle	t_{BCY1}	100	–	–	ns
DI setup time	t_{DS}	50	–	–	ns
DI hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL1}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB1}	50	–	–	ns

BCKI, DI, LRCI timing

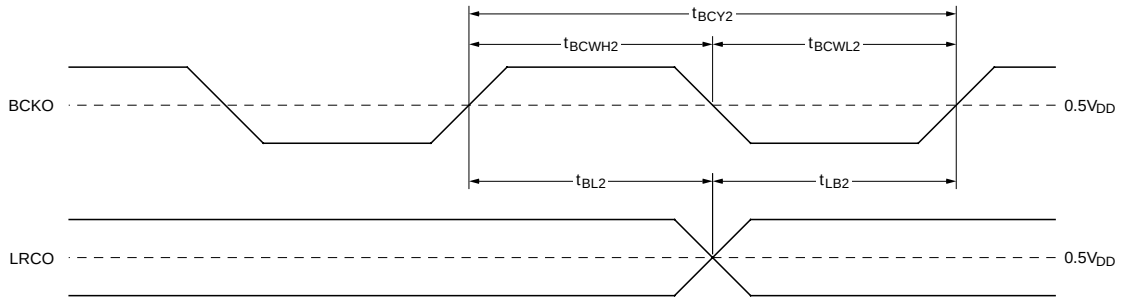


BCKO, LRCO (Inputs when SLAVE = HIGH)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKO LOW-level pulsewidth	t_{BCWL2}	78	–	–	ns
BCKO HIGH-level pulsewidth	t_{BCWH2}	78	–	–	ns
BCKO pulse cycle[1]	t_{BCY2}	156	–	–	ns
Last BCKO rising edge to LRCO edge	t_{BL2}	78	–	–	ns
LRCO edge to first BCKO rising edge	t_{LB2}	78	–	–	ns

1. BCKO clock inputs exceeding 64fso cannot be detected, and will cause incorrect operation.

BCKO, LRCO timing

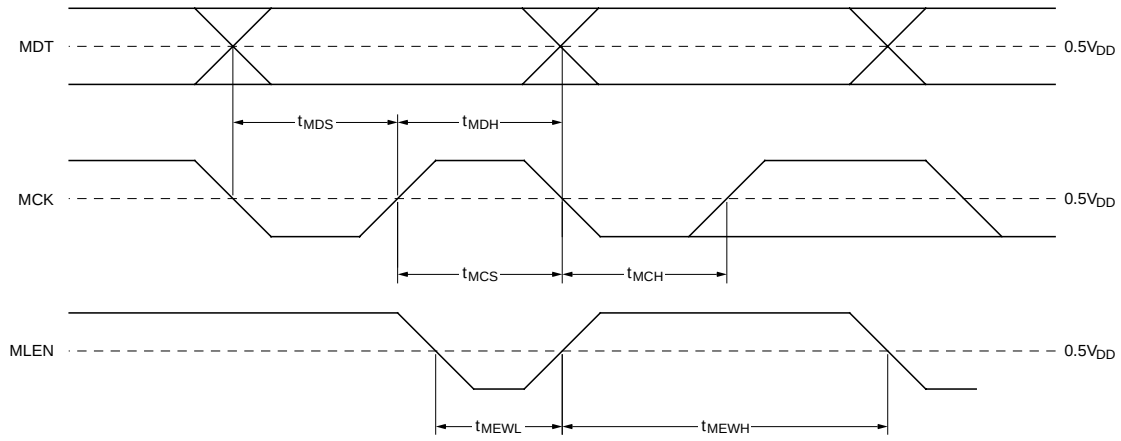


MDT, MCK, MLEN inputs

Parameter	Symbol	Rating			Unit
		min	typ	max	
MCK and MLEN rise time[1]	t_r	–	–	100	ns
MCK and MLEN fall time[1]	t_f	–	–	100	ns
MDT setup time	t_{MDS}	50	–	–	ns
MDT hold time	t_{MDH}	50	–	–	ns
MLEN setup time	t_{MCS}	50	–	–	ns
MLEN hold time	t_{MCH}	50	–	–	ns
MLEN LOW-level pulsewidth	t_{MEWL}	50	–	–	ns
MLEN HIGH-level pulsewidth	t_{MEWH}	50	–	–	ns

1. t_r and t_f are the input waveform transition times measured between $0.1V_{DD}$ and $0.9V_{DD}$ levels.

MDT, MCK, MLEN timing



DEEM, DMUTE inputs

Parameter	Symbol	Rating			Unit
		min	typ	max	
Rise time	t_r	–	–	100	ns
Fall time	t_f	–	–	100	ns

DOUT, BCKO, LRCO input/outputs

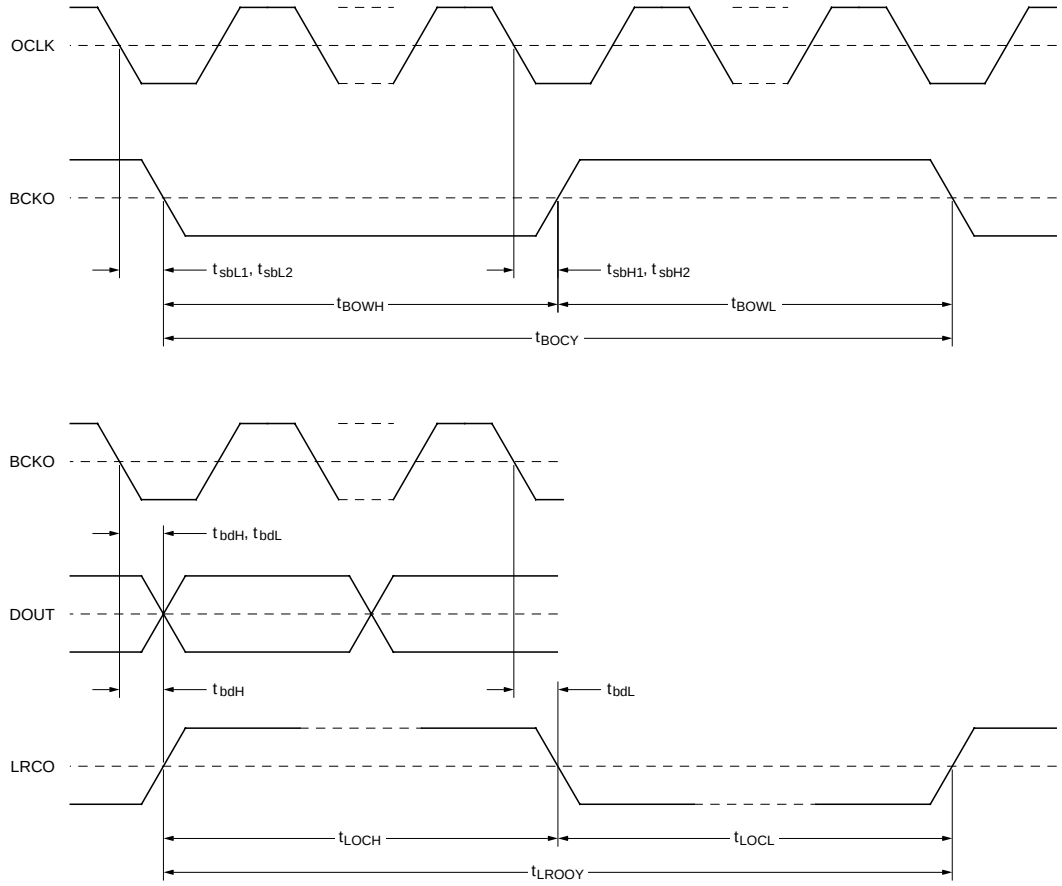
SLAVE = LOW (outputs), C_L = 15 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LRCO pulse cycle	t_{LOCY}		–	1/fso	–	ns
LRCO LOW-level pulsewidth	t_{LOCL}		–	1/2fso	–	ns
LRCO HIGH-level pulsewidth	t_{LOCH}		–	1/2fso	–	ns
BCKO pulse cycle	t_{BOCY}	OCKSL = LOW	–	1/64fso	–	ns
		OCKSL = HIGH	–	1/48fso	–	
BCKO LOW-level pulsewidth	t_{BOWL}	OCKSL = LOW	–	1/128fso	–	ns
		OCKSL = HIGH	–	1/96fso	–	
BCKO HIGH-level pulsewidth	t_{BOWH}	OCKSL = LOW	–	1/128fso	–	ns
		OCKSL = HIGH	–	1/96fso	–	
OCLK to BCKO delay time (OCKSL = LOW)	t_{sbH1}	From OCLK fall to BCKO rise	10	–	70	ns
	t_{sbL1}	From OCLK fall to BCKO fall	10	–	70	ns
OCLK to BCKO delay time (OCKSL = HIGH)	t_{sbH2}	From OCLK fall to BCKO rise	15	–	80	ns
	t_{sbL2}	From OCLK fall to BCKO fall	15	–	80	ns
BCKO to DOUT and LRCO delay time	t_{bdH1}	From BCKO fall to DOUT rise	0	–	20	ns
	t_{bdL1}	From BCKO fall to DOUT fall	0	–	20	ns

SLAVE = HIGH (inputs), C_L = 15 pF

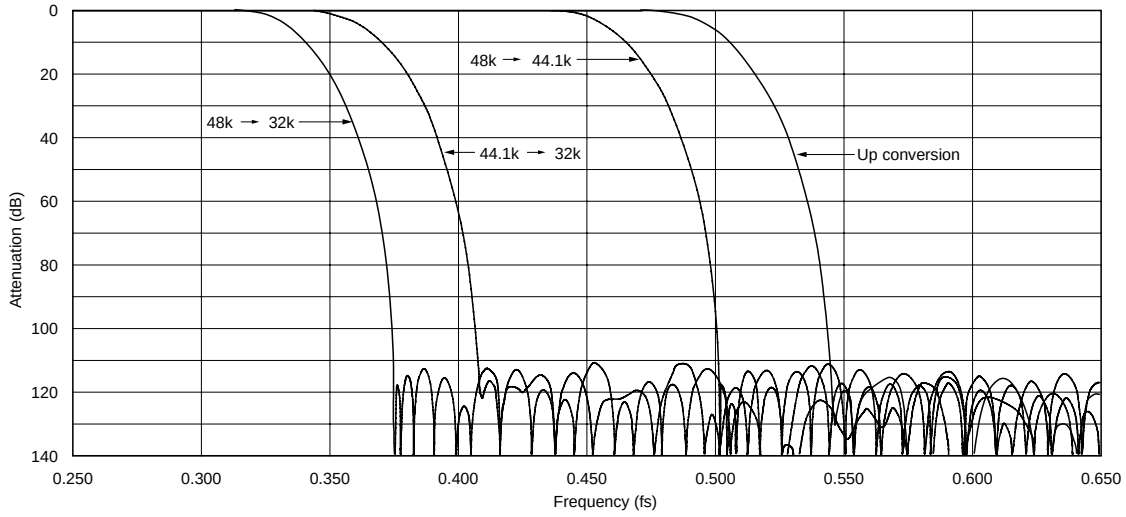
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKO to DOUT delay time	t_{bdH2}	From BCKO fall to DOUT rise	10	–	100	ns
	t_{bdL2}	From BCKO fall to DOUT fall	10	–	100	ns

DOUT, BCKO, LRCO timing

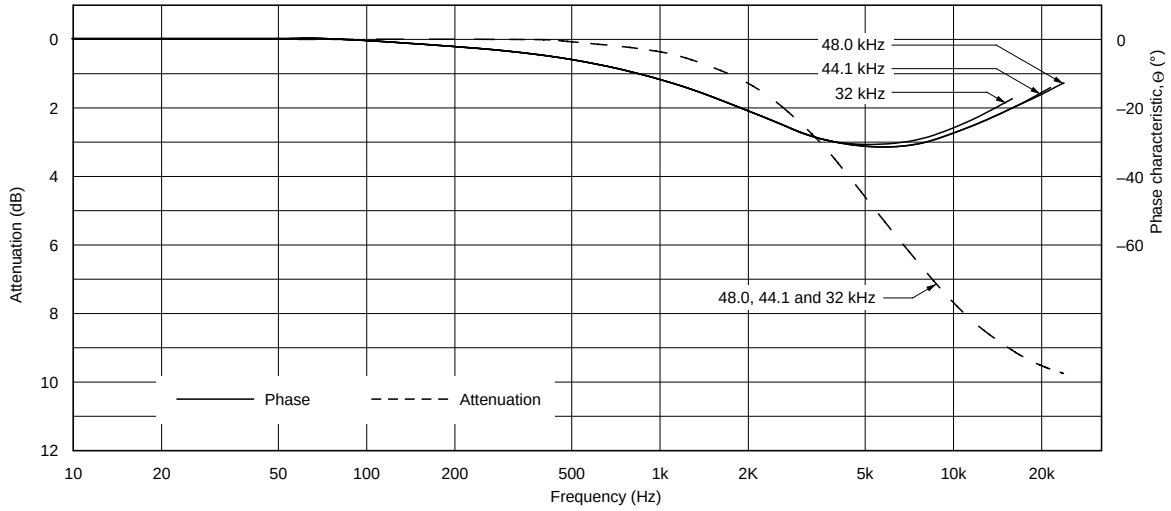


Filter Characteristics

Anti-aliasing filter frequency characteristic



Deemphasis filter frequency characteristic



FUNCTIONAL DESCRIPTION

Input Data Interface (DI, LRCI, BCKI, IFM1, IFM2)

Mode	IFM1	IFM2	Word length	Data position	Data sequence	Common features
1	LOW	LOW	16 bits	Rear packed	MSB first	Non IIS L/R alternating Bit serial
2	LOW	HIGH	20 bits			
3	HIGH	LOW		Front packed		
4	HIGH	HIGH		Rear packed	LSB first	

Attenuator and Deemphasis Selection

The attenuator is set using the microcontroller interface. When the attenuator is used, deemphasis settings also need to be set using the microcontroller interface. The microcontroller interface comprises MDT, MCK and MLEN, and is used to receive all input serial data.

Table 1. Attenuator and deemphasis function selection

Function	Function set method	
	External pins (MCOM = LOW)	Microcontroller interface flags (MCOM = HIGH)
Deemphasis ON/OFF	DEEM	FDEEM
Deemphasis frequency (fsi) select	FSI1, FSI2	FFSI1, FFSI2
Attenuator data set	N/A (no attenuation)	11 bits (a1 to a11)
Test mode select	Irreversible (test mode 1)	FTST1, FTST2

When MCOM is HIGH, serial data received on MDT, MCK and MLEN sets the attenuation data and control flag data.

When MCOM is LOW, the logic levels on FSI1, FSI2 and DEEM select the device function.

Microcontroller Interface (MCOM, MDT, MCK, MLEN)

When MCOM is HIGH, MDT (data), MCK (clock) and MLEN (latch enable clock) interface pins are used.

Input data on MDT is synchronized to the MCK clock. Data is read into the input stage shift register on the rising edge of MCK. Accordingly, the input data should change on the falling edge of MCK. Input data enters an internal SIPO (serial-to-parallel converter register), and then the parallel data is latched into the mode register on the rising edge of the latch enable clock MLEN.

The mode register addressed is determined by the 1st bit of the 12 data bits before MLEN goes HIGH. If this bit is LOW, then the data is read into the attenuation data register as shown in figure 1. If this bit is HIGH, then the data is read into the mode flag register as shown in figure 2. The function of each bit in the mode flag register is described in table 1.

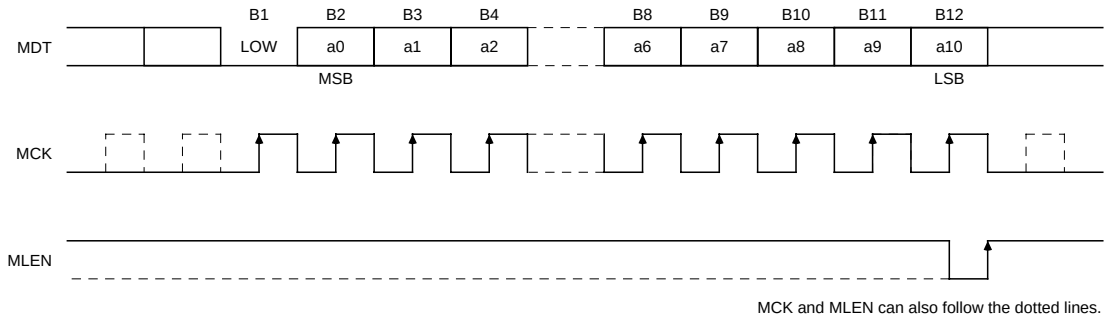


Figure 1. Attenuation data format (B1 = LOW)

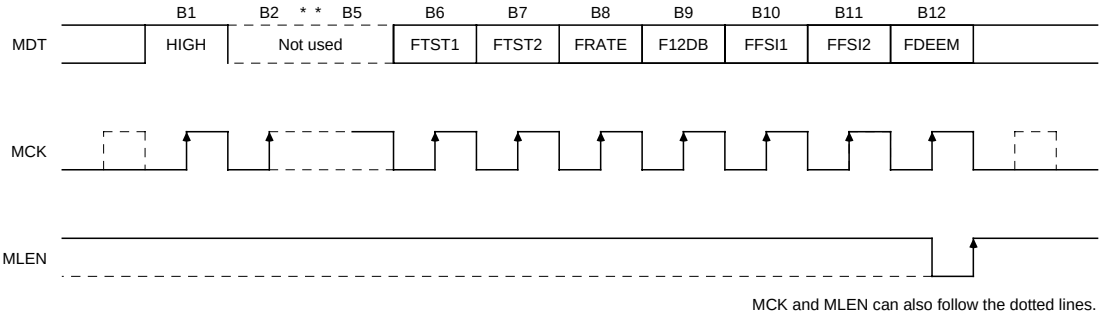


Figure 2. Mode flag data format (B1 = HIGH)

Table 2. Mode flag description

<table>
<tr><th rowspan="2">B1</th><th rowspan="2">Bit</th><th rowspan="2">Mode flag</th><th colspan="3">Mode function select</th><th rowspan="2">Reset mode</th></tr>
<tr><th>Parameter</th><th>LOW/HIGH</th><th>Select</th></tr>
<tr><td rowspan="11">HIGH</td><td>B2 to B5</td><td></td><td>Not used</td><td></td><td></td><td></td></tr>
<tr><td>B6</td><td>FTST1</td><td>Test mode select 1</td><td></td><td rowspan="5">TST2N = LOW
<table><tr><th>FTST2</th><th>FTST1</th><th>Mode</th></tr><tr><td>LOW</td><td>LOW</td><td>0</td></tr><tr><td>LOW</td><td>HIGH</td><td>1</td></tr><tr><td>HIGH</td><td>LOW</td><td>2</td></tr><tr><td>HIGH</td><td>HIGH</td><td>3</td></tr></table></td><td>LOW</td></tr>
<tr><td>B7</td><td>FTST2</td><td>Test mode select 2</td><td></td><td>LOW</td></tr>
<tr><td rowspan="2">B8</td><td rowspan="2">FRATE</td><td rowspan="2">Input/output rate</td><td>LOW</td><td>Input/output sample rate ratio check after every output</td><td rowspan="2">LOW</td></tr>
<tr><td>HIGH</td><td>Input/output sample rate ratio check for high accuracy after every 2048 outputs</td></tr>
<tr><td rowspan="2">B9</td><td rowspan="2">F12DB</td><td rowspan="2">Attenuator</td><td>LOW</td><td>Normal operation (no shift)</td><td rowspan="2">LOW</td></tr>
<tr><td>HIGH</td><td>+12 dB gain shift</td></tr>
<tr><td>B10</td><td>FFSI1</td><td>Deemphasis filter fs select 1</td><td></td><td rowspan="5"><table><tr><th>FFSI2</th><th>FFSI1</th><th>fsi</th></tr><tr><td>LOW</td><td>LOW</td><td rowspan="2">44.1 kHz</td></tr><tr><td>LOW</td><td>HIGH</td></tr><tr><td>HIGH</td><td>LOW</td><td>48.0 kHz</td></tr><tr><td>HIGH</td><td>HIGH</td><td>32.0 kHz</td></tr></table></td><td>LOW</td></tr>
<tr><td>B11</td><td>FFSI2</td><td>Deemphasis filter fs select 2</td><td></td><td>LOW</td></tr>
<tr><td rowspan="2">B12</td><td rowspan="2">FDEEM</td><td rowspan="2">Deemphasis control ON/OFF</td><td>LOW</td><td>Deemphasis filter OFF</td><td rowspan="2">LOW</td></tr>
<tr><td>HIGH</td><td>Deemphasis filter ON</td></tr>
</table>

Deemphasis (DEEM, FSI1, FSI2 pins or FDEEM, FFSI1, FFSI2 flags)

The digital deemphasis filter is an IIR filter with variable coefficients to faithfully reproduce the gain and phase characteristics of standard analog deemphasis filters.

The filter coefficients are selected by FSI1 (or FFSI1 flag) and FSI2 (or FFSI2 flag) to correspond to the sampling frequencies fs = 44.1, 48.0 and 32.0 kHz.

Table 3. Deemphasis ON/OFF

When MCOM = LOW	When MCOM = HIGH	Deemphasis
DEEM = HIGH	FDEEM = HIGH	ON
DEEM = LOW	FDEEM = LOW	OFF

Table 4. Deemphasis fs select (FSI1, FSI2 pins or FFSI1, FFSI2 flags)

MCOM = LOW (MCOM = HIGH)		fs
FSI1 (FFSI1)	FSI2 (FFSI2)	
LOW	LOW	44.1 kHz
HIGH	LOW	
LOW	HIGH	48.0 kHz
HIGH	HIGH	32.0 kHz

Attenuation (MDT, MCK, MLEN)

The digital attenuator coefficients are read in as serial data on the microcontroller interface. Data on MDT is read into the internal shift register on the rising edge of MCK, and then 12 bits are latched internally on the rising edge of MLEN.

When the leading bit is 0 (B1 = LOW), the following 11 bits are read into the attenuation register and used as an unsigned integer in MSB first format. See figure 3.

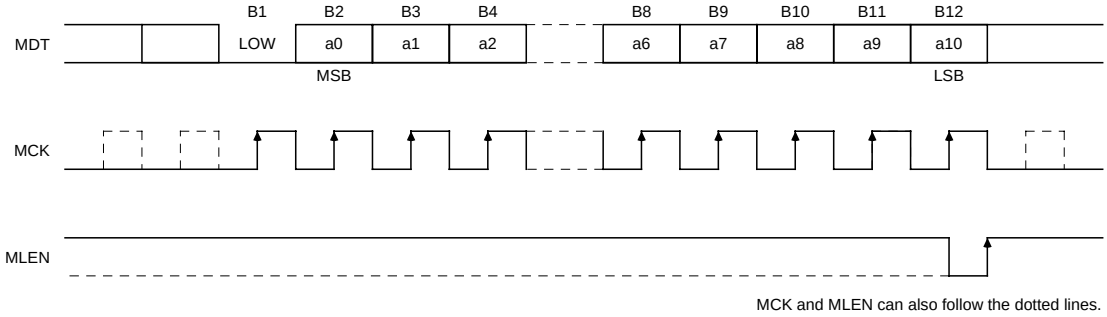


Figure 3. Attenuation data format (microcontroller interface)

Although the attenuation data comprises 11 bits, only 1025 levels are valid as given by the following.

$$\text{DATT} = \sum_{i=0}^{10} a_i \times 2^{(10-i)}$$

The gain of the attenuator for values of DATT from 001H to 400H are given by the following equations. Note that when the F12DB flag is HIGH, the gain is shifted by +12.0412 dB.

$$\text{Gain} = 20 \times \log\left(\frac{\text{DATT}}{1024}\right)[\text{dB}]$$

when F12DB = LOW

$$= 20 \times \log\left(\frac{\text{DATT}}{256}\right)[\text{dB}]$$

when F12DB = HIGH

After a system reset initialization, DATT is set to 400H and the F12DB flag is LOW, corresponding to 0 dB gain. (The F12DB flag is described in table 2.)

Table 5. Attenuator settings

Attenuation data DATT	F12DB = LOW (default)		F12DB = HIGH	
	Gain (dB)	Linear expression	Gain (dB)	Linear expression
000H	–∞	0.0	–∞	0.0
001H	–60.206	1/1024	–48.165	1/256
↓	↓	↓	↓	↓
100H	–12.041	256/1024	0.0	256/256
↓	↓	↓	↓	↓
3FFH	–0.0085	1023/1024	12.032	1023/256
400H (to 7FFH)	0	1.0	12.041	4.0

Attenuator operation

A change in the attenuation data DATT causes the gain to change smoothly from its previous value towards the new setting. The new attenuation data is stored in the attenuation data register and the current attenuation level is stored in a temporary register. Consequently, if a new attenuation level is read in before the previously set level is reached, the gain changes smoothly from the current value towards the latest setting as shown in figure 4.

The attenuation counter output changes, and hence the gain changes, by 1 step every output sample. The time taken to reduce the gain from 0 dB (or 12 dB) to −∞ dB is (1024/fso), which corresponds to approximately 23.2 ms when fso = 44.1 kHz.

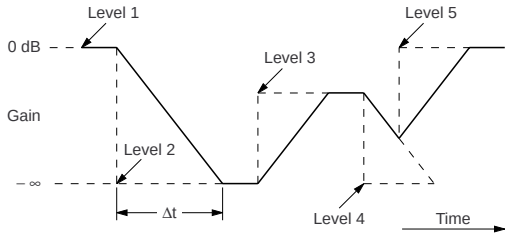


Figure 4. Attenuator operation example

Direct Mute (DMUTE)

Direct mute ON/OFF

Table 6. DMUTE operation

DMUTE	Function
LOW	Normal data is output from the next output word (mute OFF)
HIGH	0 data is output from the next output word (mute ON)

Reset mute

Table 7. RSTN mute operation

RSTN	Function
LOW	0 data is output from the next output word (mute ON)
HIGH	Normal data is output from the 3073rd output word (mute OFF)

Internal operating status (STATE)

Internally, all functions are performed using 20-bit serial data, and the conversion rate and filter type are automatically selected for output. Output data is in 20-bit front-packed format.

Table 8. Bit function

<table>
<tr><th>Output bit position</th><th colspan="2">Content</th></tr>
<tr><td>1st to 18th</td><td colspan="2">(Output data cycle/input data cycle) – 9
Ex.
1st 18th
00.111111111110111 ⇒ 1.0 times
01.111111111110111 ⇒ 2.0 times (1/2 conversion rate ratio)
00.011111111110111 ⇒ 0.5 times (2.0 conversion rate ratio)</td></tr>
<tr><td>19th</td><td>DA1</td><td rowspan="2">Selected filter type
<table><tr><th>DA1</th><th>DA0</th><th>Filter</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>Up converter</td><td>1</td></tr><tr><td>1</td><td>0</td><td>44.1 to 48 kHz</td><td>2</td></tr><tr><td>0</td><td>1</td><td>32 to 44.1 kHz</td><td>3</td></tr><tr><td>1</td><td>1</td><td>32 to 48 kHz</td><td>4</td></tr></table></td></tr>
<tr><td>20th</td><td>DA0</td></tr>
</table>

Note that when THRUN is LOW, LRCO and BCKO are not guaranteed to be synchronized to the STATE output.

System Clock

Input system clock (ICLK, ICKSL)

The input system clock can be set to run at either 256fsi or 384fsi, where fsi is the input frequency on LRCI.

Note that ICLK and LRCI should be divided from a common clock source or PLL to maintain synchronism.

Table 9. ICLK system clock

ICKSL	ICLK system clock rate
HIGH	384fsi
LOW	256fsi

Output system clock (OCLK, OCKSL)

The output system clock can be set to run at either 256fso or 384fso, where fso is the input frequency on LRCO. In through mode, OCLK and OCKSL have no function and are not used.

Note that in slave mode, a suitable clock must be input on OCLK. The clock on OCLK should ideally have a protection circuit to prevent incorrect operation for times when the clock on ICLK is halted.

Table 10. OCLK system clock

SLAVE	OCKSL	OCLK system clock rate
LOW	HIGH	384fso
	LOW	256fso
HIGH	×	Not used

Output data interface and output clock selection (LRCO, BCKO, DOUT, SLAVE)

Table 11. Output mode description

THRUN	SLAVE	Function		
		Mode	Description	LRCO, BCKO state
HIGH	LOW	Master mode	Output word clock (LRCO) and output bit clock (BCKO) are divided from OCLK.	Outputs
	HIGH	Slave mode	Output word clock (LRCO) and output bit clock (BCKO) are supplied externally.	Inputs[1]
LOW	×	Through mode	Output word clock (LRCO), output bit clock (BCKO) and output data (DOUT) are the same as LRCI, BCKI and DI, respectively.	Outputs

1. The number of BCKO input clock cycles should not exceed 64 per word. Correct operation is not guaranteed beyond these limits.

System Reset (RSTN)

At power-ON, all device functions must be reset. The device is reset by applying a LOW-level pulse on RSTN. At system reset, the internal arithmetic operation, output timing counter and internal flag register operation are synchronized on the next LRCI rising edge. Note that all flags are set to their defaults (all LOW).

A power-ON reset signal can be applied from an external microcontroller. For systems where ICLK and LRCI are stable at power ON, initialization can be performed by connecting a 0.001 µF capacitor between RSTN and VSS. Otherwise, a capacitor value should be chosen such that RSTN does not go HIGH until after LRCI and ICLK have stabilized.

Through Mode (THRUN)

Table 12. THRUN operation

THRUN	Mode	Description
LOW	Through mode	Direct connections are made: LRCI to LRCO, BCKI to BCKO, and DI to DOUT.
HIGH	Normal mode	Sample rate converter operation

Internal Arithmetic Timing Auto-reset

The clock on LRCI should pass through 1 cycle for every 384 (ICKSL = HIGH) or 256 (ICKSL = LOW) ICLK clock cycles to maintain correct internal arithmetic sequence. If the number of ICLK cycles is different, increases or decreases, or any jitter is present, device operation could be affected.

There is a fixed-value tolerance within which the internal sequence and LRCI clock timing are not adversely affected.

Table 13. Clock tolerance

ICKSL	Allowable clock variation
HIGH (384fs mode)	+8/–6 cycles
LOW (256fs mode)	+4/–3 cycles

Whenever the allowable tolerance is exceeded, the internal sequence is automatically reset so that the internal sequence matches the LRCI clock. When this occurs, there is a possibility that click noise will be generated.

Output Format Control (OW18N, OW20N, IISN)

The output is in MSB-first, 2s-complement, L/R alternating, bit serial format with a continuous bit clock.

Table 14. Output format selection

Mode	Inputs			Output format		
	IISN	OW20N	OW18N	Word length	IIS selection	Front/rear packing
1	HIGH	HIGH	HIGH	16 bits	Non IIS	Rear
2		HIGH	LOW	18 bits		
3		LOW	HIGH	20 bits		
4		LOW	LOW	20 bits		Front
5	LOW	HIGH	HIGH	16 bits	IIS	
6		HIGH	LOW	18 bits		
7		LOW	×	20 bits		

Output Timing Calculation

The output timing is calculated to maintain the desired ratio between the output data cycle and the input data cycle.

Filter Characteristic Selection

Conversion rates from 0.5 to 2.0 times are supported using the following 4 filter types.

The ratio between the output sample rate and input sample rate is measured automatically and the most suitable filter type for this ratio is selected automatically.

Table 15. fs ratio and filter selection

Mode	Filter	fs ratio (fso/fsi)	Selects range
1	Up converter	1.0 to 2.0	≥ 0.97
2	48.0 to 44.1 kHz	0.91875	0.865 to 0.97
3	44.1 to 32.0 kHz	0.72562	0.711 to 0.865
4	48.0 to 32.0 kHz	0.66667	≤ 0.711

When the selected fs conversion ratio and the actual sample rate conversion ratio do not coincide, the following phenomenon are generated.

Table 16. fs ratio mismatch

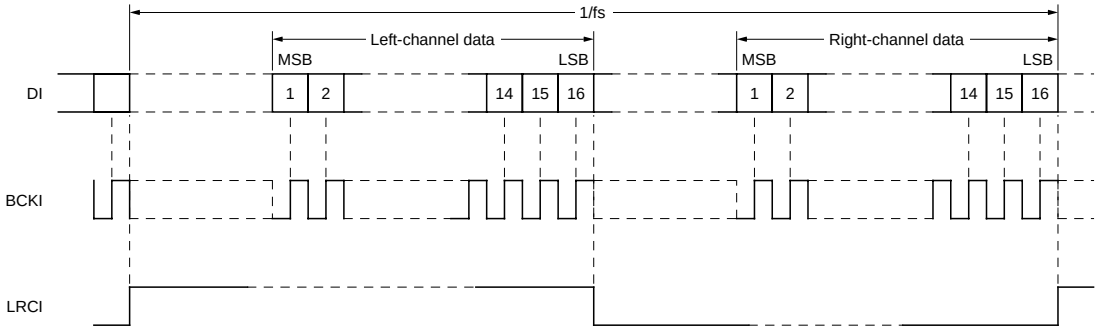
Condition	Affect
Actual sample rate conversion ratio is lower than the selected filter conversion ratio	The audio band high-pass develops aliasing noise.
Actual sample rate conversion ratio is higher than the selected filter conversion ratio	The audio band high-pass is cut off.

Note: An output noise may be generated if the fs conversion ratio changes at a rate greater than 0.057%/sec.

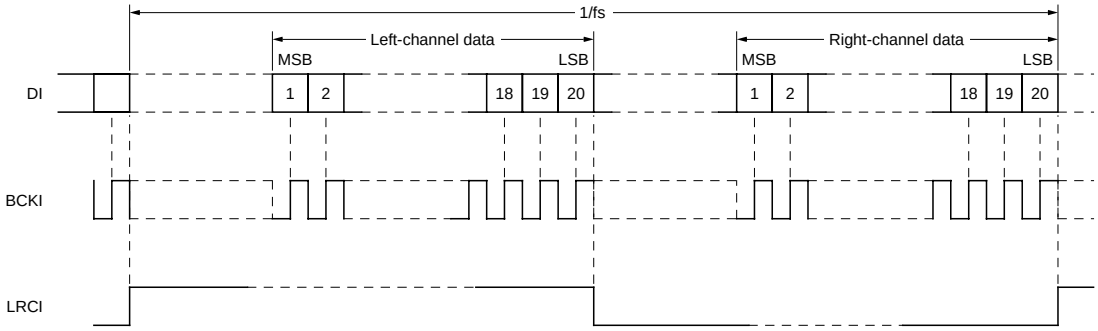
TIMING DIAGRAMS

Input Timing Examples (DI, BCKI, LRCI)

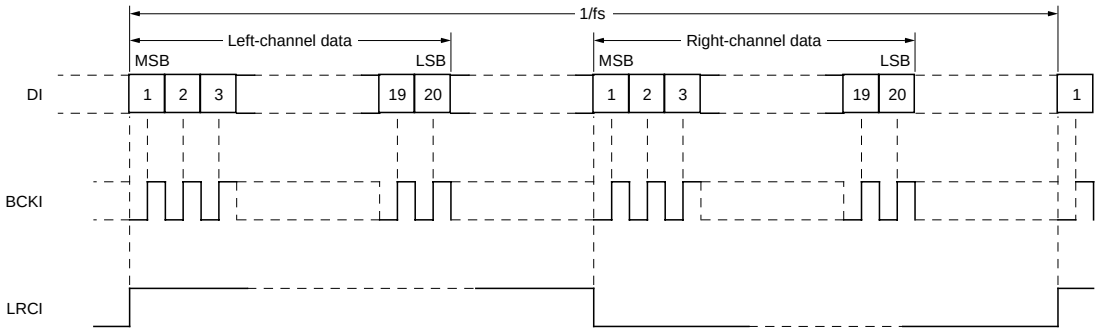
Audio data input timing (rear-packed 16-bit word, IFM1 = LOW, IFM2 = LOW)



Audio data input timing (rear-packed 20-bit word, IFM1 = LOW, IFM2 = HIGH)

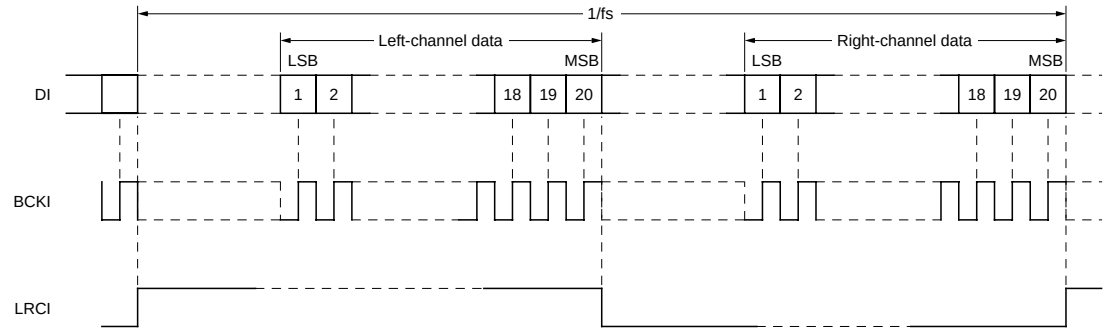


Audio data input timing (front-packed 20-bit word, IFM1 = HIGH, IFM2 = LOW)



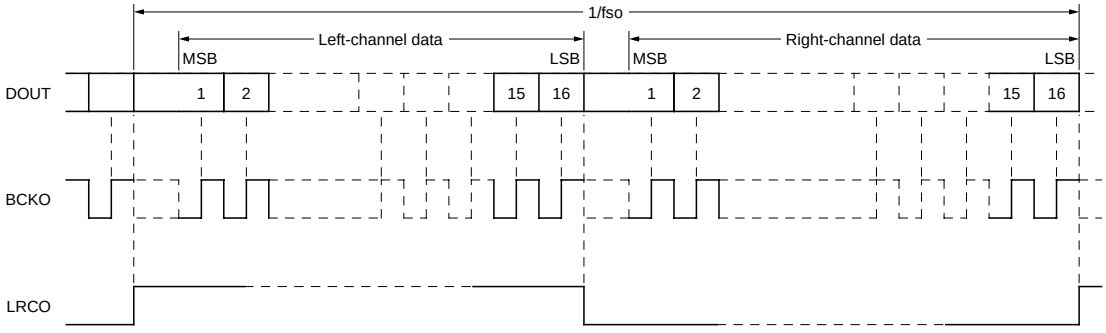
All data bits after the LSB (20th bit) are ignored. Accordingly, more than 20 BCKI cycles are required.

Audio data input timing (rear-packed 20-bit word, LSB first, IFM1 = HIGH, IFM2 = HIGH)

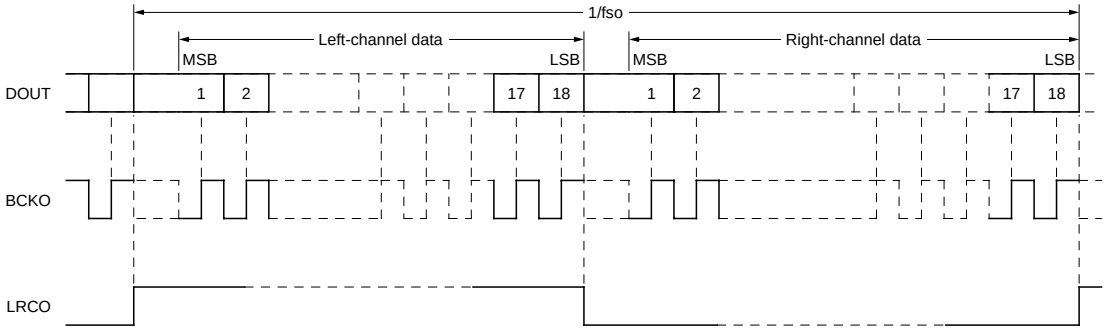


Output Timing Examples (DOUT, BCKO, LRCO)

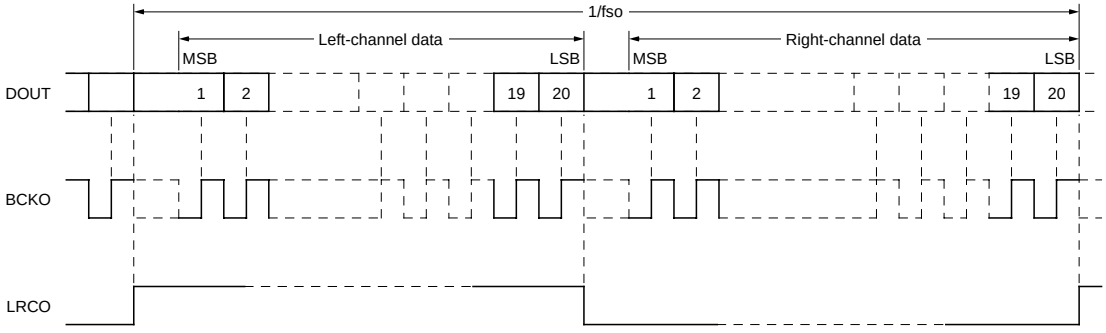
Audio data output timing (rear-packed 16-bit word)



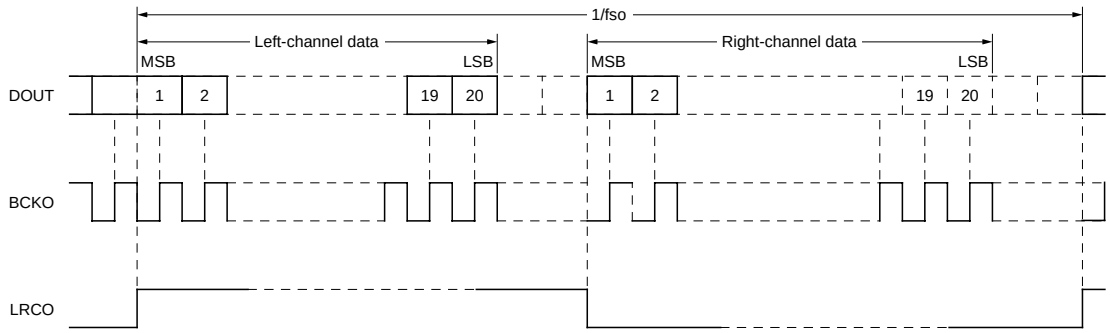
Audio data output timing (rear-packed 18-bit word)



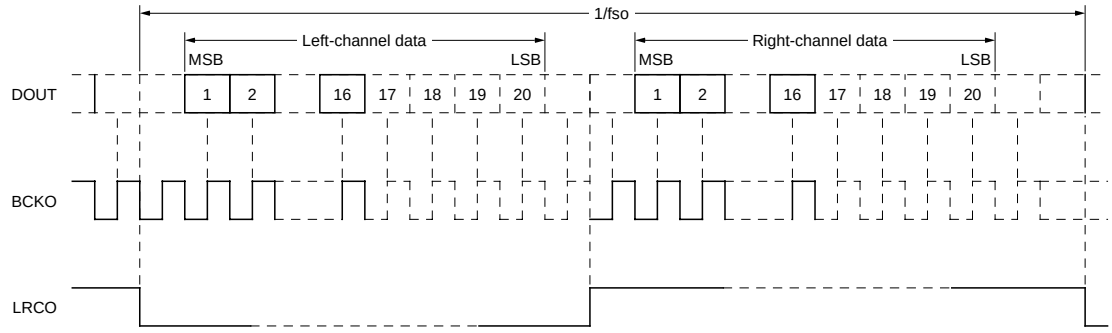
Audio data output timing (rear-packed 20-bit word)



Audio data output timing (front-packed 20-bit word, OW18N = LOW, OW20N = LOW)



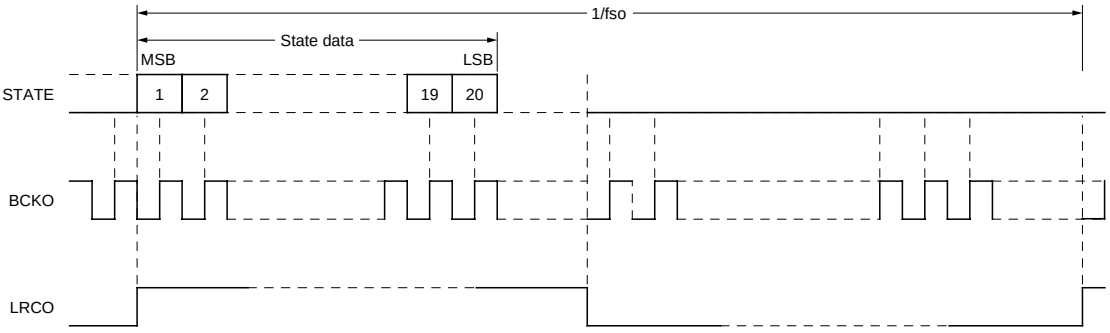
Audio data output timing (IIS mode, front-packed 16/18/20-bit word selected by OW18N and OW20N)



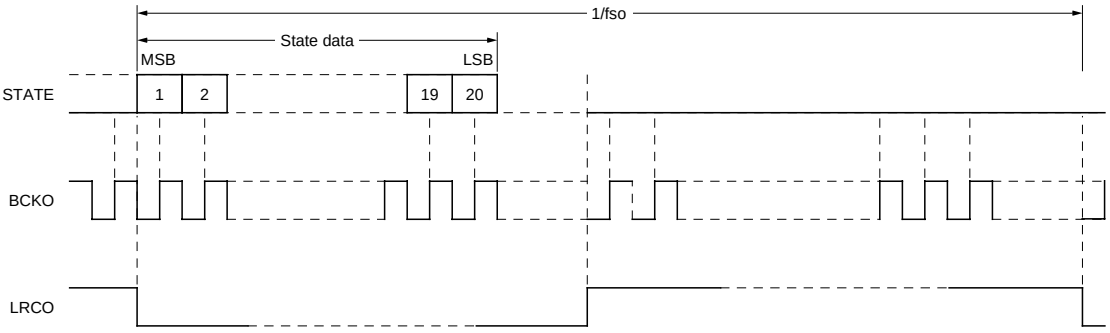
Data is output in 20-bit units.

State Data Output Timing

State data output timing (IISN = HIGH)

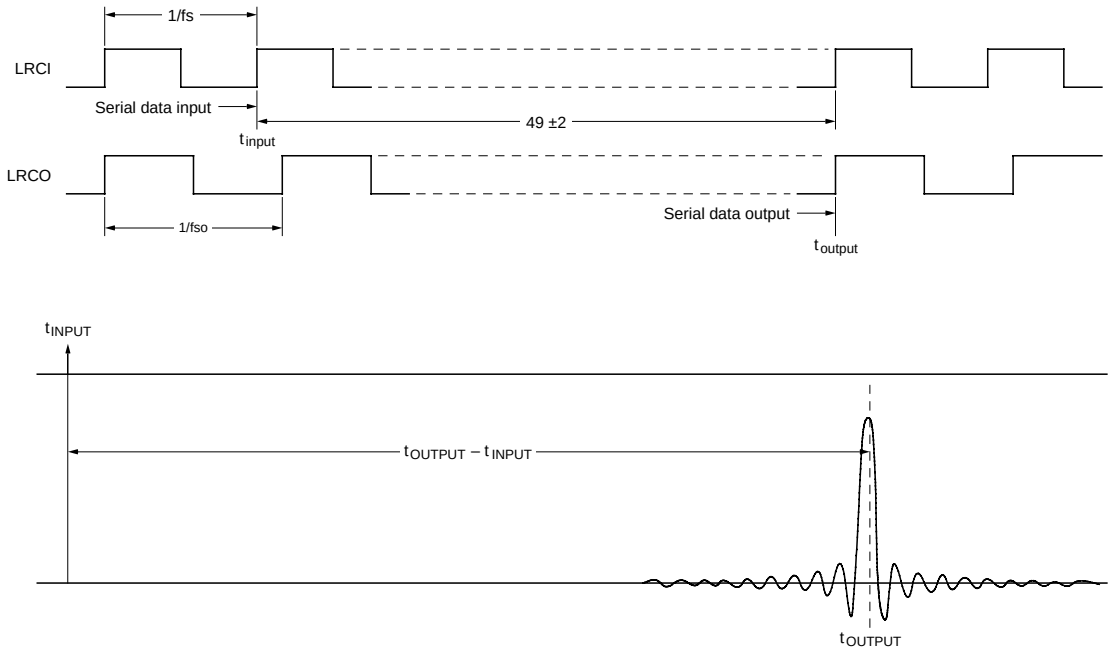


State data output timing (IISN = LOW)



Delay Time

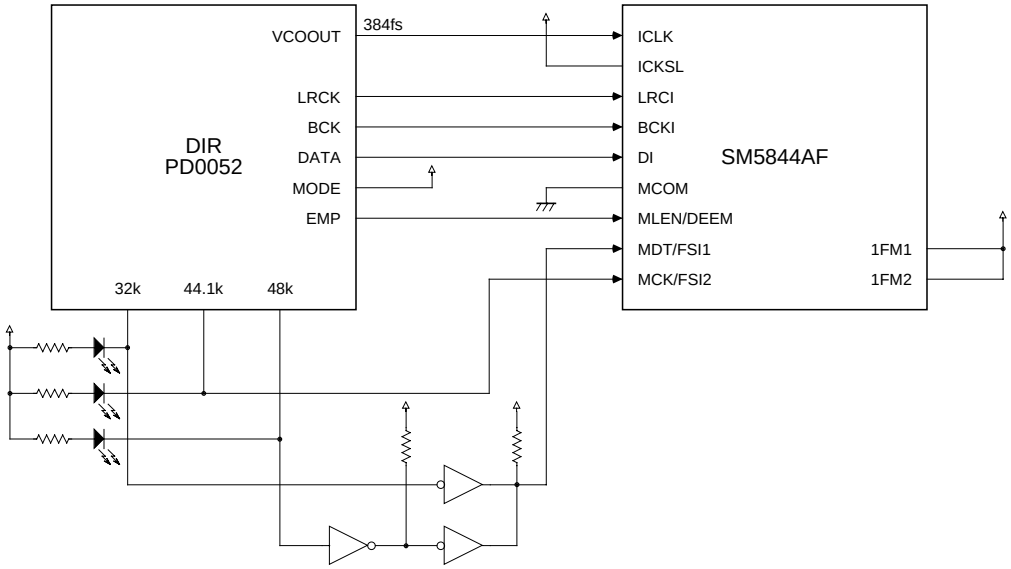
t_{INPUT} is the time when the serial input data has been read in completely (on the rising edge of LRCI). t_{OUTPUT} is the time when the serial output data has been read out completely (on the rising edge of LRCO). The delay between input and output is given by $t_{OUTPUT} - t_{INPUT} = (49 \pm 2)/fsi$.



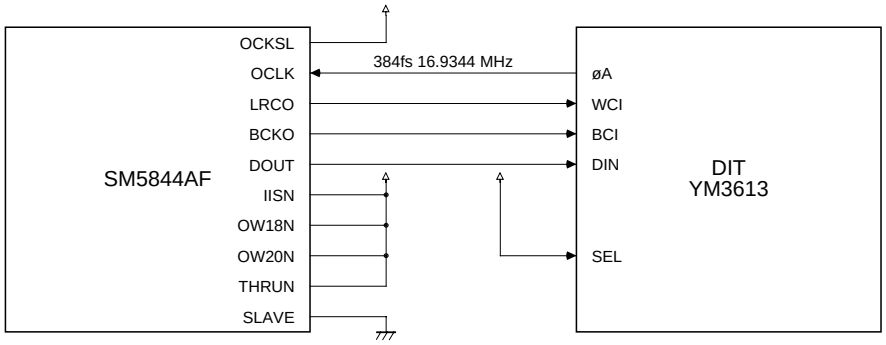
TYPICAL APPLICATIONS

Input Interface Circuits

Digital audio interface receiver (PD0052)



Digital audio interface transceiver(YM3613)



APPLICATION NOTE

Delay in the slave mode

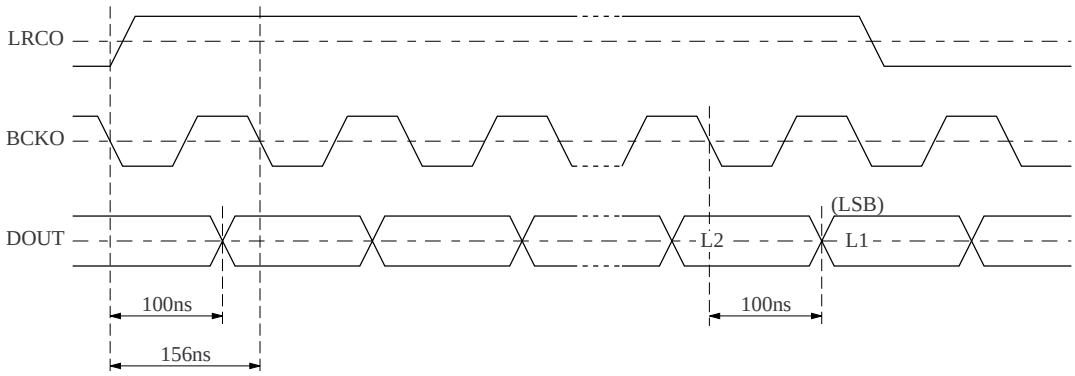
In the slave mode , the delay (tbdH2, tbdL2)of DUOT from BCKO is MIN= 10ns, MAX= 100ns which is ratter wide width.

As specified in AC Electrical Characteristics, and BCKO is prohibited from inputting longer than 64fso.

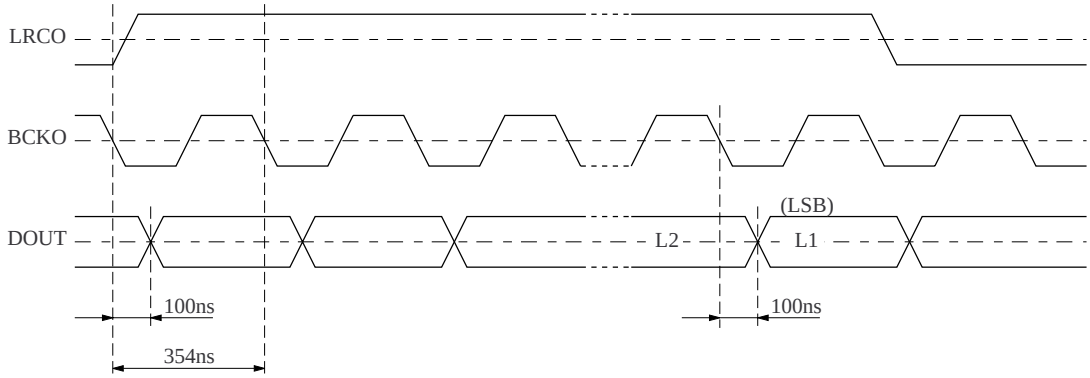
When tbdH2, tbdL2 is maximum 100ns, ideal timing may not be attained for the following devise, depending on the OCLK cycle (example 1).

Please use considering the timing in the following examples in the slave mode.

(example 1) OCLK= 39ns(fs= 99.84kHz), OCKSL= L(256fs), BCKO(64fso)= 156ns, OW20N= L, OW18N= H



(example 2) OCLK= 59ns(fs= 44.1kHz), OCKSL= H(384fs), BCKO(64fso)= 354ns, OW20N= L, OW18N= H



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