

OVERVIEW

The SM5851AF is a CMOS, digital signal processor LSI that incorporates all major functional blocks of the Dolby Prologic Surround sound system.

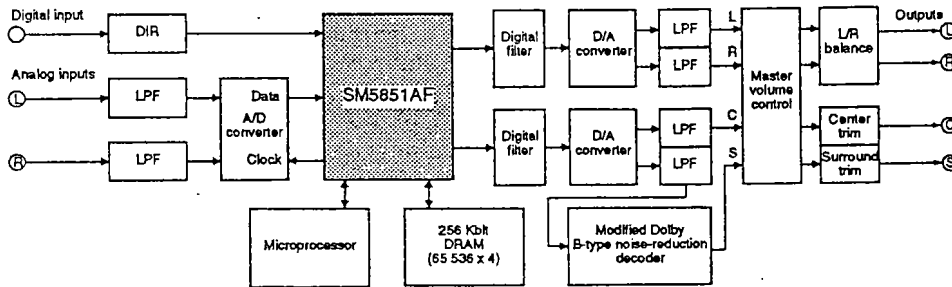
A complete decoder system conforming to the Dolby Prologic specification can be made with the addition of an A/D converter, D/A converters, a modified Dolby B decoder, a dynamic RAM and a master volume controller. The SM5851AF uses the

dynamic RAM as a digital delay for the Dolby Surround effect and other effects not in the Dolby Prologic specification.

The SM5851AF includes a serial port for communication with a microprocessor and features simple interfacing to external circuitry.

The SM5851AF operates from a single 5 V supply and is available in 64-pin QFPs.

SYSTEM BLOCK DIAGRAM



FEATURES

- Sampling frequency
 - 48 kHz, 44.1 kHz or 32 kHz sampling frequency
 - All filter coefficients change to match the selected sampling frequency.
 - A/D converter input sampling frequency set at 48 kHz
- System clock
 - 384fs system clock frequency
 - In DSP master mode, the system clock is generated by an on-chip crystal oscillator or from an external clock source.
- In DSP slave mode, the system clock is input from an external digital audio decoder or similar device.
- Deemphasis filter
 - Switchable digital deemphasis filter
- Level meter flags
 - Overflow flag indicator
 - Dolby level indicator

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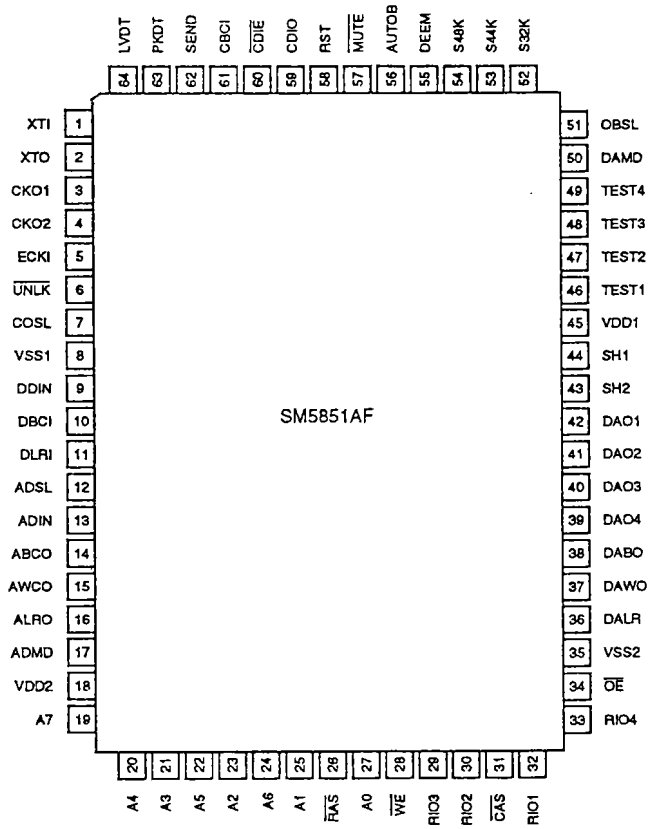
This IC is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA 94103-4813, U.S.A., from whom licensing and application information must be obtained.

- Dolby Prologic decoder functions
 - Adaptive matrix signal processing block
 - Third-order infinite impulse response (IIR) bandpass filter
 - Precision rectifier
 - Linear-to-log converter
 - Log-to-linear converter
 - Threshold switch
 - Signal polarity splitter
 - Combining network
 - Center channel modes
 - Off
 - Normal
 - Phantom
 - Wide
 - Three-channel mode
 - Optional three-channel mode that does not use the surround sound channel
 - Auto-balance
 - Input signal level balancing
 - Noise generator
 - On-chip noise generator for testing and calibration
 - Average noise level can be set to 11 dB below the Dolby reference level
 - Surround channel circuit
 - Digital delay DRAM interface
 - Second-order IIR lowpass filter
- Surround effect functions
 - Effect and simulated modes
 - Digital delay time can be controlled by the host microprocessor
 - Two-channel surround signal output
- Stereo replay functions
 - Normal stereo replay mode
 - Optional deemphasis
- Dolby reference level
 - Input reference level is 15 dB below the 16-bit full-scale amplitude.
 - Output reference level is 18 dB below the 16-bit full-scale amplitude.
- Input/output interface
 - Two serial data input interfaces
 - Three-wire digital audio decoder input
 - A/D converter interface
 - Clock generator
 - 16-bit, 2s complement, left/right alternating data format
 - Two serial data output modes
 - Four serial data output channels, with each output channel alternating between two audio data channels
 - Three serial data output channels, with each output channel cycling through four audio data channels
 - 16/18-bit selectable word length
 - 2s complement, msb first
 - Two sample-and-hold signal outputs
 - Microprocessor interface
 - Four-wire serial data inputs/outputs
 - Asynchronous data transfer
 - Digital delay DRAM interface
 - Direct interface to 256 Kbit (65 536 × 4) DRAM
 - Four programmable delay times
- Other features
 - 64-pin QFP
 - Single 5 V power supply
 - Molybdenum-gate CMOS process

SM5851AF

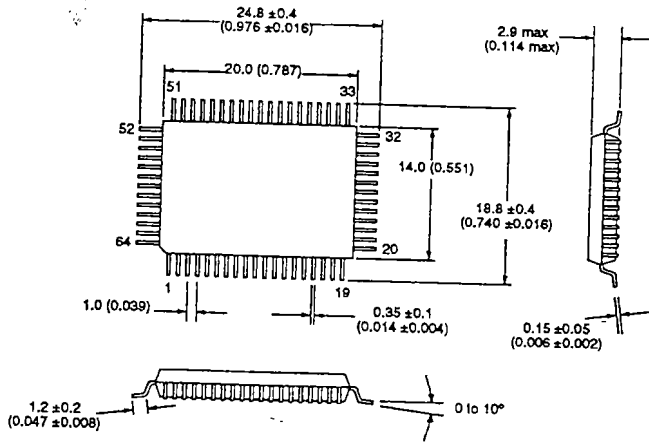
PINOUT

64-pin QFP




PACKAGE DIMENSIONS and MARKINGS

Unit: mm (inch)



NPC 

S M 5 8 5 1 A F

 Date code