NIPPON PRECISION CIRCUITS INC.

CMOS LSI ΣDECO SM5872A/B

Digital Audio D/A Converters with Built-in Digital Filters

OVERVIEW

The ΣDECO SM5872A/B D/A converters are high-speed converters for digital audio systems. They are fabricated in Molybdenum-gate CMOS. They incorporate a two-channel, 16-bit D/A converter and a digital eight-times oversampling filter, making them ideal for use in PCM and CD players and digital amplifiers. The ΣDECO SM5872A/B operate at 32, 44.1 and 48kHz sampling frequencies and incorporate deemphasis, attenuation and soft mute functions. These functions are controlled either by input pin logic levels or by the microcontroller interface. The ΣDECO SM5872A/B linearly interpolates the input signal at a high multiple of the original sampling frequency, and then requantizes the resulting signal. A fourth-order noise shaper removes most of the quantizing noise before the signal is output as a pulsewidth-modulated waveform. The ΣDECO SM5872A/B operate from a 3.2 to 5.5V supply and are available in 28-pin SOPs.

FEATURES

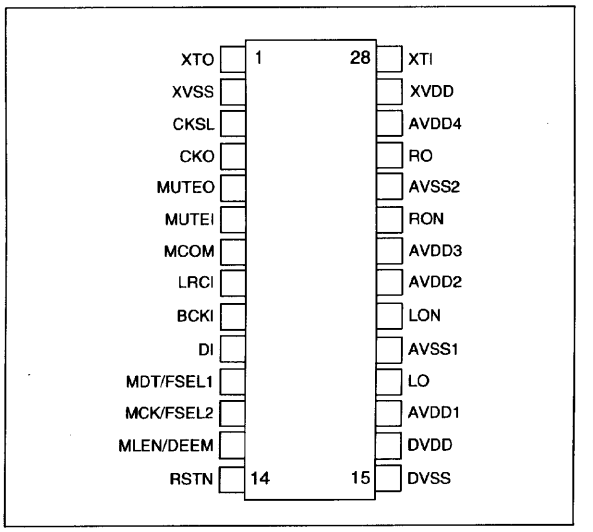
- Two-channel ΣΔ D/A converter
- 8-times oversampling FIR filter
  - 69 + 13 + 5 tap, 8fs FIR filter
  - 53dB stopband attenuation
  - ± 0.05dB passband ripple
- Fourth-order zero-shift noise shaper
- Digital deemphasis
- 128-step, linear attenuator
- Soft muting
- 13-level, quasi-symmetrical PWM outputs
- Normal- and double-speed operation (SM5872A only)
- On-chip crystal oscillation circuit
- 2s complement, msb-first, 16-bit serial input data format
- Single 5V supply in normal- and double-speed modes
- Low-voltage operation
  - 3.2V minimum supply voltage operation in normal-speed mode
  - 4.5V minimum supply voltage operation in double-speed mode
- Molybdenum-gate CMOS process
- Package: 28-pin SOP

ORDERING INFORMATION

Device	System clock	Package
SM5872AS	256fs or 512fs (selected using CKSL)	28-pin SOP
SM5872BS	384fs	

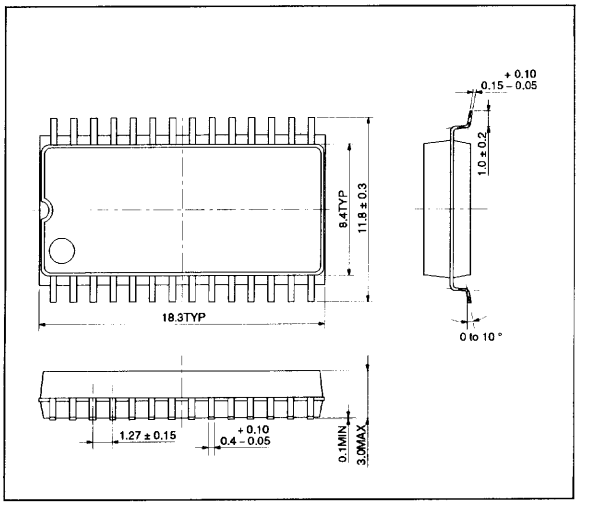
PINOUT

(Top view)

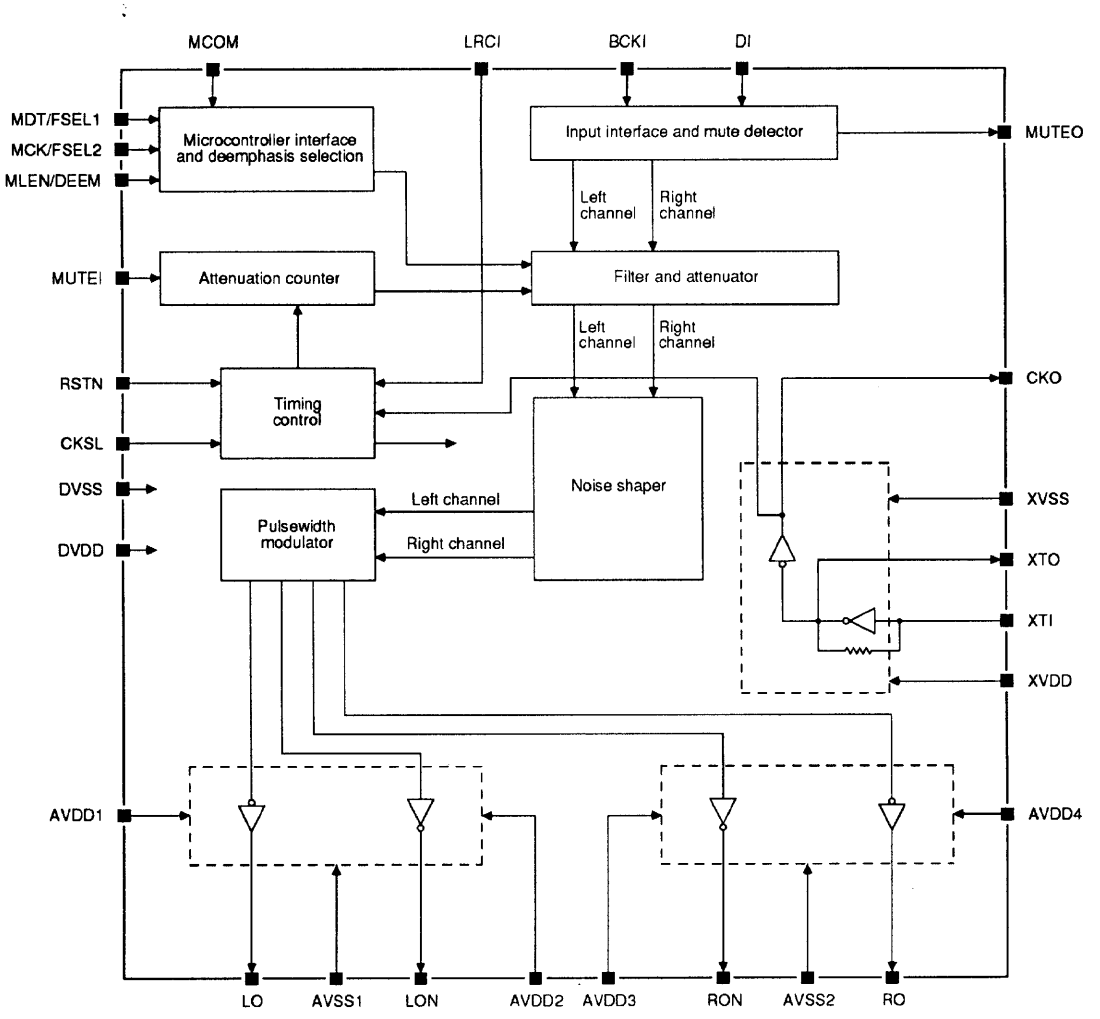


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

<table>
<tr><th>Number</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>XTO</td><td>Crystal oscillator output</td></tr>
<tr><td>2</td><td>XVSS</td><td>Clock ground</td></tr>
<tr><td>3</td><td>CKSL</td><td>Clock frequency select input.
<table>
<tr><th rowspan="2">Device</th><th colspan="2">Frequency</th></tr>
<tr><th>CLSL = HIGH</th><th>CKSL = LOW</th></tr>
<tr><td>SM5872A</td><td>512fs</td><td>256fs</td></tr>
<tr><td>SM5872B</td><td>384fs</td><td>Not used</td></tr>
</table>
Internal pull-up resistor</td></tr>
<tr><td>4</td><td>CKO</td><td>Clock output.
<table>
<tr><th rowspan="2">Device</th><th colspan="2">Frequency</th></tr>
<tr><th>CLSL = HIGH</th><th>CKSL = LOW</th></tr>
<tr><td>SM5872A</td><td>512fs</td><td>256fs</td></tr>
<tr><td>SM5872B</td><td>384fs</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>5</td><td>MUTEO</td><td>Mute detect output</td></tr>
<tr><td>6</td><td>MUTEI</td><td>Mute input. Soft muting is ON when HIGH, and OFF when LOW. Internal pull-resistor</td></tr>
<tr><td>7</td><td>MCOM</td><td>Interface mode select input. MDT, MCK and MLEN control is selected when HIGH, and FSEL1, FSEL2 and DEEM when LOW. Internal pull-up resistor</td></tr>
<tr><td>8</td><td>LRCI</td><td>Data sample rate clock input. Left channel when HIGH and right channel when LOW. Internal pull-up resistor</td></tr>
<tr><td>9</td><td>BCKI</td><td>Bit clock input. Internal pull-up resistor</td></tr>
<tr><td>10</td><td>DI</td><td>Serial data input. Internal pull-up resistor</td></tr>
<tr><td>11</td><td>MDT/FSEL1</td><td>Microcontroller interface data input MDT when MCOM is HIGH, and local mode frequency select input FSEL1 when MCOM is LOW.
<table>
<tr><th>FSEL1</th><th>FSEL2</th><th>fs</th></tr>
<tr><td>LOW</td><td>LOW</td><td>44.1 kHz</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>48.0 kHz</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>44.1 kHz</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>32.0 kHz</td></tr>
</table>
Internal pull-up resistor</td></tr>
<tr><td>12</td><td>MCK/FSEL2</td><td>Microcontroller interface clock input MCK when MCOM is HIGH, and local mode frequency select input FSEL2 when MCOM is LOW.
<table>
<tr><th>FSEL1</th><th>FSEL2</th><th>fs</th></tr>
<tr><td>LOW</td><td>LOW</td><td>44.1 kHz</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>48.0 kHz</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>44.1 kHz</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>32.0 kHz</td></tr>
</table>
Internal pull-up resistor</td></tr>
<tr><td>13</td><td>MLEN/DEEM</td><td>Microcontroller interface latch enable input MLEN when MCOM is HIGH, and local mode deemphasis control input DEEM when MCOM is LOW. Deemphasis is ON when DEEM is HIGH, and OFF when DEEM is LOW. Internal pull-up resistor.</td></tr>
</table>

<table>
<tr><th>Number</th><th>Name</th><th>Description</th></tr>
<tr><td>14</td><td>RSTN</td><td>Reset input. Normal operation when HIGH, and system reset when LOW. Internal pull-up resistor</td></tr>
<tr><td>15</td><td>DVSS</td><td>Digital ground</td></tr>
<tr><td>16</td><td>DVDD</td><td>5 V digital supply</td></tr>
<tr><td>17</td><td>AVDD1</td><td>Analog supply 1</td></tr>
<tr><td>18</td><td>LO</td><td>Left-channel positive PWM output</td></tr>
<tr><td>19</td><td>AVSS1</td><td>Analog ground 1</td></tr>
<tr><td>20</td><td>LON</td><td>Left-channel negative PWM output</td></tr>
<tr><td>21</td><td>AVDD2</td><td>Analog supply 2</td></tr>
<tr><td>22</td><td>AVDD3</td><td>Analog supply 3</td></tr>
<tr><td>23</td><td>RON</td><td>Right-channel negative PWM output</td></tr>
<tr><td>24</td><td>AVSS2</td><td>Analog ground 2</td></tr>
<tr><td>25</td><td>RO</td><td>Right-channel positive PWM output.</td></tr>
<tr><td>26</td><td>AVDD4</td><td>Analog supply 4</td></tr>
<tr><td>27</td><td>XVDD</td><td>Clock supply</td></tr>
<tr><td>28</td><td>XTI</td><td>Crystal oscillator or external clock input.
<table>
<tr><th rowspan="2">Device</th><th colspan="2">Frequency</th></tr>
<tr><th>CLSL = HIGH</th><th>CKSL = LOW</th></tr>
<tr><td>SM5872A</td><td>512fs</td><td>256fs</td></tr>
<tr><td>SM5872B</td><td>384fs</td><td>Not used</td></tr>
</table></td></tr>
</table>

SPECIFICATIONS

Absolute Maximum Ratings

$DV_{SS} = AV_{SS} = XV_{SS} = 0$ V, $AV_{SS} = AV_{SS1} = AV_{SS2}$, $AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}$

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	–0.3 to 7.0	V
Input voltage range for all inputs except XTI	V_{I1}	DV_{SS} – 0.3 to DV_{DD} + 0.3	V
XTI input voltage range	V_{I2}	XV_{SS} – 0.3 to XV_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Storage temperature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{SLD}	255	deg. C
Soldering time	t_{SLD}	10	s

Recommended Operating Conditions

DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	3.2 to 5.5	V
Operating temperature range	T_{opr}	−20 to 80	deg. C

Note

All power supply pins (VDD and VSS) must be connected to the same external power supply unit.

DC Electrical Characteristics

SM5872A

Normal supply voltage operation

DV_{DD} = AV_{DD} = XV_{DD} = 4.5 to 5.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}, T_a = −20 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Digital circuitry supply current	I_{DDD}	DV_{DD} = AV_{DD} = XV_{DD} = 5 V, f_{XTI} = 256fs = 24.6 MHz, no load, double speed mode. CKSL is LOW. See note 4.	–	27	35	mA
Clock circuitry supply current	I_{DDX}		–	3	5	mA
Analog circuitry supply current	I_{DDA}		–	1	2	mA
XTI HIGH-level input voltage	V_{IH1}	External clock input	0.7 × XV_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3 × XV_{DD}	V
XTI AC input voltage	V_{INAC}	AC coupled input	0.3 × XV_{DD}	–	–	V_{p-p}
HIGH-level input voltage. See note 1.	V_{IH2}		2.4	–	–	V
LOW-level input voltage. See note 1.	V_{IL2}		–	–	0.5	V
HIGH-level output voltage. See note 2.	V_{OHA}	I_{OH} = −1 mA	AV_{DD} − 0.3	–	–	V
LOW-level output voltage. See note 2.	V_{OLA}	I_{OL} = 1 mA	–	–	0.3	V
CKO HIGH-level output voltage	V_{OHC}	I_{OH} = −1 mA	4.0	–	–	V
CKO LOW-level output voltage	V_{OLC}	I_{OL} = 2 mA	–	–	0.5	V
MUTEO HIGH-level output voltage	V_{OHM}	I_{OH} = −1 mA	4.0	–	–	V
MUTEO LOW-level output voltage	V_{OLM}	I_{OL} = 2 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	V_I = XV_{DD}	–	10	20	µA
XTI LOW-level input current	I_{IL1}	V_I = 0 V	–	10	20	µA
LOW-level input current. See note 1.	I_{IL2}	V_I = 0 V	–	10	20	µA
Input leakage current. See note 1.	I_{LH}	V_I = DV_{DD}	–	–	1.0	µA

Notes

1. Pins CKSL, LRCI, BCKI, DI, MUTEI, MCOM, RSTN, MDT/FSEL1, MCK/FSEL2 and MLEN/DEEM
2. Pins LO, LON, RO and RON
3. I_{DDA} is the total current.
4. I_{DDD} in normal-speed mode is 20 mA (typ) and 25 mA (max).

Low supply voltage operation

DV_{DD} = AV_{DD} = XV_{DD} = 3.2 to 4.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}, T_a = −20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Digital circuitry supply current	I_{DDD}	DV_{DD} = AV_{DD} = XV_{DD} = 3.4 V, f_{XTI} = 512fs = 24.6 MHz, no load, normal speed mode. CKSL is HIGH.	–	11	15	mA
Clock circuitry supply current	I_{DDX}		–	2	3	mA
Analog circuitry supply current	I_{DDA}		–	0.5	1	mA
XTI HIGH-level input voltage	V_{IH1}	External clock input	0.7 × XV_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3 × XV_{DD}	V
XTI AC input voltage	V_{INAC}	AC coupled input	0.3 × XV_{DD}	–	–	V_{P-P}
HIGH-level input voltage. See note 1.	V_{IH2}		2.4	–	–	V
LOW-level input voltage. See note 1.	V_{IL2}		–	–	0.5	V
HIGH-level output voltage. See note 2.	V_{OHA}	I_{OH} = −1 mA	AV_{DD} − 0.3	–	–	V
LOW-level output voltage. See note 2.	V_{OLA}	I_{OL} = 1 mA	–	–	0.3	V
CKO HIGH-level output voltage	V_{OHC}	I_{OH} = −0.4 mA	2.5	–	–	V
CKO LOW-level output voltage	V_{OLC}	I_{OL} = 0.8 mA	–	–	0.4	V
MUTEO HIGH-level output voltage	V_{OHM}	I_{OH} = −0.4 mA	2.5	–	–	V
MUTEO LOW-level output voltage	V_{OLM}	I_{OL} = 0.8 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	V_I = XV_{DD}	–	–	15	µA
XTI LOW-level input current	I_{IL1}	V_I = 0 V	–	–	15	µA
LOW-level input current. See note 1.	I_{IL2}	V_I = 0 V	–	–	15	µA
Input leakage current. See note 1.	I_{LH}	V_I = DV_{DD}	–	–	1.0	µA

Notes

1. Pins CKSL, LRCI, BCKI, DI, MUTEI, MCOM, RSTN, MDT/FSEL1, MCK/FSEL2 and MLEN/DEEM
2. Pins LO, LON, RO and RON
3. I_{DDA} is the total current.

SM5872B

Normal supply voltage operation

DV_{DD} = AV_{DD} = XV_{DD} = 4.5 to 5.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}, T_a = −20 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Digital circuitry supply current	I_{DDD}	DV_{DD} = AV_{DD} = XV_{DD} = 5 V, f_{XTI} = 384fs = 16.9 MHz, no load. CKSL is HIGH.	–	15	25	mA
Clock circuitry supply current	I_{DDX}		–	3	5	mA
Analog circuitry supply current	I_{DDA}		–	1	2	mA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI HIGH-level input voltage	V_{IH1}	External clock input	0.7 × XV_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3 × XV_{DD}	V
XTI AC input voltage	V_{INAC}	AC coupled input	0.3 × XV_{DD}	–	–	V_{p-p}
HIGH-level input voltage. See note 1.	V_{IH2}		2.4	–	–	V
LOW-level input voltage. See note 1.	V_{IL2}		–	–	0.5	V
HIGH-level output voltage. See note 2.	V_{OHA}	I_{OH} = –1 mA	AV_{DD} – 0.3	–	–	V
LOW-level output voltage. See note 2.	V_{OLA}	I_{OL} = 1 mA	–	–	0.3	V
CKO HIGH-level output voltage	V_{OHC}	I_{OH} = –1 mA	4.0	–	–	V
CKO LOW-level output voltage	V_{OLC}	I_{OL} = 2 mA	–	–	0.5	V
MUTEO HIGH-level output voltage	V_{OHM}	I_{OH} = –1 mA	4.0	–	–	V
MUTEO LOW-level output voltage	V_{OLM}	I_{OL} = 2 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	V_I = XV_{DD}	–	10	20	µA
XTI LOW-level input current	I_{IL1}	V_I = 0 V	–	10	20	µA
LOW-level input current. See note 1.	I_{IL2}	V_I = 0 V	–	10	20	µA
Input leakage current. See note 1.	I_{LH}	V_I = DV_{DD}	–	–	1.0	µA

Notes

1. Pins CKSL, LRCI, BCKI, DI, MUTEI, MCOM, RSTN, MDT/FSEL1, MCK/FSEL2 and MLEN/DEEM
2. Pins LO, LON, RO and RON
3. I_{DDA} is the total current.

Low supply voltage operation

DV_{DD} = AV_{DD} = XV_{DD} = 3.2 to 4.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}, T_a = –20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Digital circuitry supply current	I_{DDD}	DV_{DD} = AV_{DD} = XV_{DD} = 3.4 V, f_{XTI} = 384fs = 16.9 MHz, no load, normal speed mode. CKSL is HIGH.	–	8	12	mA
Clock circuitry supply current	I_{DDX}		–	2	3	mA
Analog circuitry supply current	I_{DDA}		–	0.5	1	mA
XTI HIGH-level input voltage	V_{IH1}	External clock input	0.7 × XV_{DD}	–	–	V
XTI LOW-level input voltage	V_{IL1}		–	–	0.3 × XV_{DD}	V
XTI AC input voltage	V_{INAC}	AC coupled input	0.3 × XV_{DD}	–	–	V_{p-p}
HIGH-level input voltage. See note 1.	V_{IH2}		2.4	–	–	V
LOW-level input voltage. See note 1.	V_{IL2}		–	–	0.5	V
HIGH-level output voltage. See note 2.	V_{OHA}	I_{OH} = –1 mA	AV_{DD} – 0.3	–	–	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LOW-level output voltage. See note 2.	V_{OLA}	I_{OL} = 1 mA	–	–	0.3	V
CKO HIGH-level output voltage	V_{OHC}	I_{OH} = –0.4 mA	2.5	–	–	V
CKO LOW-level output voltage	V_{OLC}	I_{OL} = 0.8 mA	–	–	0.4	V
MUTEO HIGH-level output voltage	V_{OHM}	I_{OH} = –0.4 mA	2.5	–	–	V
MUTEO LOW-level output voltage	V_{OLM}	I_{OL} = 0.8 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	V_I = XV_{DD}	–	–	15	µA
XTI LOW-level input current	I_{IL1}	V_I = 0 V	–	–	15	µA
LOW-level input current. See note 1.	I_{IL2}	V_I = 0 V	–	–	15	µA
Input leakage current. See note 1.	I_{LH}	V_I = DV_{DD}	–	–	1.0	µA

Notes

1. Pins CKSL, LRCI, BCKI, DI, MUTEI, MCOM, RSTN, MDT/FSEL1, MCK/FSEL2 and MLEN/DEEM
2. Pins LO, LON, RO and RON
3. I_{DDA} is the total current.

AC Digital Characteristics

The conditions for normal supply voltage operation are DV_{DD} = AV_{DD} = XV_{DD} = 4.5 to 5.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}, T_a = –20 to 80 deg. C unless otherwise noted.
The conditions for low supply voltage operation are DV_{DD} = AV_{DD} = XV_{DD} = 3.2 to 4.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}, T_a = –20 to 70 deg. C unless otherwise noted.

System clock

SM5872A

Normal-speed mode

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock frequency	f_{OSC}	CKSL is LOW. 256fs	4.0	12.3	13.0	MHz
		CKSL is HIGH. 512fs	4.0	24.6	26.0	
External clock LOW-level pulsewidth	t_{CWL}	CKSL is LOW. 256fs	34	40.7	125	ns
		CKSL is HIGH. 512fs	17	20.3	125	
External clock HIGH-level pulsewidth	t_{CWH}	CKSL is LOW. 256fs	34	40.7	125	ns
		CKSL is HIGH. 512fs	17	20.3	125	
External clock period	t_{XI}	CKSL is LOW. 256fs	77	81.4	250	ns
		CKSL is HIGH. 512fs	38.5	40.7	250	

Note

Typical values shown are for fs = 48 kHz.

Double-speed mode

DV_{DD} = AV_{DD} = XV_{DD} = 4.5 to 5.5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}, T_a = −20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock frequency	f_{OSC}	CKSL is LOW. 256fs, crystal oscillator operation	4.0	24.6	25.0	MHz
External clock LOW-level pulsewidth	t_{CWL}	CKSL is LOW. 256fs	17	20.3	125	ns
External clock HIGH-level pulsewidth	t_{CWH}	CKSL is LOW. 256fs	17	20.3	125	ns
External clock period	t_{XI}	CKSL is LOW. 256fs	40.0	40.7	250	ns

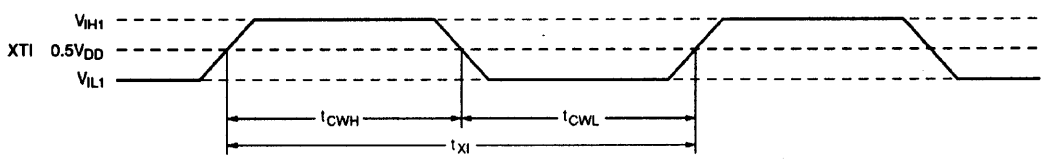
Note

Typical values shown are for fs = 96 kHz.

SM5872B

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock frequency	f_{OSC}	384fs, crystal oscillator operation	4.0	16.9	19.3	MHz
External clock LOW-level pulsewidth	t_{CWL}	384fs	21.7	29.5	125	ns
External clock HIGH-level pulsewidth	t_{CWH}	384fs	21.7	29.5	125	ns
External clock period	t_{XI}	384fs	51.7	59.0	250	ns

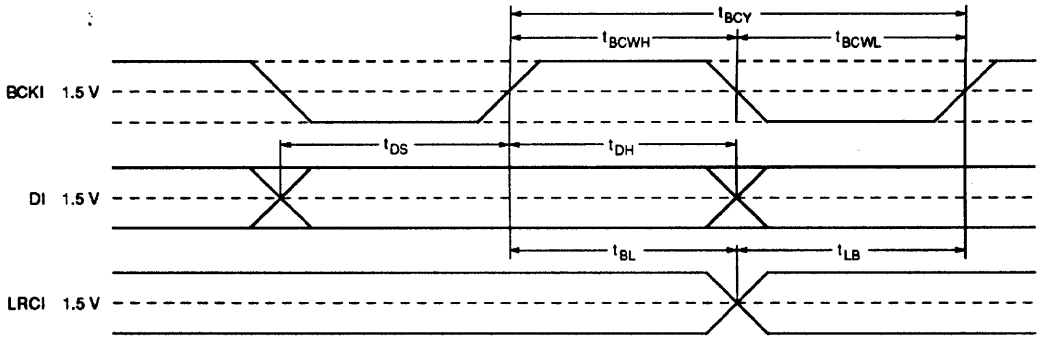
System clock timing waveform



Serial input timing

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI period	t_{BCY}	100	–	–	ns
DI setup time	t_{DS}	50	–	–	ns
DI hold time	t_{DH}	50	–	–	ns
BCKI to LRCI delay time	t_{BL}	50	–	–	ns
LRCI to BCKI delay time	t_{LB}	50	–	–	ns

Serial input timing waveform



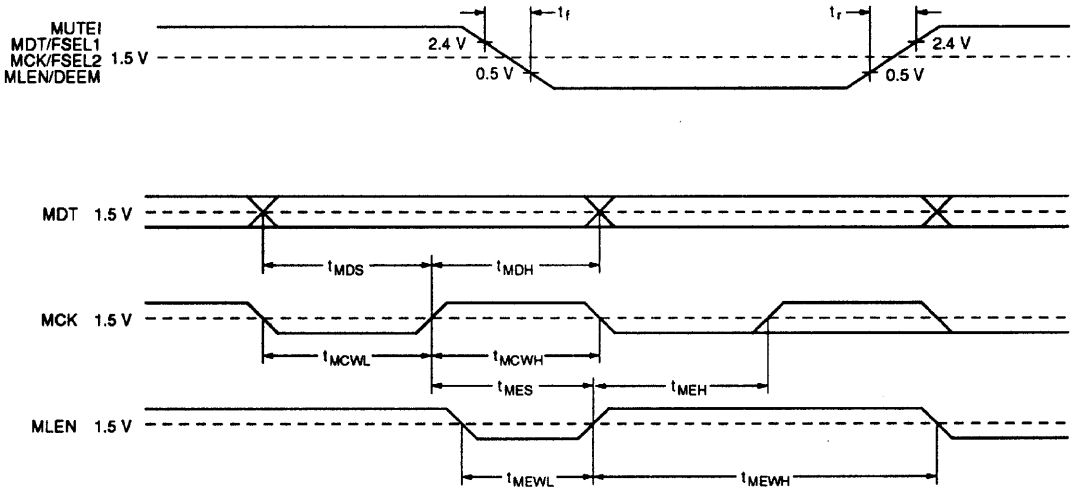
Control input timing

Parameter	Symbol	Rating			Unit
		min	typ	max	
Clock signal rise time	t_r	–	–	100	ns
Clock signal fall time	t_f	–	–	100	ns
MCK LOW-level pulsewidth	t_{MCWL}	50	–	–	ns
MCK HIGH-level pulsewidth	t_{MCWH}	50	–	–	ns
MDT setup time	t_{MDS}	50	–	–	ns
MDT hold time	t_{MDH}	50	–	–	ns
MLEN LOW-level pulsewidth	t_{MEWL}	50	–	–	ns
MLEN HIGH-level pulsewidth	t_{MEWH}	50	–	–	ns
MLEN setup time	t_{MES}	50	–	–	ns
MLEN hold time	t_{MEH}	50	–	–	ns

Note

Pins MUTEI, MDT/FSEL1, MCK/FSEL2 and MLEN/DEEM

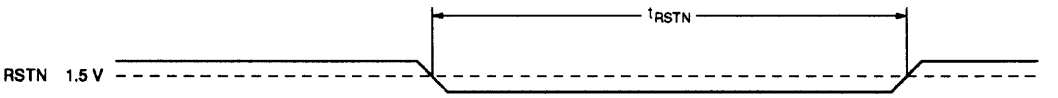
Control input timing waveforms



Reset input timing

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RSTN LOW-level pulsewidth	t_{RSTN}	After power-up	20	–	–	ns

Reset input timing waveform



AC Analog Characteristics

DV_{DD} = AV_{DD} = XV_{DD} = 5 V, DV_{SS} = AV_{SS} = XV_{SS} = 0 V, AV_{SS} = AV_{SS1} = AV_{SS2}, AV_{DD} = AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4}, CKSL is HIGH, crystal oscillator operation, f_{OSC} = 22.5792 MHz (SM5872A) or 16.9344 MHz (SM5872B), T_a = 25 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion and noise	THD + N	f = 1 kHz, V_I = 0 dB	–	0.0020	0.0035	%
Output level	V_{OUT}	f = 1 kHz, V_I = 0 dB	1.8	2.0	2.2	V_{rms}
Dynamic range	D.R	f = 1 kHz, V_I = –60 dB	92	98	–	dB
Signal-to-noise ratio	S/N	f = 1 kHz, V_I = 0 to –∞ dB. See note.	96	102	–	dB
Channel separation	Ch. Sep	f = 1 kHz, V_I = 0 to –∞ dB	92	98	–	dB

Note

The signal-to-noise ratio (S/N) is measured after reset has been cancelled and with DI held LOW. This includes the noise produced by the noise shaper.

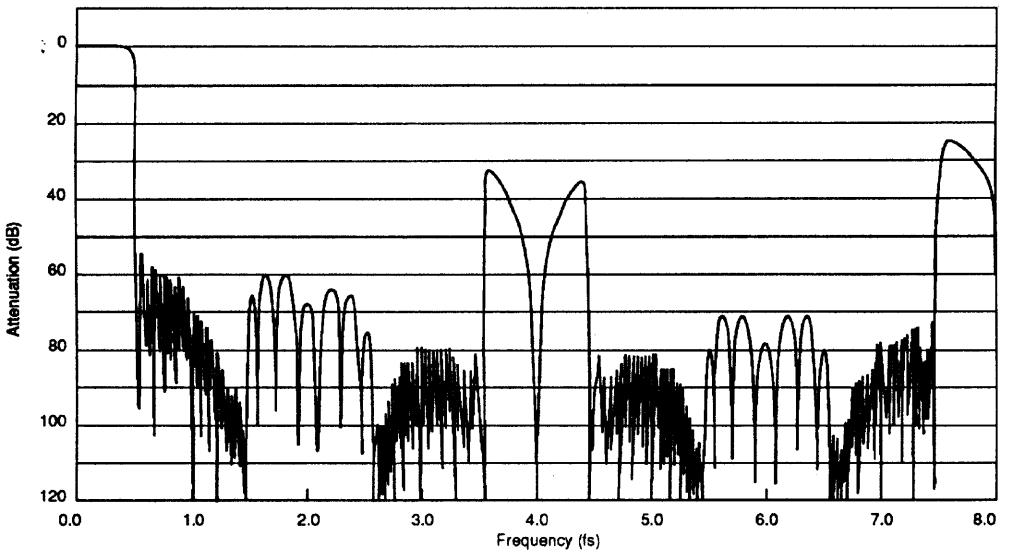
Theoretical Filter Characteristics

The overall frequency characteristics of the IIR deemphasis filter, the eight-times oversampling FIR filter, and the 32fs sample-and-hold circuit are shown in the following tables and graphs.

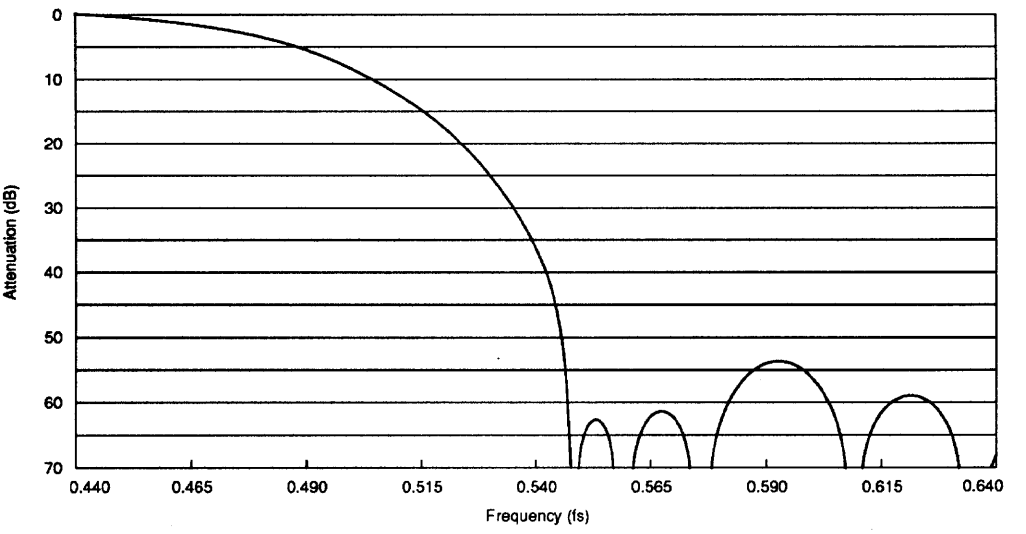
Deemphasis disabled

Parameter	Frequency range		Rating			Unit
	fs	@fs = 44.1 kHz	min	typ	max	
Passband ripple	0 to 0.4535	0 to 20.0	–0.05	–	0.05	dB
Attenuation relative to 1 kHz signal	0.4535	20.0	–	–	0.34	dB
Stopband attenuation	0.5465 to 3.45	24.1 to 152	53	–	–	dB
	3.45 to 4.55	152 to 201	32	–	–	
	4.55 to 7.45	201 to 328	70	–	–	

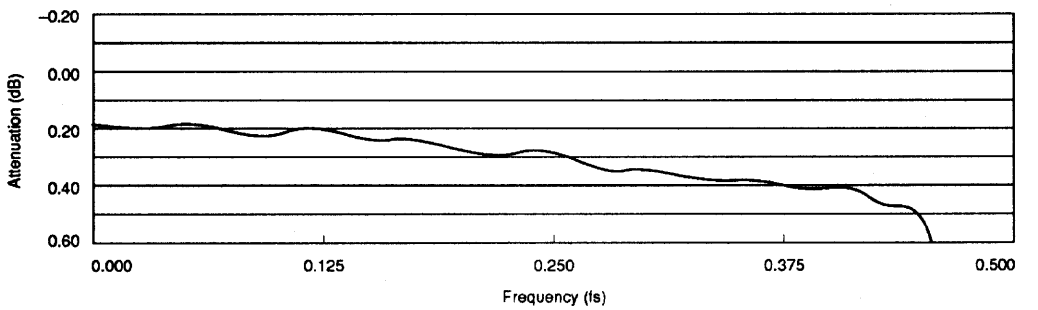
Overall frequency characteristic (Deemphasis OFF)



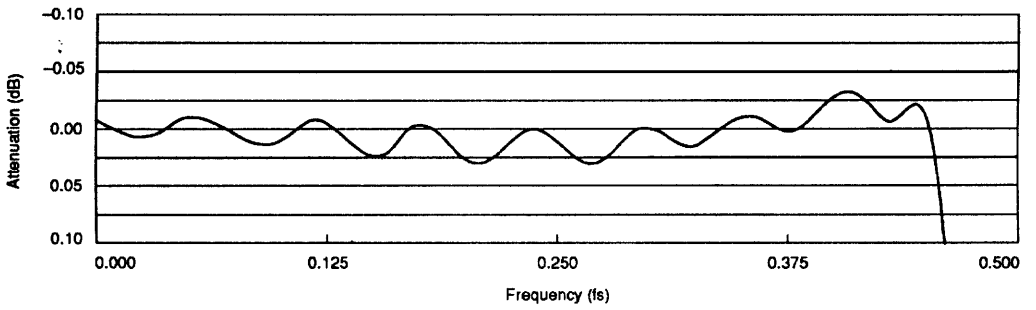
Transition band characteristic (Deemphasis OFF)



Passband characteristic (Deemphasis OFF)



Passband-only ripple characteristic (Deemphasis OFF)



Deemphasis enabled

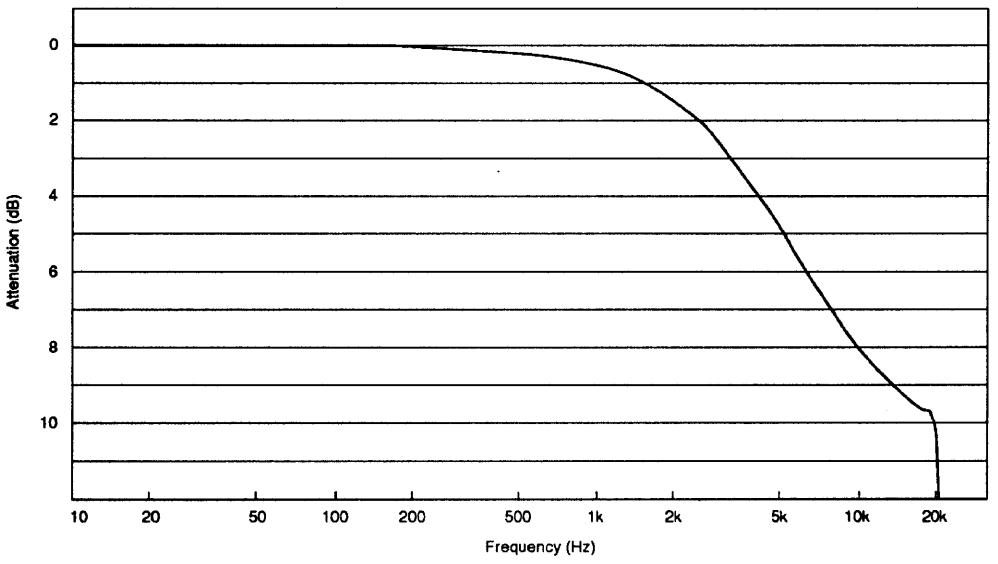
Parameter	Sampling frequency, fs	Passband	Rating			Unit
			min	typ	max	
Deviation from ideal characteristics	44.1 kHz	0 to 19.6 kHz	−0.1	-	0.3	dB
	48.0 kHz	0 to 21.4 kHz	−0.1	-	0.3	dB
	32.0 kHz	0 to 14.0 kHz	−0.4	-	0.6	dB

Note

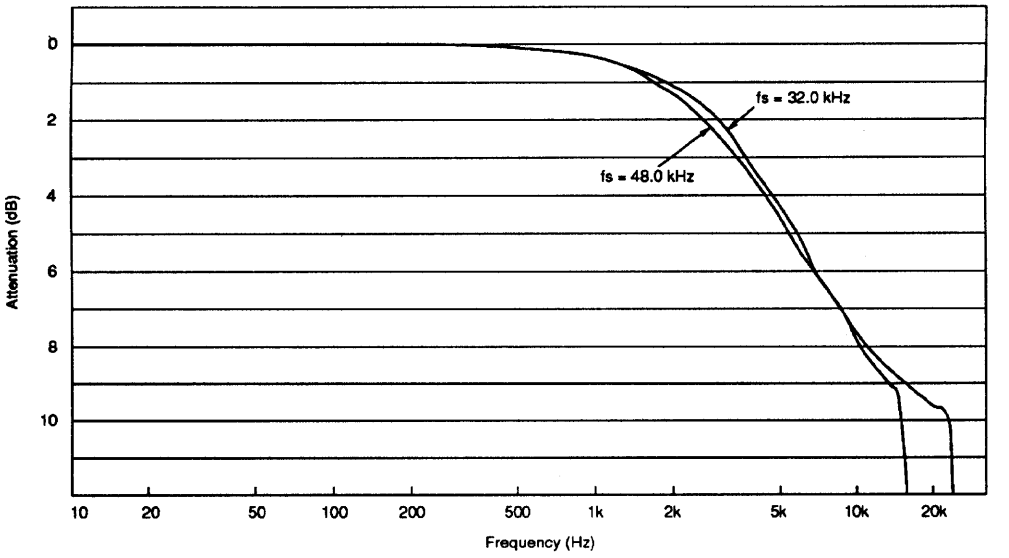
All frequencies are doubled in double-speed mode.

Overall frequency characteristic (Deemphasis ON)

fs = 44.1 kHz

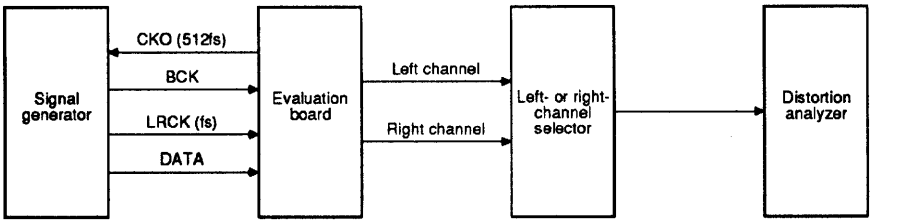


fs = 32.0 or 48.0 kHz

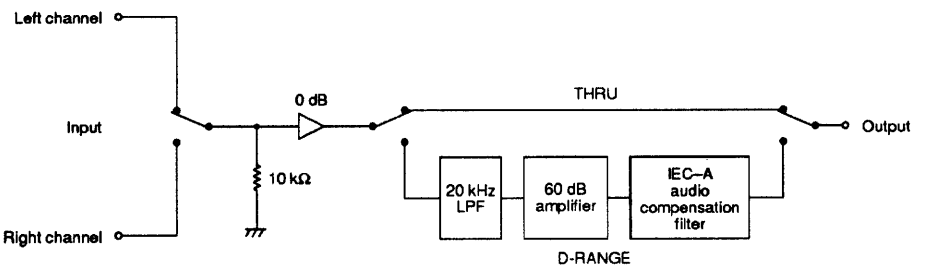


Measurement Circuits

Measurement circuit block diagram



Channel selector internal circuit



Measurement conditions

Parameter	Symbol	3346A channel selector position	AD725C distortion analyzer setting
Total harmonic distortion and noise	THD + N	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF.
Output level	V_O		
Dynamic range	D.R	D-RANGE	
Signal-to-noise ratio	S/N	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF. JIS* A-weighted filter is ON.
Channel separation	Ch. Sep	THRU	20 kHz lowpass filter is ON. 400 Hz highpass filter is OFF.

Note
JIS = Japanese Industrial Standard

FUNCTIONAL DESCRIPTION

Functional Block Diagram

The basic arithmetic operation of the ΣDECO SM5872A/B is shown in figure 1.

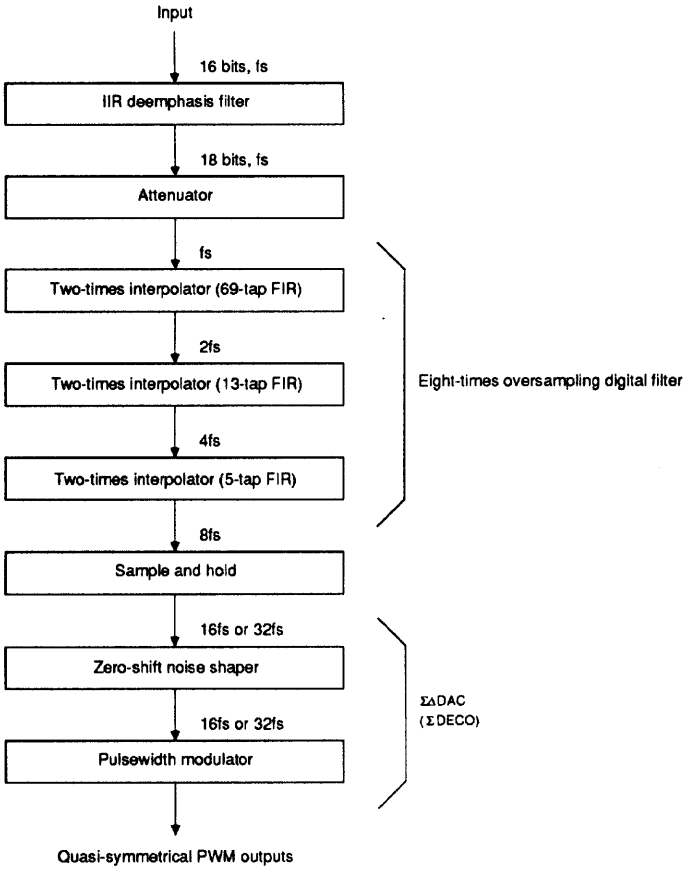


Figure 1. Arithmetic operation

Oversampling Filter

The oversampling filter comprises three, two-times oversampling filters—a 69-tap finite impulse response (FIR) filter, a 13-tap FIR filter and a 5-tap FIR filter. These filters raise the sample rate of the input signal to 8fs and attenuate quantization noise between 0.5465fs and 7.4535fs. The signal is oversampled again to either 16fs or 32fs by the sample-and-hold circuit and then input to the zero-shift noise shaper.

Controlling the Built-in Functions

The built-in functions are controlled either by input pin logic levels or by the microcontroller interface as shown in table 1.

Table 1. Built-in functions

Function	Input pin logic level mode (MCOM is LOW)	Microcontroller interface mode (MCOM is HIGH)
Deemphasis ON/OFF	DEEM	FDEEM
Deemphasis fs mode	FSEL1, FSEL2	FFSL1, FFSL2
Attenuator data	No attenuation	7-bit data (a1 to a7)
IIS (64fs BCKI) mode	Not selectable	IIS
BCKI polarity mode	Not selectable	BCPL

Note that the deemphasis functions can be controlled using both methods. The MCOM state and the control mode should not be changed after a reset or power-ON.

Microcontroller Interface

When MCOM is HIGH, MDT, MCK and MLEN function as the microcontroller data clock and latch enable inputs, respectively. Using this interface, an external microcontroller can control the built-in functions and also read the attenuation data and mode flag registers.

The data from the microcontroller input on MDT is latched into the internal shift register on the rising edge of MCK. Changing the state of MDT should, therefore, be done on the falling edge of MCK. The data in the serial-in-parallel-out (SIPO) shift register is latched into either the attenuation data or the mode flag registers on the rising edge of MLEN.

When the first data bit, B1 is LOW, the attenuation data, shown in figure 2, is written to the attenuation data register. When B1 is HIGH, the mode flags, shown in figure 3 and table 2 are written to the mode flag register. Note that MCK and MLEN can have waveforms as shown by the dotted lines in the following two figures.

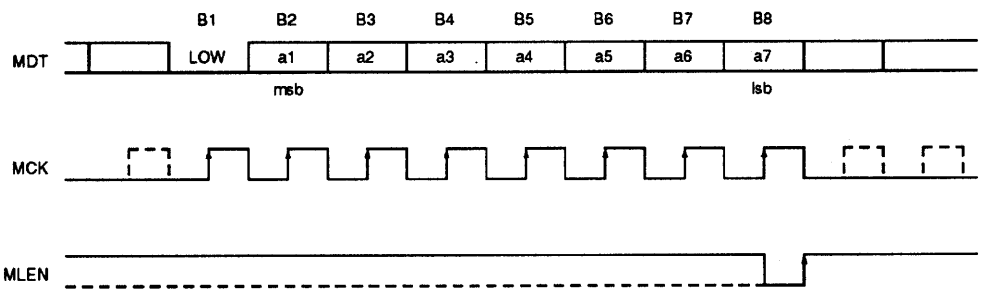


Figure 2. Attenuation data input

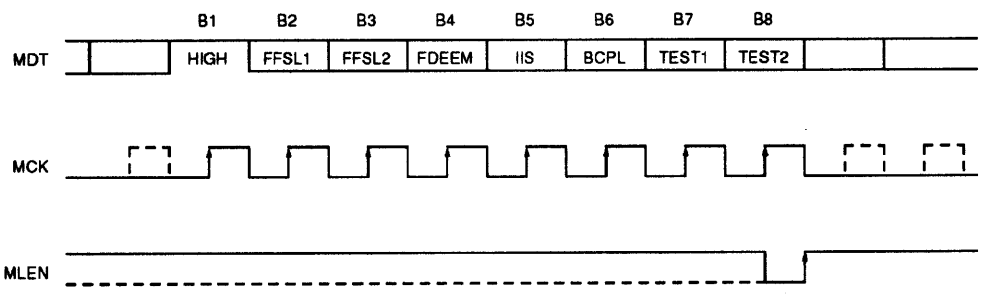


Figure 3. Mode flag data input

Table 2. Mode flags (B1 = HIGH)

Bit	Mode flag	Description	0	1
B2	FFSL1	Deemphasis frequency select bit	See table 3.	
B3	FFSL2			
B4	FDEEM	Deemphasis ON/OFF select	Deemphasis is OFF.	Deemphasis is ON.
B5	IIS	IIS (64fs BCKI) mode select	Normal format data (data at end of channel time, LRCI is HIGH for the left channel.)	IIS format data (64fs BCKI)
B6	BCPL	BCKI polarity select	Data read on rising edge of BCKI.	Data read on falling edge of BCKI.
B7	TEST1	Test mode select	Tie LOW for normal operation.	
B8	TEST2			

Note that all mode flags are LOW after the devices are reset.

Deemphasis Filter

The deemphasis filter is an infinite impulse response (IIR) filter with variable filter coefficients that reproduces the gain and phase characteristics of an analog filter. The filter coefficients can be set to one of three sampling rates as shown in table 3. Deemphasis is turned ON and OFF by DEEM when MCOM is LOW and by the FDEEM flag when MCOM is HIGH.

Table 3. Deemphasis selection

MCOM is LOW.		MCOM is HIGH.		Deemphasis frequency (kHz)
FSEL2	FSEL1	FFSL2	FFSL1	
LOW	LOW	0	0	44.1
LOW	HIGH	0	1	
HIGH	LOW	1	0	48.0
HIGH	HIGH	1	1	32.0

Attenuator

The 7-bit attenuation coefficient data, DATT, is loaded by the SM5872A/B as shown in figure 4.

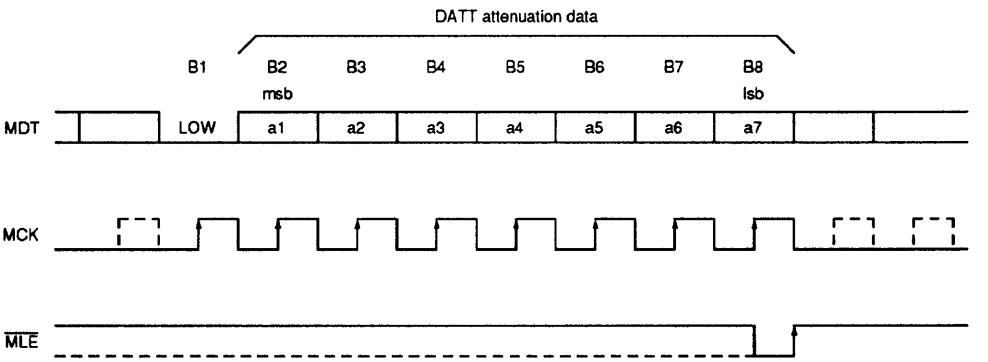


Figure 4. Attenuation data

The output signals are attenuated by multiplying the signal data by the contents of the built-in 7-bit attenuation up/down counter. If the counter value equals the DATT attenuation coefficient, the gain for each channel is given by the following equation.

$$\text{Gain} = 20 \times \log_{10} (1 - \text{DATT}/127) \text{ dB}$$

Both channels are muted completely when the DATT coefficient is 127. Upon reset, DATT is set to zero, corresponding to the maximum gain of 0 dB.

When a new DATT attenuation coefficient is loaded, the gain for each channel ramps up or down to the new level set by the coefficient as shown in

figure 5. If another attenuation coefficient is loaded before this new level has been reached, the gain ramps in the direction of the newest level setting. The gain can change in this way because the current attenuation level is stored in a different register from the DATT coefficient register.

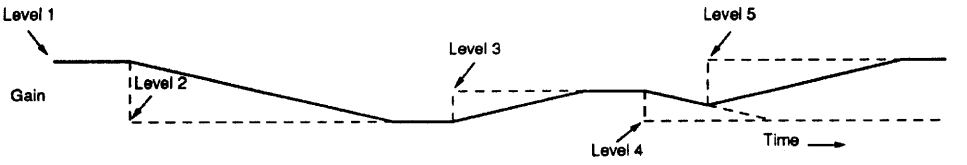


Figure 5. Attenuation example

Soft mute

When MUTEI is taken HIGH, the soft mute function using the built-in attenuation counter is enabled. The counter increments, decreasing the gain level, until the outputs are completely muted. Muting takes 1024/fs seconds, or approximately 23.2 ms when fs is 44.1 kHz.

Whe MUTEI is taken LOW again, muting is cancelled and the attenuation counter decrements, increasing the gain level. Returning to the 0 dB level also takes 1024/fs seconds as shown in figure 6.

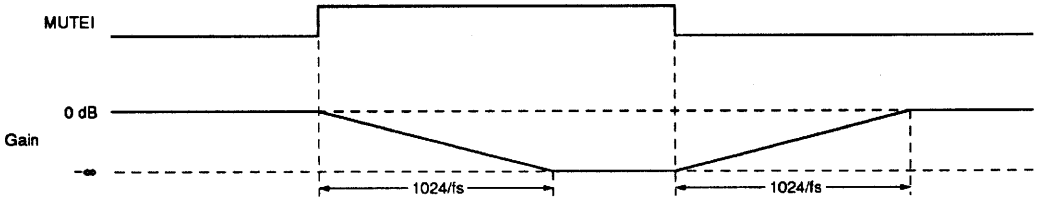


Figure 6. Soft muting

System Clock

The system clock can oscillate at 256fs, 384fs or 512fs, depending upon the device, selected by the level on CKSL. When the system clock frequency is 256fs (SM5872A only), double-speed playback is possible. The normal- and double-speed mode system clock frequencies are shown in the following tables.

SM5872A

Normal-speed mode

V_{DD} = 3.2 to 5.5 V, T_a = −20 to 70 deg. C

f_{LRCI} = fs (kHz)	f_{XTI} = f_{CKO} (MHz)	
	CKSL is HIGH.	CKSL is LOW.
44.1	22.5792	11.2896
48.0	24.576	12.288
32.0	16.384	8.192

Double-speed mode

V_{DD} = 4.5 to 5.5 V, T_a = −20 to 70 deg. C, CKSL is LOW.

f_{LRCI} = fs (kHz)	f_{XTI} = f_{CKO} (MHz)
88.2	22.5792
96.0	24.576
64.0	16.384

SM5872B

Normal-speed mode

V_{DD} = 3.2 to 5.5 V, T_a = –20 to 70 deg. C

f_{LRCI} = fs (kHz)	f_{XTI} = f_{CKO} (MHz)	
	CKSL is HIGH.	CKSL is LOW.
44.1	16.9344	Not used
48.0	18.432	Not used
32.0	12.288	Not used

As the stability and signal-to-noise ratio of the system clock greatly affects the AC analog characteristics, care should be taken to ensure that the clock is free from jitter.

The system clock can be controlled by a crystal oscillator connected as shown in figure 7. Capacitors C1 and C2 should be chosen to match the crystal oscillator.

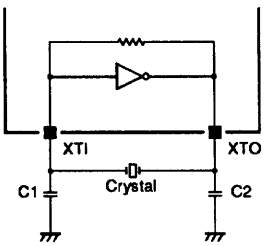


Figure 7. External crystal oscillator connection

The system clock can also be supplied externally as shown in figure 8. When using this method, XTO should be left open. As the system clock inverter has an internal feedback resistor, the external clock input can be AC coupled.

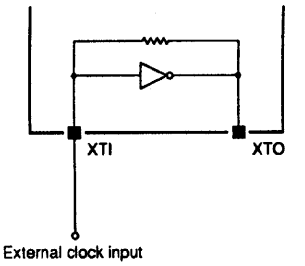


Figure 8. External system clock connection

To optimize the AC analog characteristics, use an external crystal oscillator connected to a 74HCU04 inverter to drive XTI.

Audio Data Input

The digital audio data is input on DIN in 2s-complement, msb-first, 16-bit serial data format with interleaved left- and right-channel data words.

When the IIS flag is 0, the normal data format shown in figure 9 is selected. When the IIS flag is 1, the IIS data format shown in figure 10 is selected.

The data input on DI is latched into the internal SIPO shift register on either the rising edge of BCKI (when the BCPL flag is 0) or the falling edge (when the BCPL flag is 1).

The data is latched into either the left-channel or right-channel input register on the rising and falling edges of LRCI. When the IIS flag is 0, the data is latched to the left-channel input register on the falling edge of LRCI, and when the IIS flag is 1, the data is latched to the left-channel register on the rising edge of LRCI.

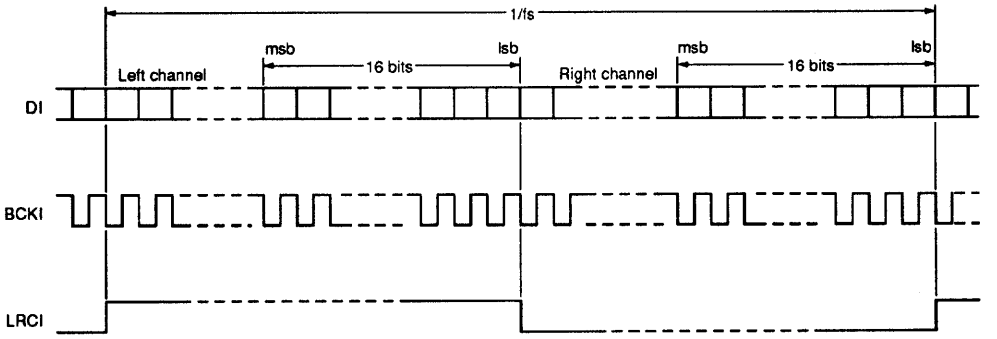


Figure 9. Normal data format (IIS = 0)

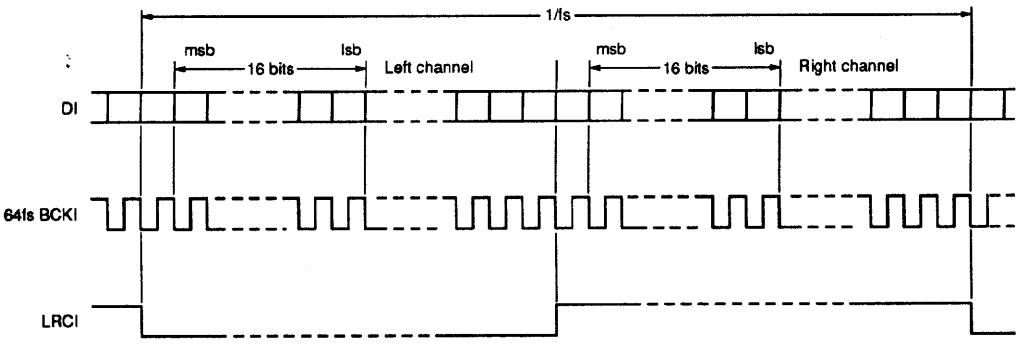


Figure 10. IIS data format (IIS = 1)

The timing of the arithmetic and output circuits is independent of the input circuits, isolating them from jitter or skew on the input circuit clocks. As a result, phase differences between LRCI, BCKI and XTI that may occur after a reset do not affect the correct operation of the device. However, the correct frequency ratio between LRCI and XTI should be maintained.

If the input data format uses word lengths greater than 16 bits (for example, 24- or 32-bit words) then the mute detector will not work unless all bits in the word other than the 16 data bits are set to 0. This condition does not have to be satisfied, however, if MUTEO is not being used.

Zero-shift Noise Shaper

The fourth-order zero-shift noise shaper (ZSNS) virtually eliminates noise in the 13-level quantized signal by altering the noise characteristic. The characteristic is altered by shifting the zeros in the *z*-plane, moving the noise out of the audio band so it is then removed by the output filters.

The ZSNS suppresses noise in a frequency range exceeding twice the audio bandwidth for a 32fs oversampled signal, and over almost the entire audio bandwidth for a 16fs oversampled signal. A theoretical characteristic is shown in figure 11, calculated by converting the data back into its original form, before the PWM output stage. Note that when CKSL is LOW, the frequency values should be halved.

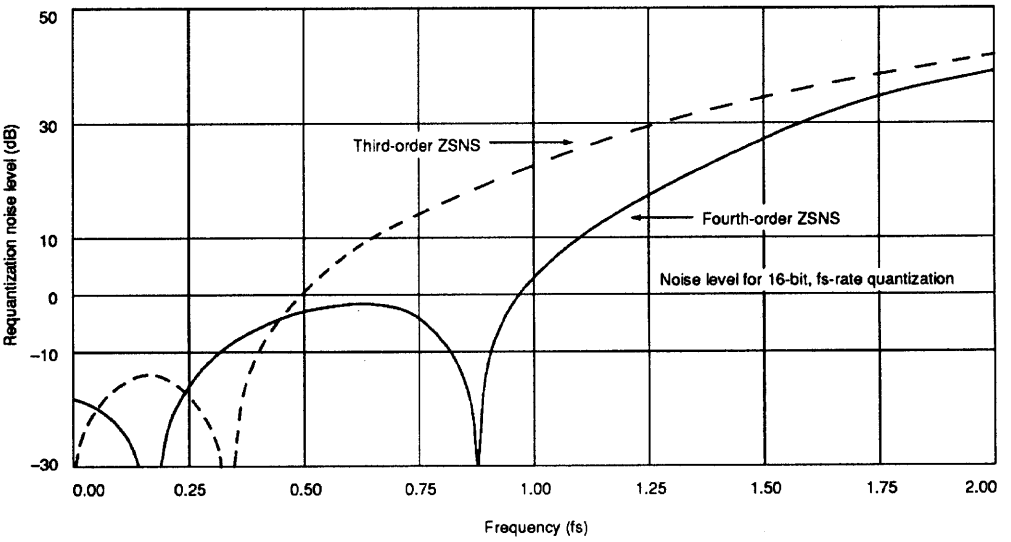


Figure 11. Requantizer noise characteristic

Pulsewidth Modulation Waveforms

The signals output by the ΣDECO SM5872A/B are quasi-symmetrical. When the PWM outputs produce odd-valued output levels, the individual output signals are not symmetrical about the center of the output pulses, however, the difference signals (LO – LON) and (RO – RON) are symmetrical as shown in figure 12. Even-valued output signals have symmetrical waveforms. Using this output method, the SM5872A/B can operate at half the clock frequency required by conventional devices.

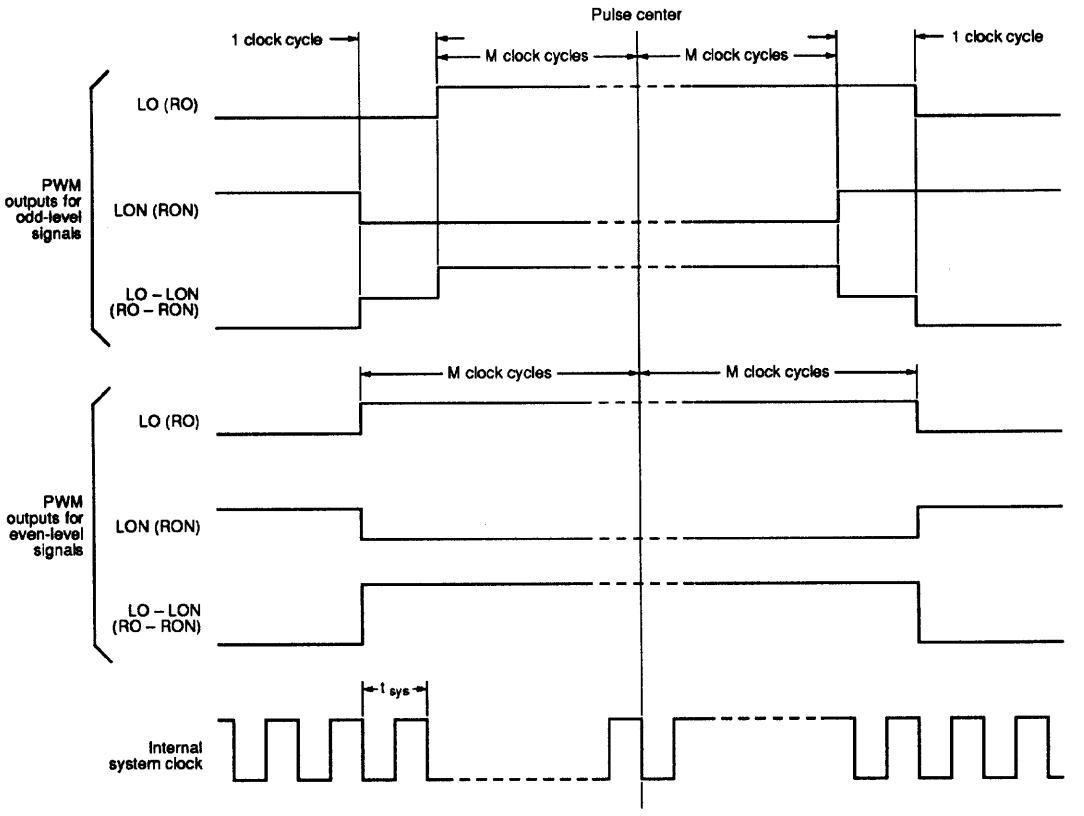


Figure 12. Pulsewidth modulation waveforms

Reset

The ΣDECO SM5872A/B should be reset after power-up, when MCOM changes state or when the XTI clock stops for longer than 10 µs. A LOW-level pulse on RSTN will resynchronize the ΣDECO SM5872A/B internal arithmetic and output clocks on the first rising edge of LRCI after RSTN returns HIGH as shown in 13.

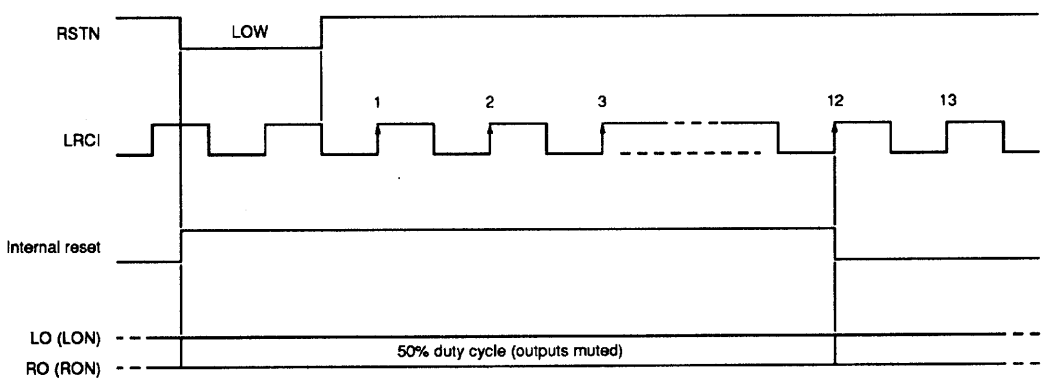


Figure 13. Reset waveforms

An external microcontroller can reset the devices at power-ON, or power-ON reset can be performed automatically if a capacitor is connected between RSTN and VSS. If the XTI and LRCI clocks are stable at power-up, then a value of 300 pF is sufficient to satisfy the reset timing requirements. If the XTI and LRCI clocks are not stable at power-up, then a value should be chosen such that RSTN goes HIGH only after both clocks have stabilized.

Upon reset, the PWM outputs are muted with a 50% duty cycle signal from the time when RSTN goes LOW until the 12th rising edge of LRCI after RSTN goes HIGH. Note that the duty cycle may change temporarily as the circuits resynchronize following the first rising edge of LRCI.

Mute Detection

MUTEO is LOW under the following three conditions.

1. While RSTN is LOW and for approximately 12 LRCI cycles after RSTN goes HIGH.
2. For approximately 12 LRCI cycles after CKSL changes state.
3. While a muted signal is detected as explained in the following paragraphs.

Note that the mute detector detects when the data bits are all 0 and does not detect when the bits are all 1.

The mute detector monitors the BCKI, DI and LRCI inputs. DI should be LOW when not transmitting data if there are more BCKI pulses than there are data bits as shown in figure 14.

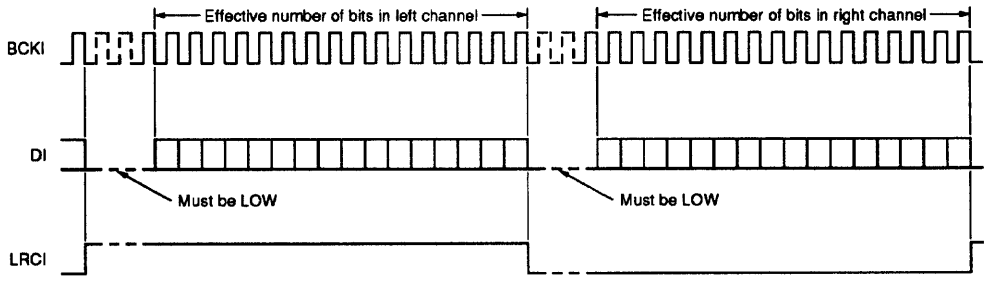


Figure 14. Input waveforms

When both channels contain zeros for 2^{19} consecutive BCKI cycles, the internal counter overflows and MUTEO goes HIGH. When a 1 is input on DI, the counter is reset and MUTEO goes LOW again.

The time to overflow the counter can be calculated using the following equation.

$$t_z = 2^{19}/(NB \times fs)$$

where NB = the number of BCKI cycles per LRCI period (typically 32 or 48).

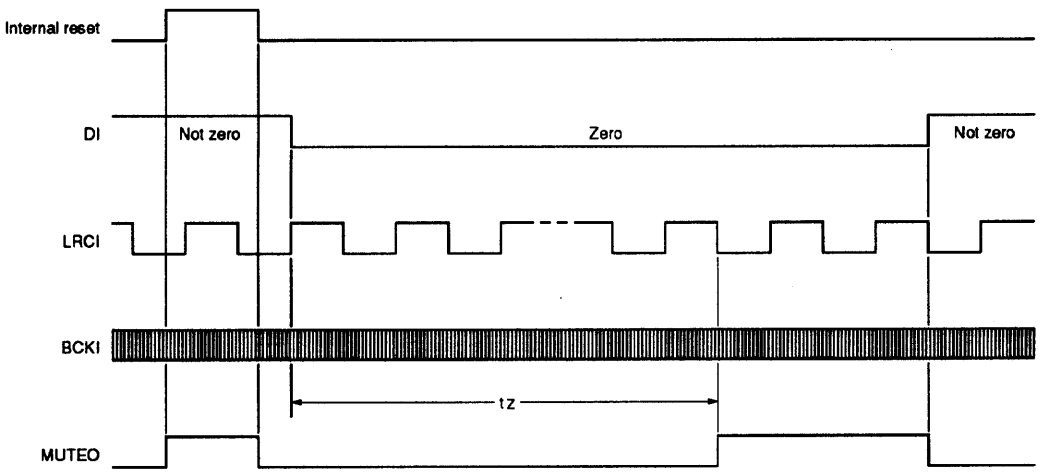


Figure 15. MUTEO output waveforms

For a 44.1 kHz sampling rate and 32 BCKI pulses per sampling period, 2^{19} bits corresponds to a mute detect time of 372 ms. When there are 48 BCKI pulses per sampling period, the mute detect time becomes 248 ms as shown in table 4.

Table 4. Mute detect time

Bit clock frequency	Mute detect time	Unit
32fs	372	ms
48fs	248	ms

Note
fs = 44.1 kHz

TIMING DIAGRAMS

Digital Audio Input Formats

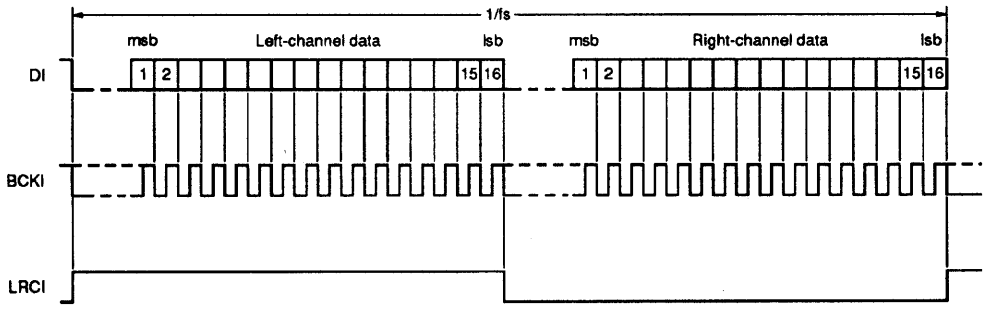


Figure 16. Normal format (IIS is 0 and BCPL is 0.)

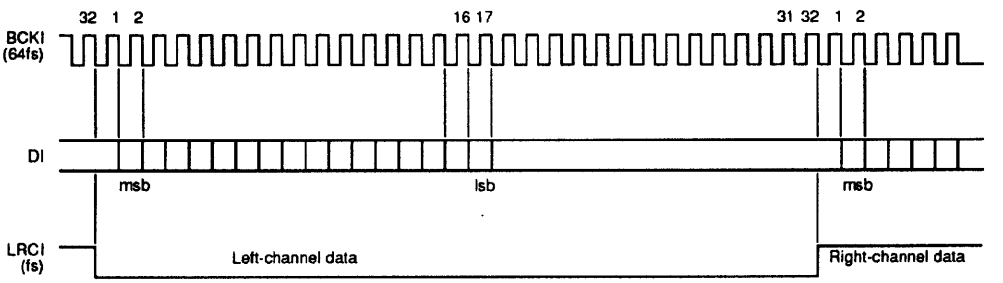


Figure 17. IIS format (IIS is 1 and BCPL is 0.)

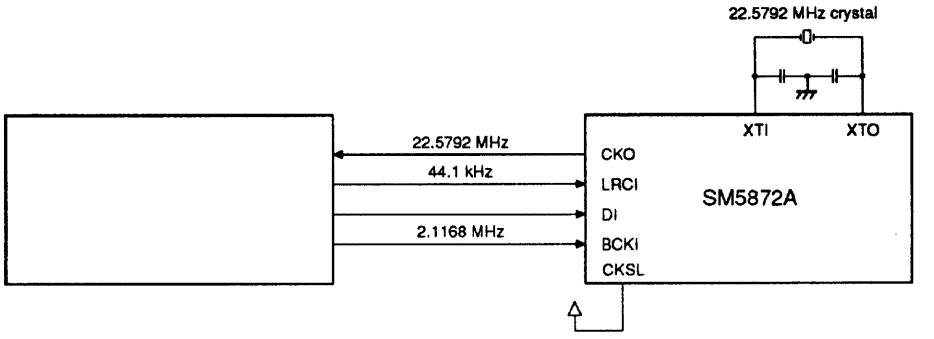
APPLICATION NOTES

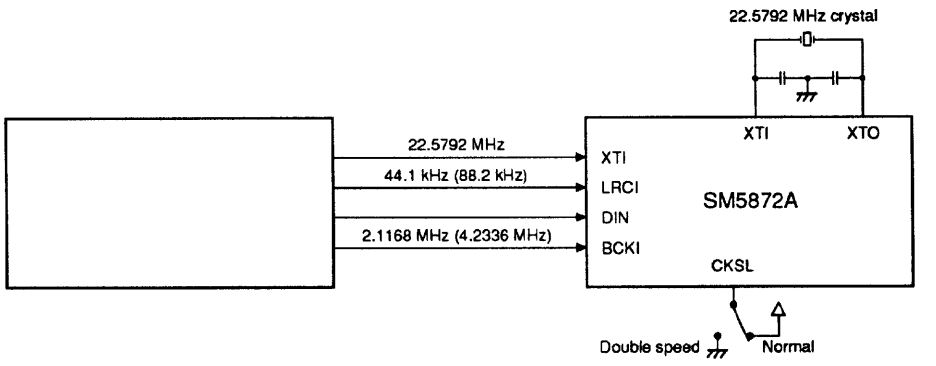
Input Interfaces

Normal data format (IIS is 0.)

Normal replay mode

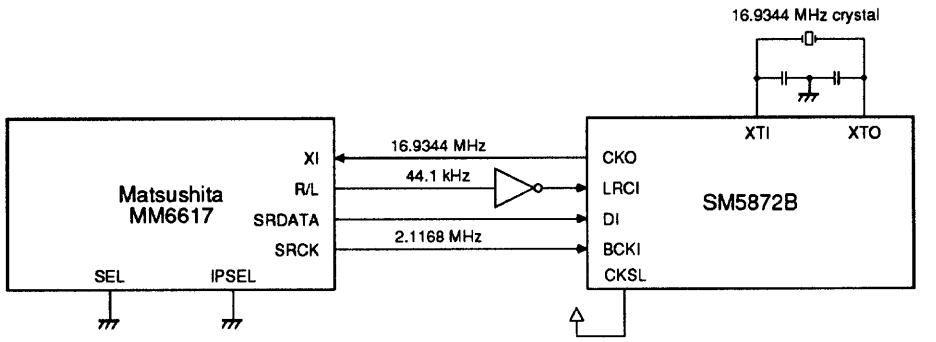
SM5872A

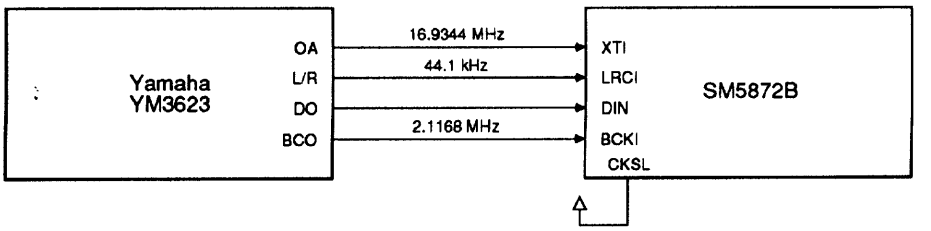




Note
The values in parentheses are for double-speed mode.

SM5872B





IIS data format (IIS is 1.)

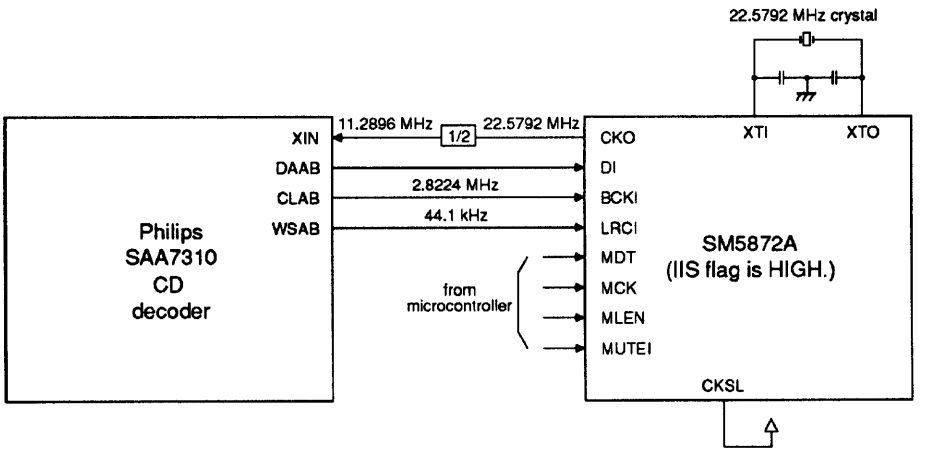


Figure 18. Phillips SAA7310 interface

Output Interfaces

In the following figures, only the left channel has been shown to avoid duplication.

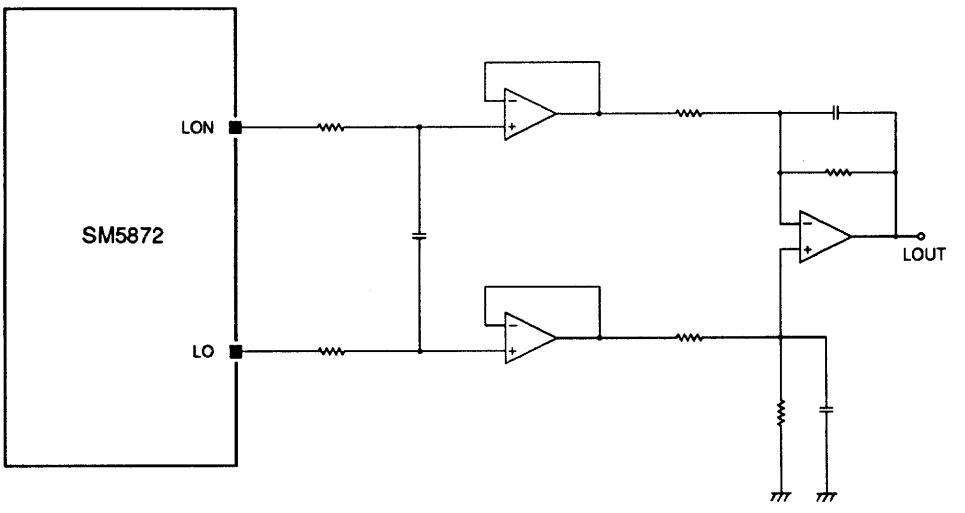


Figure 19. Output interface 1

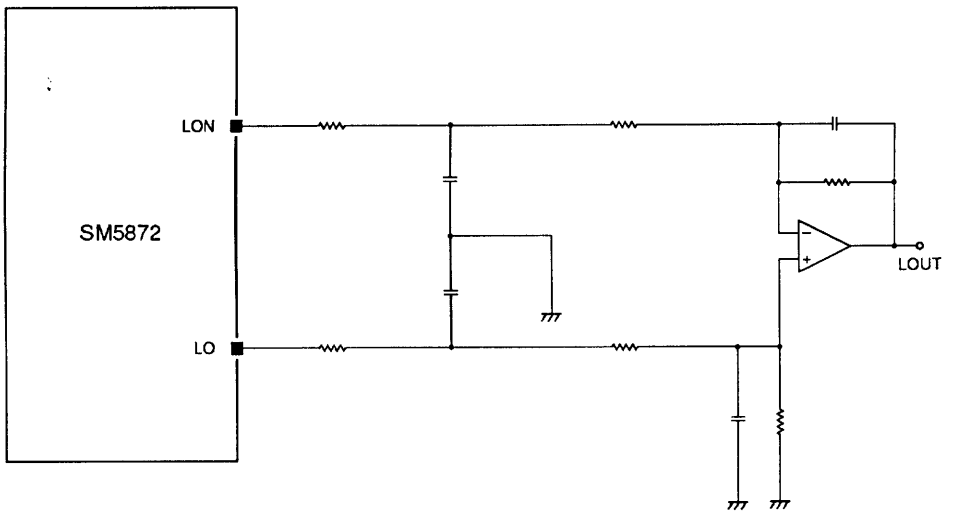


Figure 20. Output interface 2

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