

## OVERVIEW

The SM5878AM/AV is a 3rd-order  $\Sigma\Delta$ , 2-channel D/A converter LSI for digital audio reproduction equipment. It also incorporates an 8-times oversampling digital filter and analog, post-converter lowpass filters.

The SM5878AM/AV has digital deemphasis filter, attenuator, and soft mute circuits built-in. Double-speed operation and low-voltage operation are also supported.

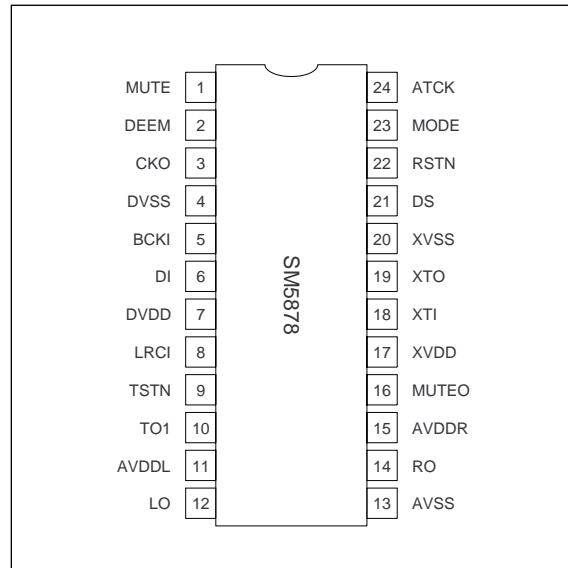
SM5878AM/AV D/A converter incorporates 3rd-order  $\Sigma\Delta$  modulator and DEM (Dynamic Element Mating) circuits for high performance, even in the presence of clock jitter.

The SM5878AM/AV operates from a 4.5 to 5.5 V supply, and is available in 24-pin SSOP or VSOPs.

## FEATURES

- 4.5 to 5.5 V operating supply voltage range
- 44.1 kHz sampling frequency
- Normal (384fs) and double-speed (192fs), 16.9344 MHz system clock
- 16.9344 MHz crystal oscillator circuits built-in
- 16-bit, MSB first, rear-packed serial data input format ( $\leq 64$ fs bit clock)
- 8-times oversampling digital filter
  - 32 dB stopband attenuation
  - $\pm 0.05$  dB passband ripple
- Deemphasis filter operation
  - 36 dB stopband attenuation
  - $-0.09$  to  $+0.23$  dB deviation from ideal deemphasis filter characteristics
- Attenuator
  - 6-bit attenuator (64 steps)
  - Soft mute function when MODE is HIGH (approx. 1024/fs total muting time)
- Built-in infinity-zero detector
- $\Sigma\Delta$  2-channel D/A converter
  - 3rd-order noise shaper
  - 32fs oversampling (16fs for double-speed mode)
- 2nd-order analog, post-converter lowpass filters built-in
- 24-pin SSOP/VSOP
- Molybdenum-gate CMOS process

## PINOUT



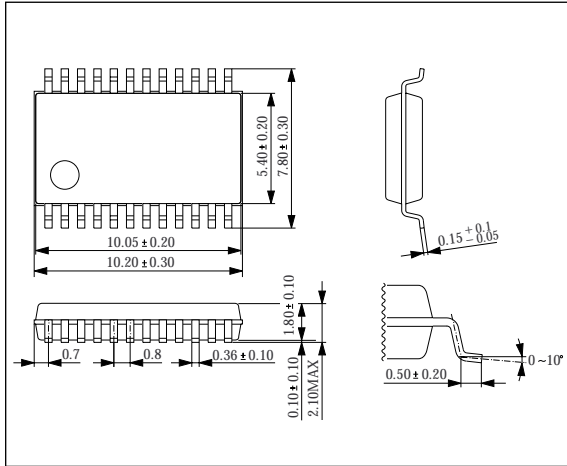
## ORDERING INFORMATIONS

DEVICE	PACKAGE
SM5878AM	24 - pin SSOP
SM5878AV	24 - pin VSOP

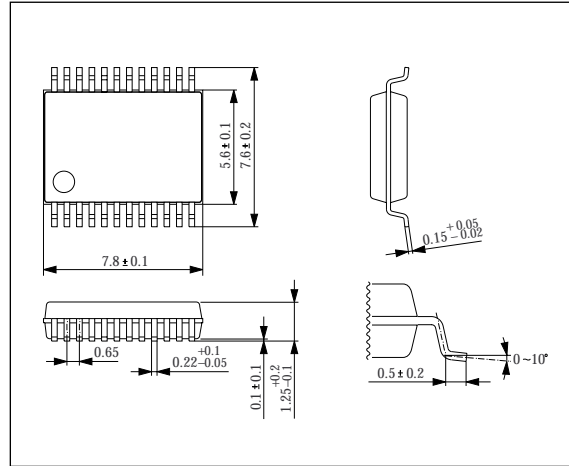
**PACKAGE DIMENSIONS**

Unit: mm

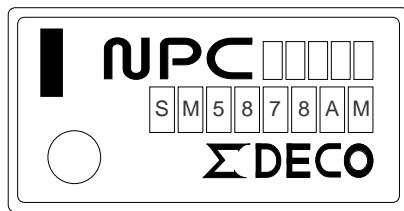
**24-pin SSOP**



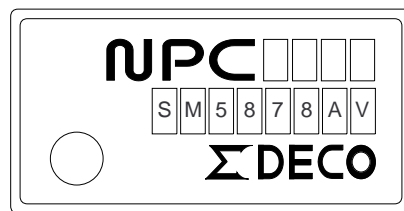
**24-pin VSOP**



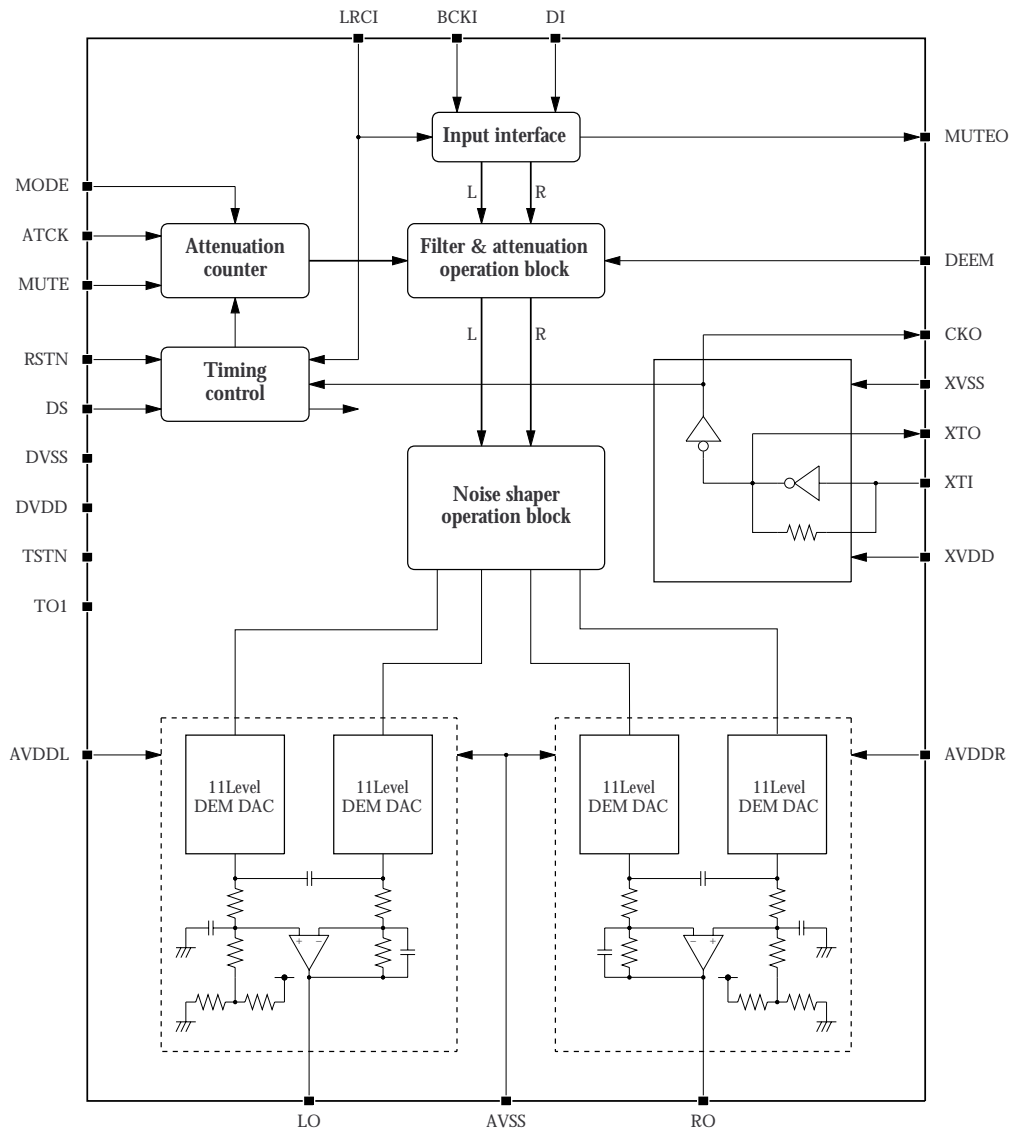
**Package Marking**



**Package Marking**



**BLOCK DIAGRAM**



**PIN DESCRIPTION**

Number	Name	I/O	Description
1	MUTE	Ip	When MODE is HIGH: Soft mute ON/OFF control. Mute is active when HIGH. When MODE is LOW: Attenuator level direction control. The attenuator direction is down when HIGH.
2	DEEM	Ip	Deemphasis control. Deemphasis is ON when HIGH, and OFF when LOW.
3	CKO	O	16.9344 MHz clock output
4	DVSS	-	Digital ground
5	BCKI	Ip	Bit clock input
6	DI	Ip	Serial data input
7	DVDD	-	Digital supply
8	LRCI	Ip	Input sample data rate (fs) clock input pin. Left-channel input when HIGH, and right-channel input when LOW.
9	TSTN	Ip	Test pin. Test mode when LOW.

## SM5878AM/AV

Number	Name	I/O	Description
10	TO1	O	Test output 1. Normally LOW.
11	AVDDL	-	Left-channel analog supply
12	LO	O	Left-channel analog output
13	AVSS	-	Analog ground
14	RO	O	Right-channel analog output
15	AVDDR	-	Right-channel analog supply
16	MUTEO	O	Infinity-zero detection output
17	XVDD	-	Crystal oscillator supply
18	XTI	I	Crystal oscillator or 16.9344 MHz external clock input
19	XTO	O	Crystal oscillator output
20	XVSS	-	Crystal oscillator ground
21	DS	Ip	Double/Normal-speed mode select. Double-speed mode when HIGH.
22	RSTN	Ip	Reset pin. Reset when LOW.
23	MODE	Ip	Soft mute/attenuator mode select. Soft mute mode when HIGH.
24	ATCK	Ip	Attenuator level setting clock. Disabled when MODE is HIGH.

## SPECIFICATIONS

### Absolute Maximum Ratings

$DV_{SS} = AV_{SS} = XV_{SS} = 0\text{ V}$ ,  $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Rating	Unit
Supply voltage range	$DV_{DD}$ , $AV_{DD}$ , $XV_{DD}$	-0.3 to 7.0	V
Input voltage range <sup>1</sup>	$V_{IN1}$	$DV_{SS} - 0.3$ to $DV_{DD} + 0.3$	V
XTI input voltage range	$V_{IN}$	$XV_{SS} - 0.3$ to $XV_{DD} + 0.3$	V
Storage temperature range	$T_{stg}$	-55 to 125	°C
Power dissipation	$P_D$	250	mW
Soldering temperature	$T_{sld}$	255	°C
Soldering time	$t_{sld}$	10	s

1. Pins MUTE, DEEM, BCKI, DI, LRCI, TSTN, DS, RSTN, MODE and ATCK.  
Also applicable during supply switching.

### Recommended Operating Conditions

$DV_{SS} = AV_{SS} = XV_{SS} = 0\text{ V}$ ,  $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Rating	Unit
Supply voltage range	$DV_{DD}$ , $AV_{DD}$ , $XV_{DD}$	4.5 to 5.5	V
Supply voltage variation	$DV_{DD} - XV_{DD}$ , $DV_{DD} - AV_{DD}$ , $XV_{DD} - AV_{DD}$ , $DV_{SS} - XV_{SS}$ , $DV_{SS} - AV_{SS}$ , $XV_{SS} - AV_{SS}$	±0.1	V
Operating temperature range	$T_{opr}$	-40 to 85	°C

note) Since  $DV_{DD}$ ,  $XV_{DD}$ ,  $AV_{DDL}$ , and  $AV_{DDR}$  are connected via the LSI substrate, current may flow if potential difference occurs among them.

## DC Electrical Characteristics

$DV_{SS} = AV_{SS} = XV_{SS} = 0\text{ V}$ ,  $DV_{DD} = AV_{DD} = XV_{DD} = 4.5\text{ to }5.5\text{ V}$ ,  $AV_{DD} = AV_{DDL} = AV_{DDR}$ ,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD digital supply current <sup>1</sup>	$I_{DD}$		–	10	15	mA
XVDD system clock supply current <sup>1</sup>	$I_{DDX}$		–	1.5	3	mA
AVDD analog supply current <sup>1</sup>	$I_{DDA}$ <sup>2</sup>		–	8.5	12	mA
XTI HIGH-level input voltage	$V_{IH1}$	Clock input	$0.7XV_{DD}$	–	–	V
XTI LOW-level input voltage	$V_{IL1}$	Clock input	–	–	$0.3XV_{DD}$	V
XTI AC-coupled input voltage	$V_{INAC}$		$0.3XV_{DD}$	–	–	$V_{p-p}$
HIGH-level input voltage <sup>3</sup>	$V_{IH2}$		2.4	–	–	V
LOW-level input voltage <sup>3</sup>	$V_{IL2}$		–	–	0.5	V
HIGH-level output voltage <sup>4</sup>	$V_{OHA}$	$I_{OH} = -1\text{ mA}$	$AV_{DD} - 0.4$	–	–	V
LOW-level output voltage <sup>4</sup>	$V_{OLA}$	$I_{OL} = 1\text{ mA}$	–	–	0.4	V
CKO HIGH-level output voltage	$V_{OHC}$	$I_{OH} = -1\text{ mA}$	$DV_{DD} - 0.4$	–	–	V
CKO LOW-level output voltage	$V_{OLC}$	$I_{OL} = 1\text{ mA}$	–	–	0.4	V
XTI HIGH-level input current	$I_{IH1}$	$V_{IN} = XV_{DD}$	–	9	18	$\mu\text{A}$
XTI LOW-level input current	$I_{IL1}$	$V_{IN} = 0\text{ V}$	–	9	18	$\mu\text{A}$
LOW-level input current <sup>4</sup>	$I_{IL2}$	$V_{IN} = 0\text{ V}$	–	9	18	$\mu\text{A}$
Input leakage current <sup>4</sup>	$I_{LH}$	$V_{IN} = DV_{DD}$	–	–	1.0	$\mu\text{A}$

1.  $DV_{DD} = AV_{DD} = XV_{DD} = 5\text{ V}$ , DS = 5 V (double speed), XTI clock input frequency  $f_{XTI} = 16.9344\text{ MHz}$ , no output load.

2.  $I_{DDA}$  is the total current.

3. Pins MUTE, DEEM, BCKI, DI, LRCI, TSTN, DS, RSTN, MODE and ATCK.

4. Pins TO1 and MUTE0.

## AC Electrical Characteristics

### System clock (XTI)

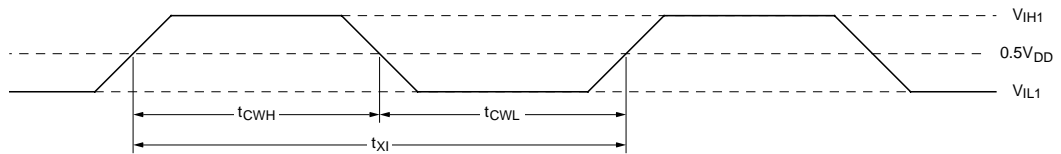
#### Crystal Oscillator

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	$f_{osc}$	4.0	16.9344	20.0	MHz

**External clock input**

Parameter	Symbol	Rating			Unit
		min	typ	max	
HIGH-level clock pulsewidth	$t_{CWH}$	20.0	29.5	125	ns
LOW-level clock pulsewidth	$t_{CWL}$	20.0	29.5	125	ns
Clock pulse cycle	$t_{XI}$	50.0	59.0	250	ns

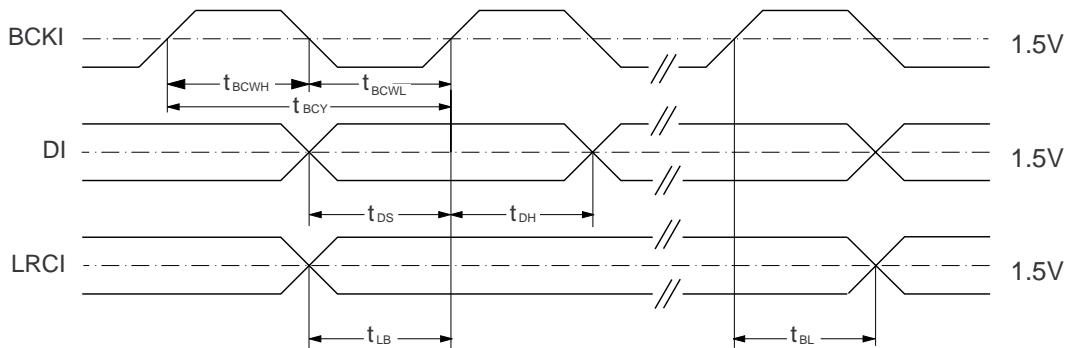
**XTI input clock**



**Serial input (BCKI, DI, LRCI)**

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	$t_{BCWH}$	50	-	-	ns
BCKI LOW-level pulsewidth	$t_{BCWL}$	50	-	-	ns
BCKI pulse cycle	$t_{BCY}$	$6t_{XI}$	-	-	ns
DI setup time	$t_{DS}$	50	-	-	ns
DI hold time	$t_{DH}$	50	-	-	ns
Last BCKI rising edge to LRCI edge	$t_{BL}$	50	-	-	ns
LRCI edge to first BCKI rising edge	$t_{LB}$	50	-	-	ns

**Serial input timing**

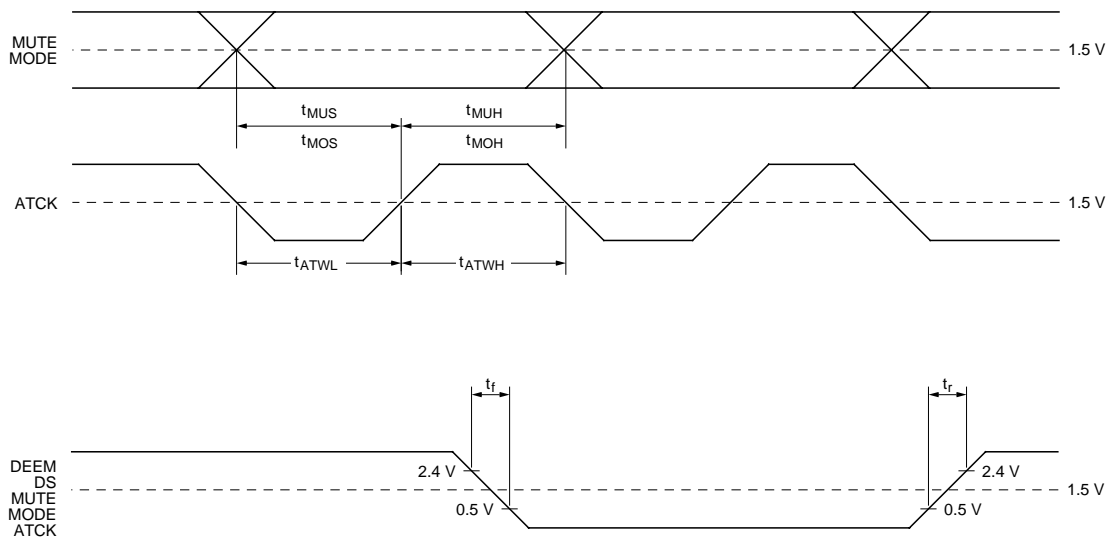


**Control input (MUTE, MODE, ATCK, DEEM, DS)**

Parameter	Symbol	Rating			Unit
		min	typ	max	
ATCK LOW-level pulsewidth	$t_{ATWL}$	$0.5/f_s^1$	-	-	$\mu s$
ATCK HIGH-level pulsewidth	$t_{ATWH}$	$0.5/f_s^1$	-	-	$\mu s$
MUTE setup time	$t_{MUS}$	100	-	-	ns
MUTE hold time	$t_{MUH}$	100	-	-	ns
MODE setup time	$t_{MOS}$	100	-	-	ns
MODE hold time	$t_{MOH}$	100	-	-	ns
Rise time	$t_r$	-	-	50	ns
Fall time	$t_f$	-	-	50	ns

1.  $f_s$  is LRCI clock frequency.

**Control input timing**



**Reset Input (RSTN)**

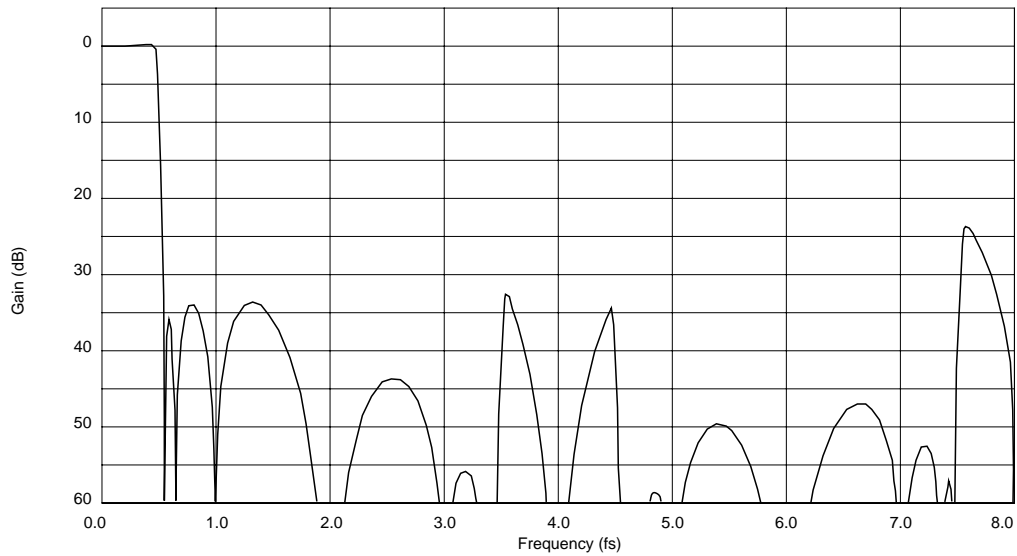
Parameter	Symbol	Rating			Unit
		min	typ	max	
RSTN LOW-level pulsewidth after supply rising edge	$t_{RSTN}$	50	-	-	ns

### Theoretical Filter Characteristics

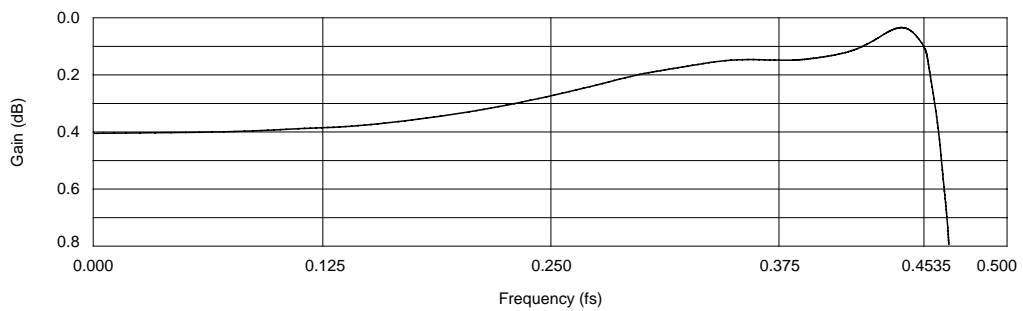
#### Deemphasis OFF overall characteristics

Parameter	Frequency band		Attenuation (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Passband ripple	0 to 0.4535fs	0 to 20.0 kHz	-0.05	-	+0.05
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	32	-	-
Built-in analog LPF compensation	0.4535fs	20.0 kHz	-	-0.34	-

#### Overall frequency characteristic (deemphasis OFF)



#### Passband characteristic (deemphasis OFF)

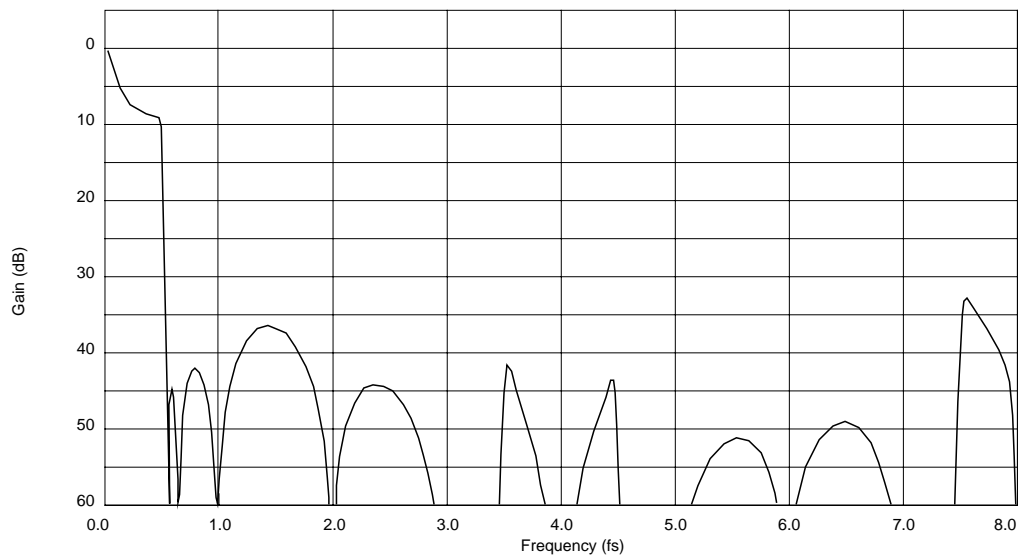




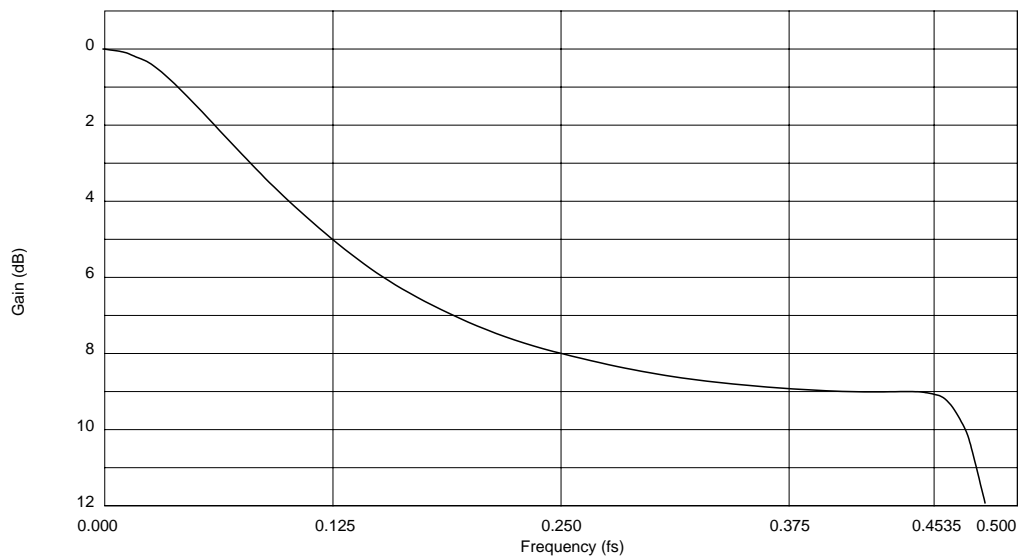
**Deemphasis ON overall characteristics**

Parameter	Frequency band		Attenuation (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Deviation from ideal deemphasis filter characteristics	0 to 0.4535fs	0 to 20.0 kHz	-0.09	-	+0.23
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	36	-	-
Built-in analog LPF compensation	0.4535fs	20.0 kHz	-	-0.34	-

**Overall frequency characteristic (deemphasis ON)**



**Passband characteristic (deemphasis ON)**



## AC Analog Characteristics

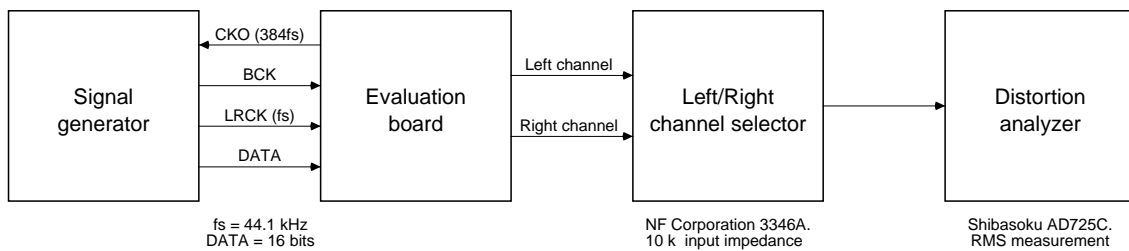
Normal-voltage:  $DV_{SS} = AV_{SS} = XV_{SS} = 0\text{ V}$ ,  $DV_{DD} = AV_{DD} = XV_{DD} = 5\text{ V}$ ,  $AV_{DD} = AV_{DDL} = AV_{DDR}$ ,  $DS = 0\text{ V}$ ,  $DEEM = 0\text{ V}$ , crystal oscillator frequency  $f_{OSC} = 16.9344\text{ MHz}$ ,  $T_a = 25\text{ °C}$

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	1 kHz, 0 dB	–	0.003	0.006	%
LSI output level	$V_{out1}$	1 kHz, 0 dB	1.2	1.3	1.4	$V_{rms}$
Evaluation board output level	$V_{out2}$	1 kHz, 0 dB	–	1.3	–	$V_{rms}$
Dynamic range	D.R	1 kHz, –60 dB	92	98	–	dB
Signal-to-noise ratio <sup>1</sup>	S/N	1 kHz, 0/–∞ dB	94	100	–	dB
Channel separation	Ch. Sep	1 kHz, –∞/0 dB	91	97	–	dB

1. Signal-to-noise is measured following a device reset, with DATA = 0 (DI = LOW). Under these conditions, the signal-to-noise ratio includes noise-shaper noise.

## Measurement Circuit and Conditions

### Measurement circuit block diagram

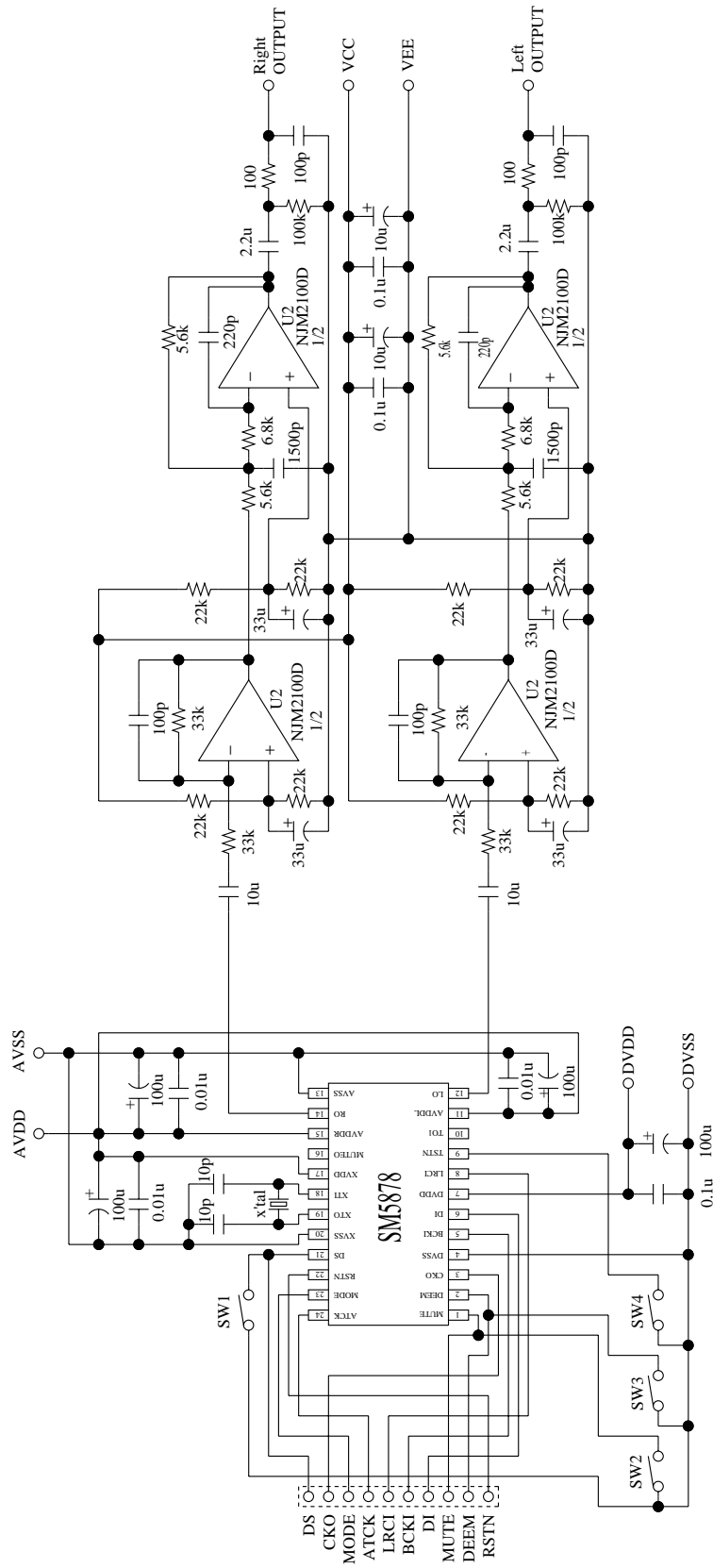


### Measurement conditions

Parameter <sup>1</sup>	Symbol	3346A left/right-channel selector switch	AD725C distortion analyzer with built-in filter
Total harmonic distortion	THD + N	THRU	20 kHz lowpass filter ON 400 Hz highpass filter OFF
Output level	$V_{out}$		
Dynamic range	DR	D-RANGE	20 kHz lowpass filter ON 400 Hz highpass filter OFF JIS A filter ON
Signal-to-noise ratio	S/N	THRU	
Channel separation	Ch. Sep	THRU	

1. Pins LO and RO should have an output load of 10 k $\Omega$  (min).

Measurement circuit



## FUNCTIONAL DESCRIPTION

### System Clock/Speed Switching (XTI, XTO, CKO, DS)

The system clock on XTI can be set to run at one of two speeds, 384fs (normal speed) or 192fs (double-speed), where fs is the input frequency on LRCI. The speed for CD playback is set by the input level on DS, as shown in table 1. The system clock should be fixed at 16.9344 MHz.

Table 1. System clock select

Parameter	Symbol	DS	
		LOW (normal speed)	HIGH (double speed)
XTI input clock frequency	$f_{XI}$ (= $1/t_{XI}$ )	384fs	192fs
CD playback XTI frequency	$f_{XI}$	16.9344 MHz at fs = 44.1 kHz	16.9344 MHz at fs = 88.2 kHz
CKO output clock frequency	$f_{CO}$	384fs	192fs
Internal system clock period	$T_{SYS}$	$t_{XI}$	$t_{XI}$

Note that the input clock accuracy and signal-to-noise ratio greatly influence the AC analog characteristics.

The system clock can be controlled by a crystal oscillator comprising a crystal connected between XTI and XTO and the built-in CMOS inverter. Alternatively, an external system clock can be input on XTI. As the internal CMOS inverter has a feedback resistor, the external clock can be AC coupled to XTI. The system clock is output on CKO.

### System Reset (RSTN)

The device should be reset in the following cases.

- At power ON
- When LRCI and/or the system clock XTI stop, or other abnormalities occur.

The device is reset by applying a LOW-level pulse on RSTN. At system reset, the internal arithmetic operation and output timing counter are synchronized on the next LRCI rising edge, as shown in figure 1.

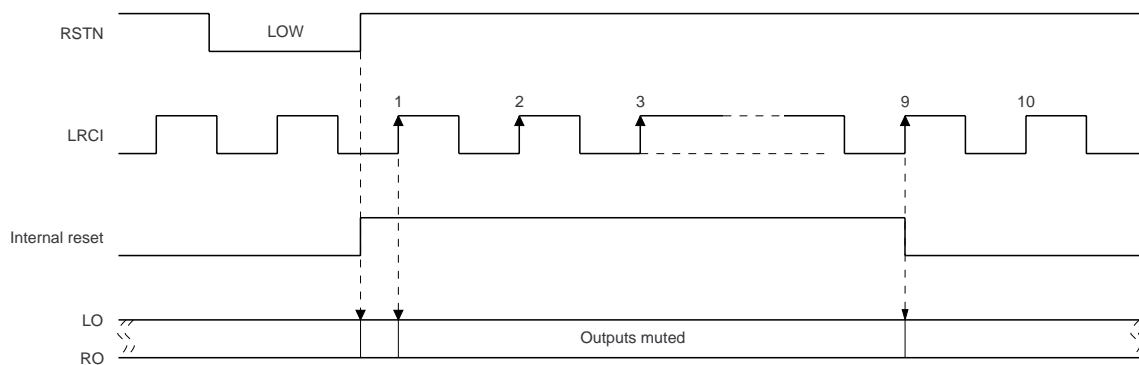


Figure 1. System reset timing

### Audio Data Input (DI, BCKI, LRCI)

The digital audio data is input on DI in MSB-first, 2s-complement, 16-bit serial format.

Serial data bits are read into the SIPO register (serial-to-parallel converter register) on the rising edge of the bit clock BCKI.

The arithmetic operation and output timing are independent of the input timing. Accordingly, after a

reset, as long as the clock frequency ratio between LRCI and the system clock XTI is maintained, phase differences between LRCI, BCKI and the system clock XTI do not affect the functional operation. Also, any jitter present on the data input clock does not appear as output pulse jitter.

The bit clock frequency on BCKI should be between 32fs and 64fs.

## Deemphasis Filter (DEEM)

The built-in digital deemphasis filter is designed to operate at 44.1 kHz. Deemphasis is ON when DEEM is HIGH, and OFF when DEEM is LOW.

## Attenuation (MODE, ATCK, MLEN)

The digital attenuation mode is selected when MODE is LOW. The attenuator operates by multiplying the internal 6-bit up/down counter's output data with the signal data.

The direction of the 6-bit up/down counter is controlled by the level on MUTE (down when MUTE is HIGH, and up when MUTE is LOW). The count is advanced on the rising edge of ATCK.

When the count reaches 0 (down) or 63 (up), the counter automatically stops.

The gain is set by the counter contents DATT as follows.

$$\text{Gain} = 20 \times \log\left(\frac{\text{DATT}}{63}\right) [\text{dB}]$$

Upon system initialization or when MODE changes state, DATT is set to 63, which corresponds to the maximum gain of 0 dB as shown in table 2.

Table 2. Attenuator gain

DATT	Gain (dB)	DATT	Gain (dB)	DATT	Gain (dB)	DATT	Gain (dB)
63	0.0	47	-2.545	31	-6.160	15	-12.465
62	-0.139	46	-2.732	30	-6.444	14	-13.064
61	-0.280	45	-2.923	29	-6.739	13	-13.708
60	-0.424	44	-3.118	28	-7.044	12	-14.403
59	-0.570	43	-3.317	27	-7.360	11	-15.159
58	-0.718	42	-3.522	26	-7.687	10	-15.987
57	-0.869	41	-3.731	25	-8.028	9	-16.902
56	-1.023	40	-3.946	24	-8.383	8	-17.925
55	-1.180	39	-4.166	23	-8.752	7	-19.085
54	-1.339	38	-4.391	22	-9.138	6	-20.424
53	-1.501	37	-4.623	21	-9.542	5	-22.007
52	-1.667	36	-4.861	20	-9.966	4	-23.946
51	-1.835	35	-5.105	19	-10.412	3	-26.444
50	-2.007	34	-5.357	18	-10.881	2	-29.966
49	-2.183	33	-5.617	17	-11.378	1	-35.987
48	-2.362	32	-5.884	16	-11.904	0	$-\infty$

### Soft Mute (SMUTE)

Soft mute mode is selected when MODE is HIGH. The up/down counter is switched to internal clock drive, and soft mute operation is controlled by MUTE only.

When MUTE goes HIGH, the up/down counter counts down. The total time to go from 0 to maximum mute is  $1024/f_s$ . This corresponds to approximately 23.2 ms at  $f_s = 44.1$  kHz.

When MUTE is LOW, soft mute is released. The attenuation counter output counts up, increasing the gain. The time taken to return to 0 dB is also  $1024/f_s$ . Soft mute operation is shown in figure 2.

Upon system initialization or when MODE changes state, mute is released, which corresponds to the maximum gain of 0 dB.

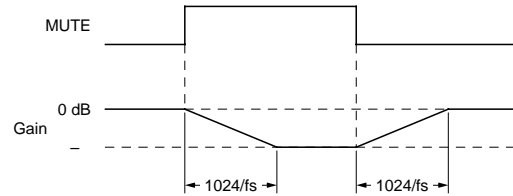


Figure 2. Soft mute operation example

### Infinity-Zero (MUTEO)

The SM5878AM/AV outputs an infinity-zero detection output signal under the following circumstances.

- From immediately after a reset input on RSTN until the initialization cycle finishes and the first data cycle occurs.

- When an infinity-zero occurs in the input data. When an infinity-zero is detected, a period of  $2^{14} \times (1/f_s) \approx 0.37$  seconds takes place before MUTEO goes HIGH.

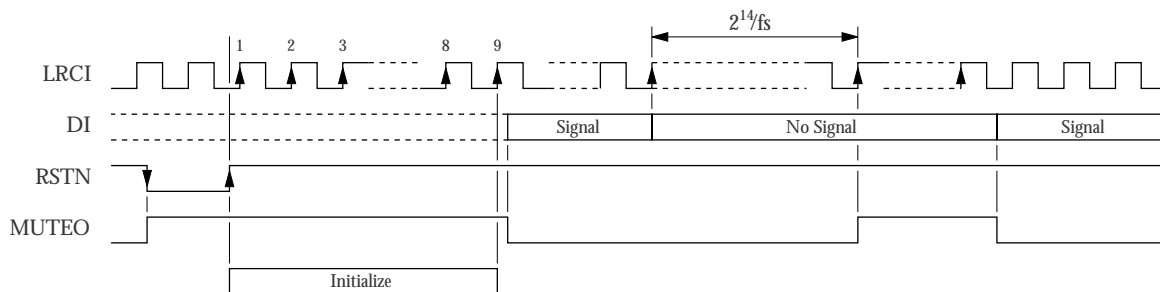
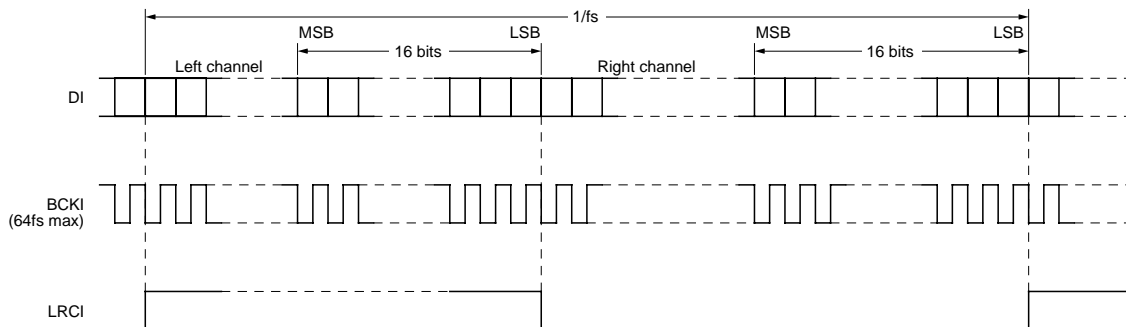


Figure 3. MUTEO output timing

## TIMING DIAGRAMS

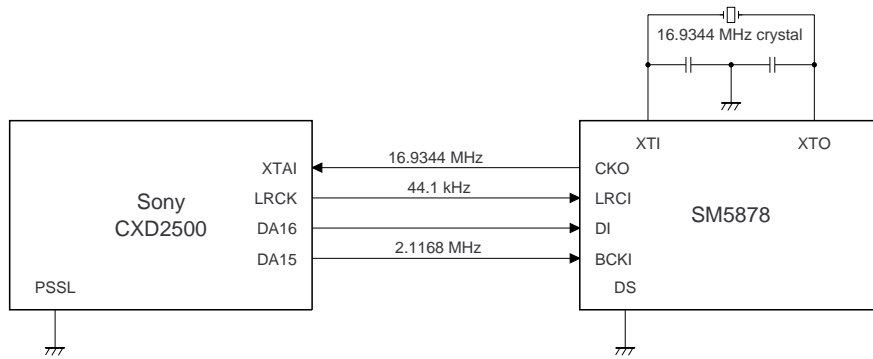
### Input Timing (DI, BCKI, LRCI)



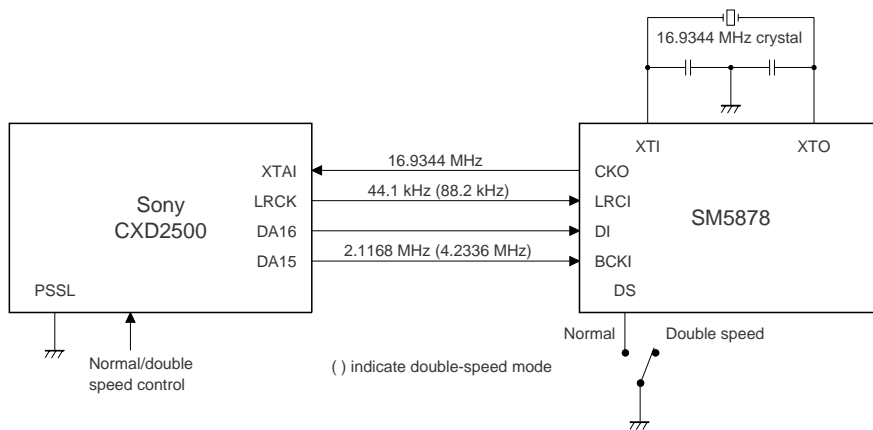
## TYPICAL APPLICATIONS

### Input Interface Circuits

#### Normal Speed



#### Double Speed



Note that the output analog characteristics and other specifications are not guaranteed for a particular format or application circuit.

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