SM5921A

8-channel Lip Sync Delay

OVERVIEW

The SM5921A is an SDRAM controller LSI for audio applications. It stores 64-fs slot 3-wire serial format audio data input at sampling frequency fs in SDRAM, and can access data at an arbitrary address to add a delay to each channel data. It also has a direct mute function to mute the audio data.

FEATURES

Functions

- System clock input
  64fs (fs = 32 to 192kHz) bit clock
- Sampling frequency: fs = 32 to 192kHz support
- Data input/output
  3-wire serial, 8-channel PCM
  64 clock/slot, word clock polarity inversion
- Direct mute function
- MCU interface: 3-wire serial
- Delay settings: sum of intrinsic delay and individual delay
  - Intrinsic delay (common to all channels, default = 0 samples, 16-sample units)
  - Individual delay (independent for each channel, default = 0 samples, 1-sample units)
    Maximum delay values
    1365.3ms @ fs = 48kHz
    682.7ms @ fs = 96kHz
    341.3ms @ fs = 192kHz
- Address shift function: ×1, ×2, ×4 support
  Delay time can be multiplied between ×1, ×2, or ×4 times without changing the delay set value.
- SDRAM interface: 16M/64M/128M (×16 devices supported)
- Package: 64-pin QFP

Structure

- Silicon-gate CMOS

Applications

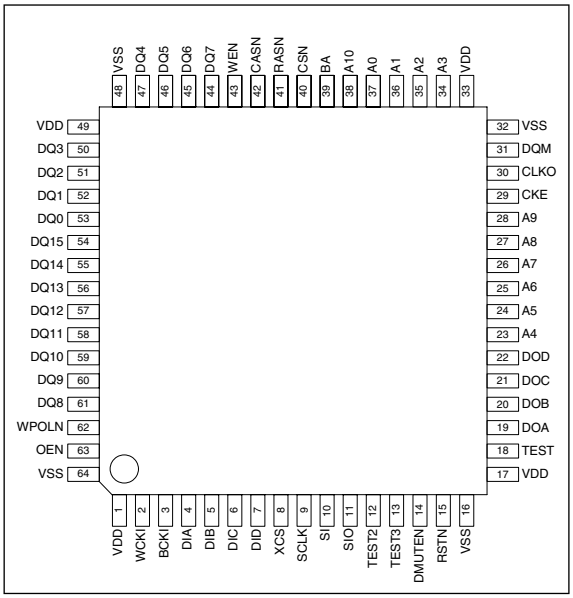
- Audio delay for multi-channel PCM signals

ORDERING INFORMATION

Device	Package
SM5921AF	64-pin QFP

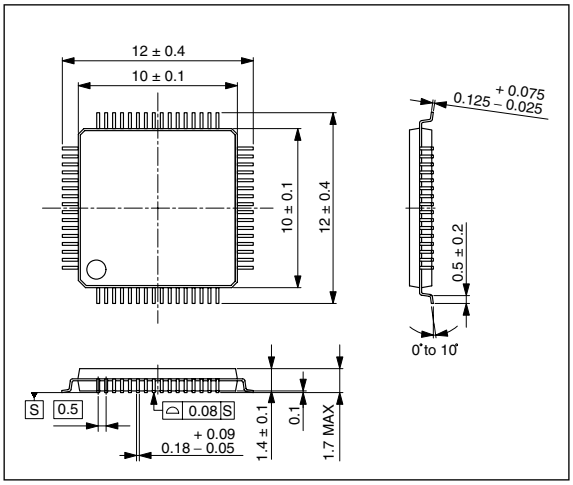
PINOUT

(Top view)



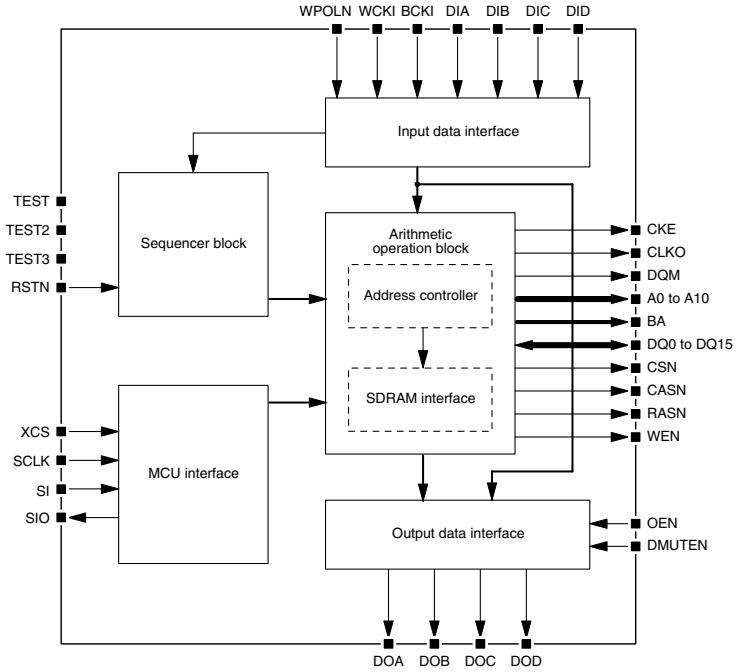
PACKAGE DIMENSIONS

(Unit: mm)
Weight: 0.35g



Note. Dimensions without tolerance are reference values.

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O*1	Function	Setting	
				HIGH	LOW
1	VDD	–	Supply pin		
2	WCKI	I	Word clock input		
3	BCKI	I	Bit clock input (64fs)		
4	DIA	I	Serial data input A		
5	DIB	I	Serial data input B		
6	DIC	I	Serial data input C		
7	DID	I	Serial data input D		
8	XCS	I	MCU latch enable input		
9	SCLK	I	MCU clock input		
10	SI	I	MCU data input		
11	SIO	Ot	MCU data output		
12	TEST2	Id	Test input pin	Test	
13	TEST3	Id	Test input pin	Test	
14	DMUTEN	Ip	Direct mute control		Mute
15	RSTN	Ip	Reset input pin		Reset
16	VSS	–	Ground pin		
17	VDD	–	Supply pin		
18	TEST	Id	Test input pin	Test	
19	DOA	Ot	Serial data output A		
20	DOB	Ot	Serial data output B		
21	DOC	Ot	Serial data output C		
22	DOD	Ot	Serial data output D		

Number	Name	I/O*1	Function	Setting	
				HIGH	LOW
23	A4	O	Address output A4		
24	A5	O	Address output A5		
25	A6	O	Address output A6		
26	A7	O	Address output A7		
27	A8	O	Address output A8		
28	A9	O	Address output A9		
29	CKE	O	SDRAM clock enable output		
30	CLKO	O	SDRAM clock output (64fs)		
31	DQM	O	DQM output		
32	VSS	–	Ground pin		
33	VDD	–	Supply pin		
34	A3	O	Address output A3		
35	A2	O	Address output A2		
36	A1	O	Address output A1		
37	A0	O	Address output A0		
38	A10	O	Address output A10		
39	BA	O	Bank address output BA		
40	CSN	O	$\overline{CS}$ output		
41	RASN	O	$\overline{RAS}$ output		
42	CASN	O	$\overline{CAS}$ output		
43	WEN	O	$\overline{WE}$ output		
44	DQ7	I/O	Data input/output DQ7		
45	DQ6	I/O	Data input/output DQ6		
46	DQ5	I/O	Data input/output DQ5		
47	DQ4	I/O	Data input/output DQ4		
48	VSS	–	Ground pin		
49	VDD	–	Supply pin		
50	DQ3	I/O	Data input/output DQ3		
51	DQ2	I/O	Data input/output DQ2		
52	DQ1	I/O	Data input/output DQ1		
53	DQ0	I/O	Data input/output DQ0		
54	DQ15	I/O	Data input/output DQ15		
55	DQ14	I/O	Data input/output DQ14		
56	DQ13	I/O	Data input/output DQ13		
57	DQ12	I/O	Data input/output DQ12		
58	DQ11	I/O	Data input/output DQ11		
59	DQ10	I/O	Data input/output DQ10		
60	DQ9	I/O	Data input/output DQ9		
61	DQ8	I/O	Data input/output DQ8		
62	WPOLEN	Ip	Word clock polarity control		Inverted
63	OEN	Id	Data output enable control	Hi-Z	Output
64	VSS	–	Ground pin		

*1. I: Input, I/O: Input/Output, O: Output, Ip: Input with pull-up resistor, Id: Input with pull-down resistor, Ot: Three-state output

ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V, VDD pin voltage = V_{DD}

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.3 to 4.6	V
Input voltage	V_I		–0.3 to 5.5	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}		–55 to 125	°C
Power dissipation	P_W		120	mW

Note. Supply ratings apply both when switching power ON or OFF.

RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V, VDD pin voltage = V_{DD}

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0	3.3	3.6	V
Operating temperature	T_{OPR}		–40	25	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{SS} = 0V, V_{DD} = 3.0 to 3.6V, Ta = –40 to 85°C

Parameter	Pins	Symbol	Conditions	Rating			Unit
				min	typ	max	
Current consumption	VDD	I_{DD}	(*A)		18	30	mA
Input voltage	(*1) (*2) (*3) (*5)	V_{IH}		2.0		V_{DD}	V
		V_{IL}		0		0.8	
Output voltage	(*4) (*5)	V_{OH}	I_{OH} = –2.0mA	V_{DD} – 0.4		V_{DD}	V
		V_{OL}	I_{OL} = 2.0mA	0		0.4	
Input leakage current	(*1) (*5)	I_{LH}	V_{IN} = V_{DD}	–1.0		1.0	µA
		I_{LL}	V_{IN} = 0V	–1.0		1.0	
Input current	(*2)	I_{IH1}	V_{IN} = V_{DD}	–1.0		1.0	µA
		I_{IL1}	V_{IN} = 0V	–90.0	–33.0	–12.5	
	(*3)	I_{IH2}	V_{IN} = V_{DD}	12.5	33.0	90.0	
		I_{IL2}	V_{IN} = 0V	–1.0		1.0	

(*A) All output pins no load, system clock frequency f_{BCKI} = 12.288MHz, input sampling frequency fs = 192kHz, supply voltage V_{DD} = 3.6V
Note. See “Pin Classification” below for description of pins.

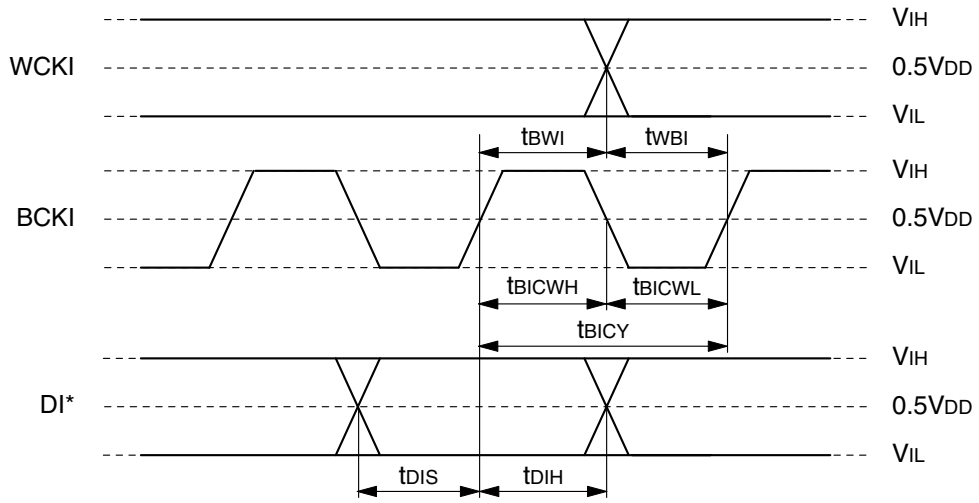
Pin classification

Symbol	Pin type	Pin name
(*1)	Inputs	WCKI, BCKI, DIA, DIB, DIC, DID, XCS, SCLK, SI
(*2)	Inputs	DMUTEN, WPOLN, RSTN
(*3)	Inputs	OEN, TEST, TEST2, TEST3
(*4)	Outputs	DOA, DOB, DOC, DOD, RASN, CASN, CSN, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, BA, WEN, CLKO, CKE, DQM, SIO
(*5)	Input/Outputs	DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7, DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, DQ15

AC Characteristics

Serial inputs (WCKI, BCKI, DI* pins)

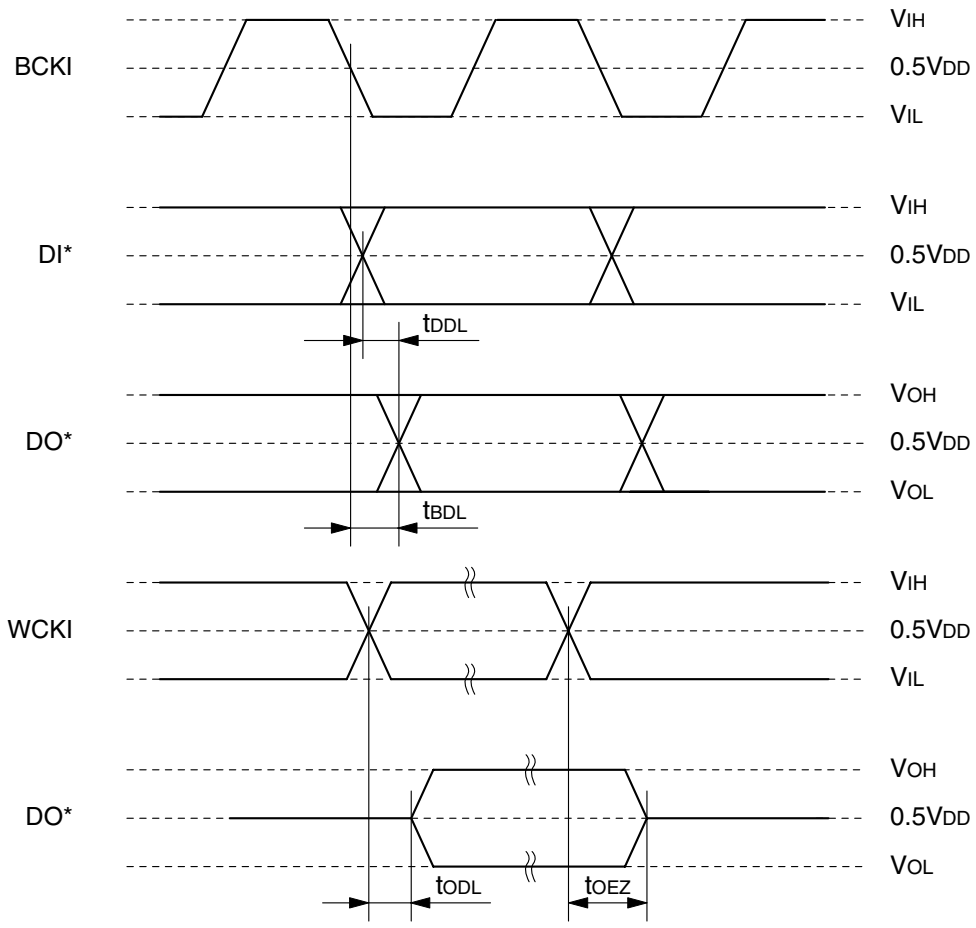
Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
WCKI cycle time	t_{WCCY}		5.2	20.8	32	µs
BCKI pulse cycle time	t_{BICY}		81.25	325.5	500	ns
BCKI HIGH-level pulsewidth	t_{BICWH}		32.5	130.2	320	ns
BCKI LOW-level pulsewidth	t_{BICWL}		32.5	130.2	320	ns
DI* setup time	t_{DIS}		20.0			ns
DI* hold time	t_{DIH}		20.0			ns
Last BCKI rising edge → WCKI edge	t_{BWI}		32.5			ns
WCKI edge → first BCKI rising edge	t_{WBI}		32.5			ns



Note. DI*: DIA, DIB, DIC, DID pins

Serial outputs (DO* pins)

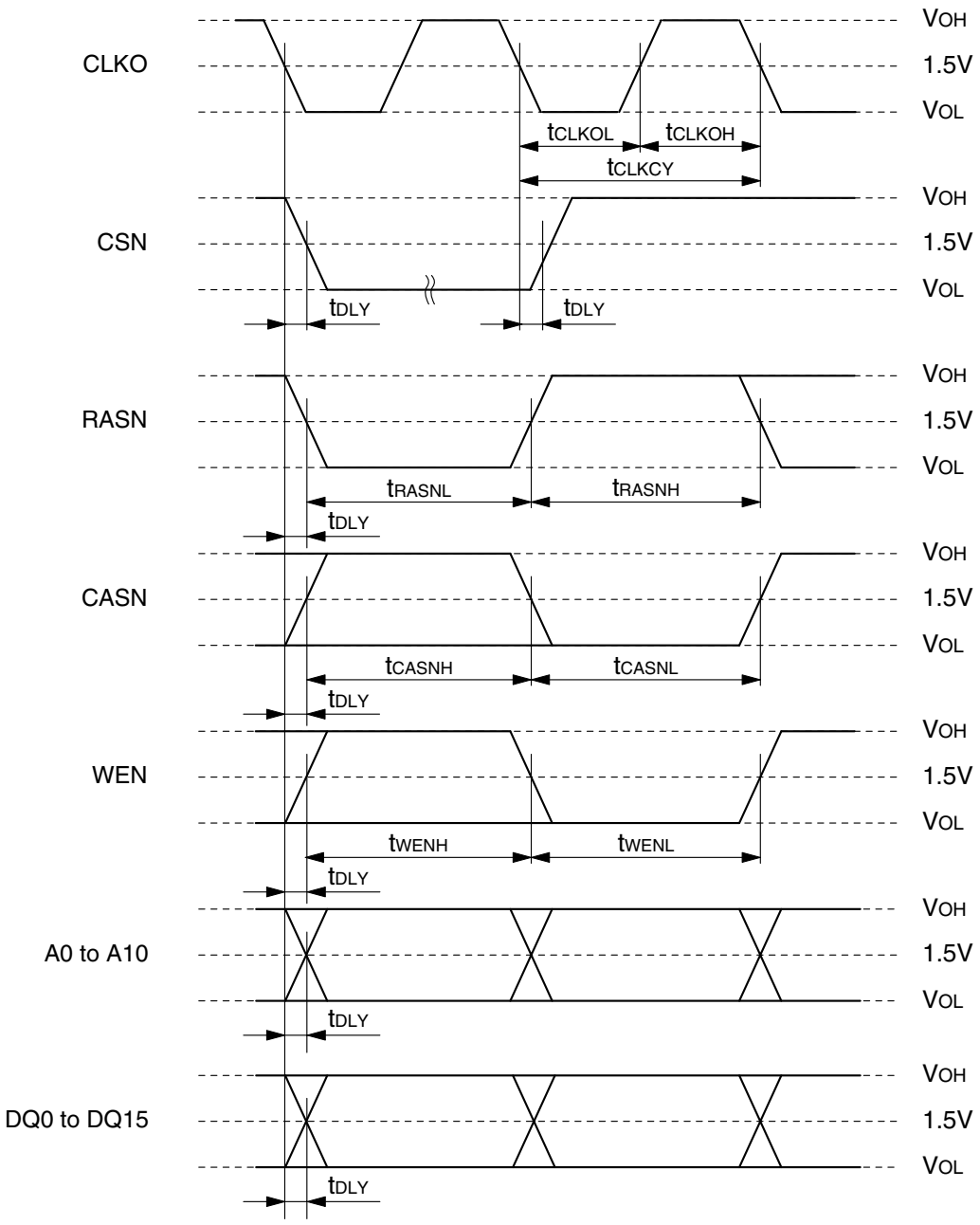
Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
BCKI to output delay	t_{BDL}	C_L = 15pF	0		20	ns
DI* to output delay	t_{DDL}	Data-through (THROU = 1), C_L = 15pF	0		20	ns
Word boundary to enable time	t_{ODL}	OEN = H → L, C_L = 15pF	0		30	ns
Word boundary to disable time	t_{OEZ}	OEN = L → H, C_L = 15pF	0		30	ns



Note. DI*: DIA, DIB, DIC, DID pins
DO*: DOA, DOB, DOC, DOD pins

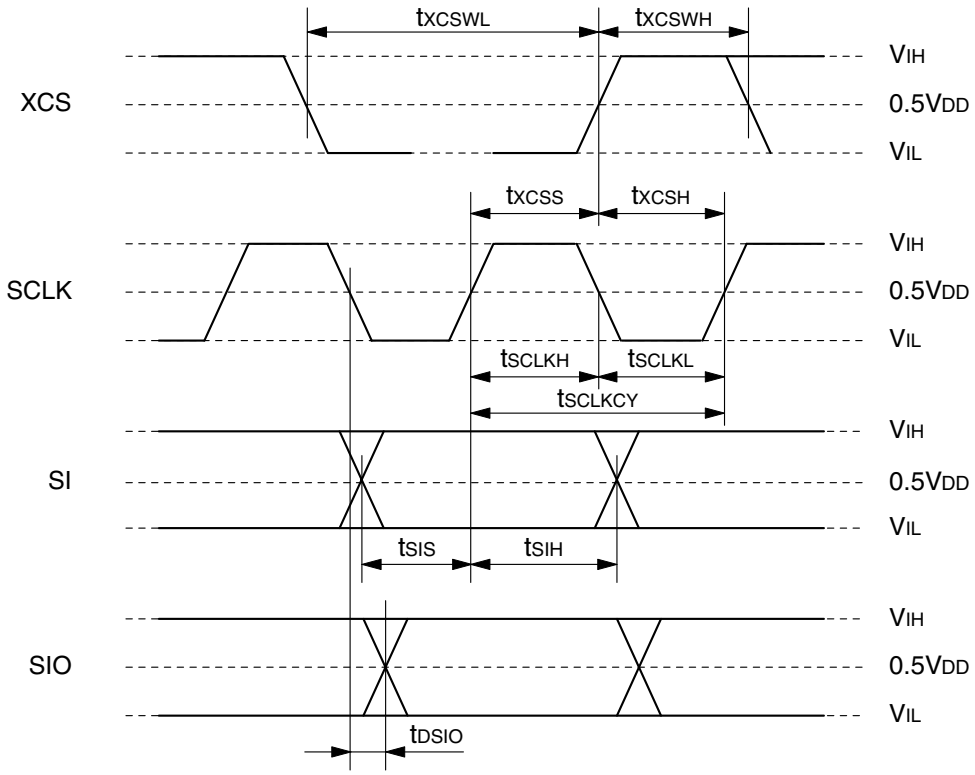
SDRAM interface (CLKO, RASN, CASN, WEN, CSN, A0 to A10, DQ0 to DQ15 pins)

Parameter		Symbol	Conditions	Rating			Unit
				min	typ	max	
CLKO pulse cycle time		t_{CLKCY}	C_L = 15pF		1		t_{BICY}
CLKO HIGH-level pulsewidth		t_{CLKOH}	C_L = 15pF		1/2		t_{BICY}
CLKO LOW-level pulsewidth		t_{CLKOL}	C_L = 15pF		1/2		t_{BICY}
RASN pulsewidth		t_{RASNH}	C_L = 15pF	1			t_{BICY}
		t_{RASNL}	C_L = 15pF	1			t_{BICY}
CASN pulsewidth		t_{CASNH}	C_L = 15pF	1			t_{BICY}
		t_{CASNL}	C_L = 15pF	1			t_{BICY}
WEN pulsewidth		t_{WENH}	C_L = 15pF	1			t_{BICY}
		t_{WENL}	C_L = 15pF	1			t_{BICY}
CLKO ↑ – CSN	Setup time	t_{CSNS}	C_L = 15pF		1/2		t_{BICY}
	Hold time	t_{CSNH}	C_L = 15pF		1/2		t_{BICY}
CLKO ↑ – RASN	Setup time	t_{RASNS}	C_L = 15pF		1/2		t_{BICY}
	Hold time	t_{RASNHO}	C_L = 15pF		1/2		t_{BICY}
CLKO ↑ – CASN	Setup time	t_{CASNS}	C_L = 15pF		1/2		t_{BICY}
	Hold time	t_{CASNHO}	C_L = 15pF		1/2		t_{BICY}
CLKO ↑ – WEN	Setup time	t_{WENS}	C_L = 15pF		1/2		t_{BICY}
	Hold time	t_{WENHO}	C_L = 15pF		1/2		t_{BICY}
CLKO ↑ – A0 to A10	Setup time	t_{ADS}	C_L = 15pF		1/2		t_{BICY}
	Hold time	t_{ADH}	C_L = 15pF		1/2		t_{BICY}
CLKO ↑ – DQ0 to DQ15	Setup time	t_{DQS}	C_L = 15pF		1/2		t_{BICY}
	Hold time	t_{DQH}	C_L = 15pF		1/2		t_{BICY}
Refresh command interval		t_{REF}	C_L = 15pF		3		times/fs
CLKO propagation delay		t_{DLY}	C_L = 15pF	0		15	ns



MCU interface input/outputs (SCLK, SI, XCS, SIO pins)

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
XCS HIGH-level pulsewidth	t_{XCSWH}		30 + t_{BICY}			ns
XCS LOW-level pulsewidth	t_{XCSWL}		30 + 17t_{BICY}			ns
SCLK setup time	t_{XCSS}		30 + t_{BICY}/2			ns
SCLK hold time	t_{XCSH}		30 + t_{BICY}/2			ns
SCLK pulse cycle time	t_{SCLKCY}		60 + t_{BICY}			ns
SCLK HIGH-level pulsewidth	t_{SCLKH}		30 + t_{BICY}			ns
SCLK LOW-level pulsewidth	t_{SCLKL}		30 + t_{BICY}			ns
SI setup time	t_{SIS}		30 + t_{BICY}/2			ns
SI hold time	t_{SIH}		30 + t_{BICY}/2			ns
SCLK to output propagation delay	t_{DSIO}	C_L = 15pF	0		20	ns



FUNCTIONAL DESCRIPTION

Delay Settings

The SM5921A sets the delay value set using an MCU interface and adds that delay to the input data. The total delay value for each channel data is given by the following equation.

$$t_{Delay}\ (sec) = \frac{(nSample\text{-}system + (nSample\text{-}intrinsic + nSample\text{-}individual) \times nMp)}{fs}$$

nSample-system:	Number of system delay samples (fixed 2 samples)
nSample-intrinsic:	Number of intrinsic delay samples (16-sample units)
nSample-individual:	Number of individual delay samples (1-sample units)
nMp:	Address shift coefficient
fs:	Sampling frequency

Note that even when the intrinsic delay and individual delay are both set to 0 samples, a 2-sample delay is applied.

Address shift coefficient

The address shift coefficient is determined by the settings of the MP0N and MP1N flags. These enable the time delay to be multiplied by ×1, ×2, or ×4 without changing the delay value setting. For example, if the sampling frequency fs is switched from 48kHz to 192kHz and the address shift is set to ×4, then the same delay time is added.

MP0N	MP1N	nMp
LOW	LOW	1
LOW	HIGH	2
HIGH	LOW	4
HIGH	HIGH	1

- Data setting values cannot exceed the upper limit.
- Calculation examples
  - If fs = 48kHz, REG 0/H = 200/H, REG 2/H = 800/H, nMp = 1, then the delay value is:
    t_{Delay} = (nSample-system + (nSample-intrinsic + nSample-individual) × nMp) ÷ fs [sec]
    = (2 + (8192 + 2048) × 1) ÷ 48000 = 213.3ms
  - If fs = 192kHz, REG 0/H = 200/H, REG 2/H = 800/H, nMp = 1, then the delay value is:
    t_{Delay} = (nSample-system + (nSample-intrinsic + nSample-individual) × nMp) ÷ fs [sec]
    = (2 + (8192 + 2048) × 1) ÷ 192000 = 53.3ms
  - If fs = 192kHz, REG 0/H = 200/H, REG 2/H = 800/H, nMp = 2, then the delay value is:
    t_{Delay} = (nSample-system + (nSample-intrinsic + nSample-individual) × nMp) ÷ fs [sec]
    = (2 + (8192 + 2048) × 2) ÷ 192000 = 106.6ms
  - If fs = 192kHz, REG 0/H = 200/H, REG 2/H = 800/H, nMp = 4, then the delay value is:
    t_{Delay} = (nSample-system + (nSample-intrinsic + nSample-individual) × nMp) ÷ fs [sec]
    = (2 + (8192 + 2048) × 4) ÷ 192000 = 213.3ms

From the examples, it can be seen that switching the sampling frequency from 48kHz to 192kHz and changing nMp from 1 to 4 results in an identical time delay. Note, however, that the memory size physical limit cannot be exceeded. So, for example, the physical limit is reached with a sum (nSample-intrinsic + nSample-individual) of 16384 samples when nMp = 4, or the equivalent of 65535 samples at nMp = 1.

Intrinsic delay

The intrinsic delay is the common delay applied to each channel group, and is used to add the same delay value to the channel group data. The default value is 0 samples. The intrinsic delay is set by the values of REG 0/H (DIA/DOA and DIB/DOB groups) and REG 1/H (DIC/DOC and DID/DOD groups), with the values measured in 16-sample units (333.2µs @ fs = 48kHz).

When the TRACKT flag in REG A/H is set to HIGH, the same delay value is added to all the channel groups (DIA/DOA, DIB/DOB, DIC/DOC, DID/DOD). See the "MCU Interface" section.

Individual delay

The individual delay is the delay applied to each channel individually, and is used to add a delay offset for each channel data. The default value is 0 samples. The individual delay is set by the values of REG 2/H, REG 3/H, REG 4/H, REG 5/H, REG 6/H, REG 7/H, REG 8/H, and REG 9/H, with the values measured in 1-sample units (20.8µs @ fs = 48kHz).

When the TRACKD flag in REG A/H is set to HIGH, the delay value set in REG 2/H (DIA/DOA left-channel) is also applied to the DIA/DOA right-channel, DIB/DOB left-channel, and DIB/DOB right-channel data. Similarly, the delay value set in REG 6/H (DIC/DOC left-channel) is also applied to the DIC/DOC right-channel, DID/DOD left-channel, and DID/DOD right-channel data.

The minimum parameter settings required to apply the same delay to all channels is to set delay values in REG 0/H, REG 2/H, REG 6/H, and to set the TRACKT and TRACKD flags to HIGH. The relationship between the intrinsic delay, individual delay, and the registers is shown in the following table.

Channel	Intrinsic delay	Individual delay
DIA/DOA left-channel	REG 0/H	REG 2/H
DIA/DOA right-channel		REG 3/H
DIB/DOB left-channel		REG 4/H
DIB/DOB right-channel		REG 5/H
DIC/DOC left-channel	REG 1/H	REG 6/H
DIC/DOC right-channel		REG 7/H
DID/DOD left-channel		REG 8/H
DID/DOD right-channel		REG 9/H

Delay time examples

The total delay value is defined by the equation described earlier. The following table shows some examples.

nSample-intrinsic + nSample-individual setting	Sampling frequency (fs)					Unit
	32kHz	44.1kHz	48kHz	96kHz	192kHz	
0*1	62.5	45.4	41.7	20.8	10.4	µs
1000	31.3	22.7	20.8	10.4	5.2	ms
10000	312.5	226.8	208.3	104.2	52.1	ms
20000	625	453.5	416.7	208.3	104.2	ms
36863	1152	835.9	768	384	192	ms
65535	2048	1486.1	1365.3	682.7	341.3	ms

*1. Even when the set value is 0 samples, a fixed 2-sample system delay is applied.

Delay set value upper limit

The upper limit for the delay set value input {(nSample-intrinsic + nSample-individual) × nMp} for each channel is 65535 samples. If a delay value input exceeding 65536 is incorrectly set, an internal limiter treats the channel delay set value as 65535 samples. The following table shows some delay value setting examples.

Delay set value input			nSample-intrinsic + nSample-individual × nMp [samples]	Limiter delay set value [samples]
nMp	REG 0/H	REG 2/H		
1	FFF/H	00F/H	(65520 + 15) × 1 = 65535	65535
1	FFF/H	010/H	(65520 + 16) × 1 = 65536	65535
2	7FF/H	00F/H	(32752 + 15) × 2 = 65534	65534
2	7FF/H	010/H	(32752 + 16) × 2 = 65536	65535
4	3FF/H	00F/H	(16368 + 15) × 4 = 65532	65532
4	3FF/H	010/H	(16368 + 16) × 4 = 65536	65535

System Reset (RSTN, WPOLN pins, INIT flag)

The SM5921A must be reset when power is applied. The system is reset by applying a LOW-level pulse on the RSTN pin. When the system is reset, all registers are cleared and the sequencer is also reset. The system reset is released by a LOW-to-HIGH transition on RSTN when the supply voltage has stabilized and the WCKI and BCKI clocks have stabilized. If the WCKI or BCKI clocks stop during operation, the system should be reset again after the clocks have stabilized. After the system reset is released, the SM5921A enters the initialization sequence and starts SDRAM initialization. The initialization requires an interval of 1/fs × 64. During the initialization sequence, input data on DIA, DIB, DIC, or DID is ignored. The system can also be reset without applying a LOW-level pulse on RSTN under the following conditions.

When switching WPOLN pin or INIT flag

The SDRAM initialization sequence also begins when the WPOLN pin is switched or the INIT flag is set. During SDRAM initialization, each output is muted by the direct mute function.

Word Clock Polarity (WPOLN pin)

The SM5921A handles 64fs slot data as 1 word, enabling the word boundary polarity to be specified. The WPOLN pin has pull-up resistor built-in. When WPOLN is open circuit (or HIGH), data is handled as left-channel data when WCKI is HIGH. The data-through (bypass), output enable, and direct mute functions operate on the word boundary set by the WPOLN pin.

Refer to the “TIMING DIAGRAMS” section for more information.

WPOLN	Function
LOW	Data is handled as left-channel data during the LOW-level pulse on WCKI. The word boundary is a falling edge on WCKI.
HIGH	Data is handled as left-channel data during the HIGH-level pulse on WCKI. The word boundary is a rising edge on WCKI.

Data Through (THROU flag)

The SM5921A applies a fixed 2-sample system delay when exchanging with the SDRAM, even if the delay setting is 0 (see the “Delay Settings” section). The THROU flag in REG A/H can be set to 1 when a completely zero delay is required. When the THROU flag is set to 1, the DIA, DIB, DIC, DID input data bypasses the delay processing and is passed directly to the DOA, DOB, DOC, DOD outputs, respectively. The default setting of the THROU flag is 0, so if not set specifically, delayed data is output on the DOA, DOB, DOC, DOD pins. The THROU flag is detected on the WCKI boundary edge, which means that there is a maximum 1-word delay before the change is reflected at the output.

Output Enable (OEN pin)

The SM5921A has an output enable control for the DOA, DOB, DOC, DOD outputs. When OEN is HIGH, the output pins are disabled. The OEN pin has a pull-down resistor built-in. When the OEN pin is open-circuit (or LOW), the output pins are enabled and delay data is output. The OEN pin is detected on the WCKI boundary edge, which means that there is a maximum 1-word delay before the change is reflected at the output.

Direct Mute (DMUTEN pin)

Direct mute ON/OFF

DMUTEN	Function
LOW	0 data output from the next output word after writing the setting.
HIGH	Normal delay data output from the next output word after writing the setting.

Other mute operations

The outputs are also muted (direct mute) when a reset pulse is applied.

RSTN	Function
LOW	0 data output from the next output word after writing the setting.
HIGH	Normal delay data output after 64 output words after writing the setting.

The outputs are also muted (direct mute) when the INIT flag is set.

INIT	Function
LOW	Normal output operation.
HIGH	Normal delay data output after a 64-word mute interval after writing the setting.

The outputs are also muted (direct mute) when the PDW flag is set.

PDW	Function
LOW (HIGH → LOW)	0 data output from the next output word after writing to the register. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.
HIGH	0 data output from the next output word after writing data to the register.

The outputs are also muted (direct mute) setting the delay data values.

Delay setting	Function
Intrinsic delay	0 data output from the next output word after writing to registers REG 0/H and 1/H. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.
Individual delay	0 data output from the next output word after writing to registers REG 3/H to 9/H. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.

The outputs are also muted (direct mute) when changing the setting of the MP0n and MP1N flags.

MP0N, MP1N	Function
(L,L) → (H,L) (L,L) → (L,H) (H,H) → (H,L) (H,H) → (L,H)	0 data output from the next output word after changing the setting of the flags. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.
(H,L) → (L,L) (H,L) → (L,H) (H,L) → (H,H)	0 data output from the next output word after changing the setting of the flags. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.
(L,H) → (L,L) (L,H) → (H,L) (L,H) → (H,H)	0 data output from the next output word after changing the setting of the flags. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.
(L,L) → (H,H) (H,H) → (L,L)	Normal output operation.

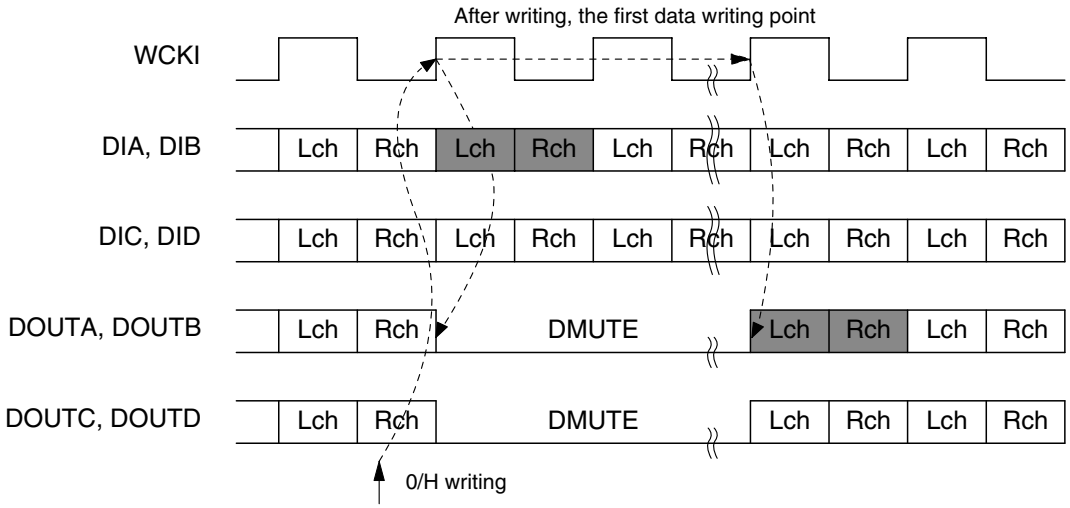
The outputs are also muted (direct mute) when setting the TRACKT and TRACKD flags.

TRACKT	Function
LOW (HIGH → LOW)	0 data output from the next output word after writing to the register. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.
HIGH (LOW → HIGH)	0 data output from the next output word after writing to the register. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.

TRACKD	Function
LOW (HIGH → LOW)	0 data output from the next output word after writing to the register. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.
HIGH (LOW → HIGH)	0 data output from the next output word after writing to the register. The outputs are muted during the interval until the initialization data write point, and then mute is released for delay data output.

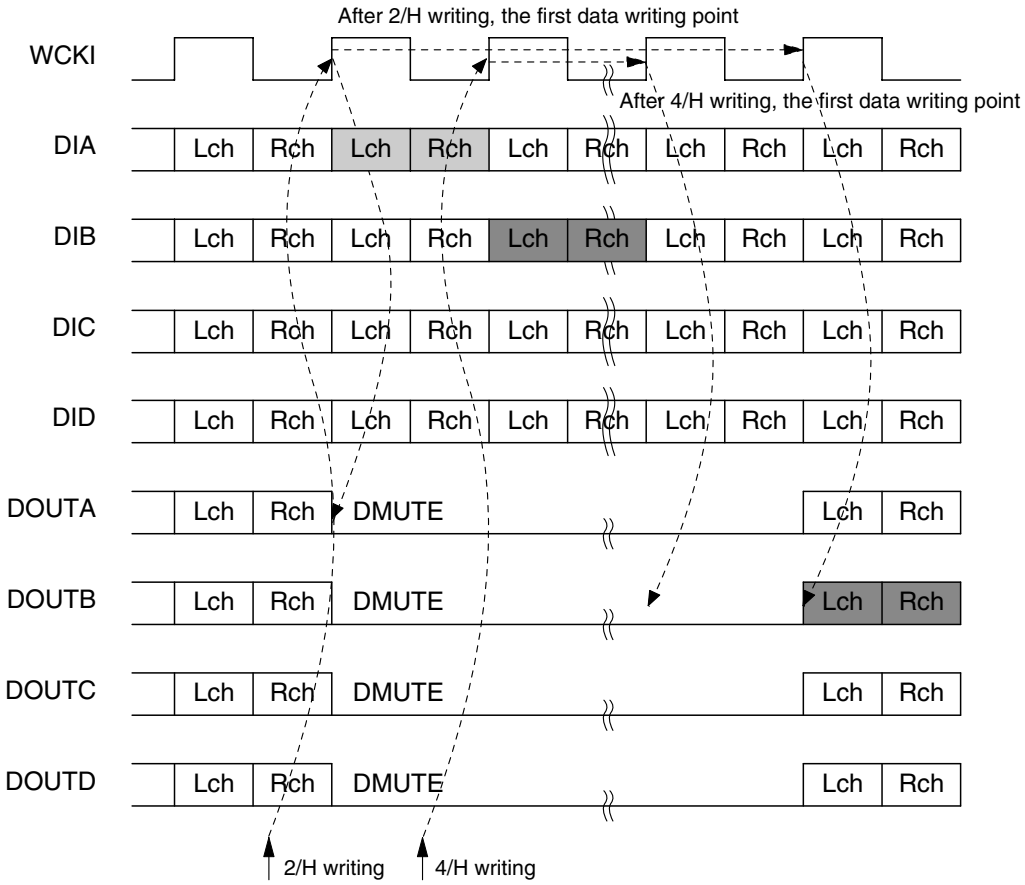
- If the delay value is set during the 64-word direct mute interval after reset is released, the output muting is extended until the initialization data write point after the direct mute interval.
- If the delay value is updated during mute operation, and the extended mute interval determined by a previous delay setting is longer than that due to the updated value, muting continues until the previously set delay value setting. If that mute interval is smaller than that due to the updated value, muting continues until the point determined by the updated value. In other words, muting continues until a point determined by the larger of the two values.

Intrinsic delay timing example (TRACKT = LOW)



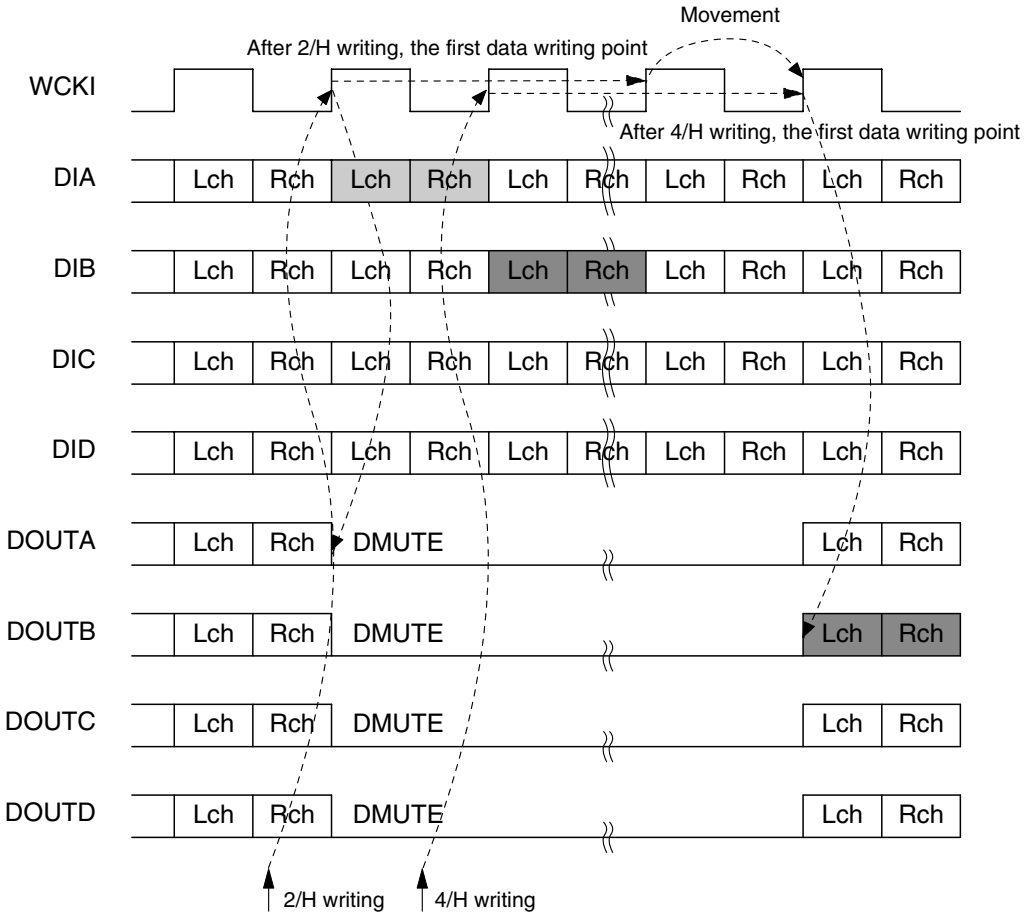
Individual delay timing example (TRACKD = LOW)

- Mute interval determined by REG 2/H is larger than that determined by REG 4/H



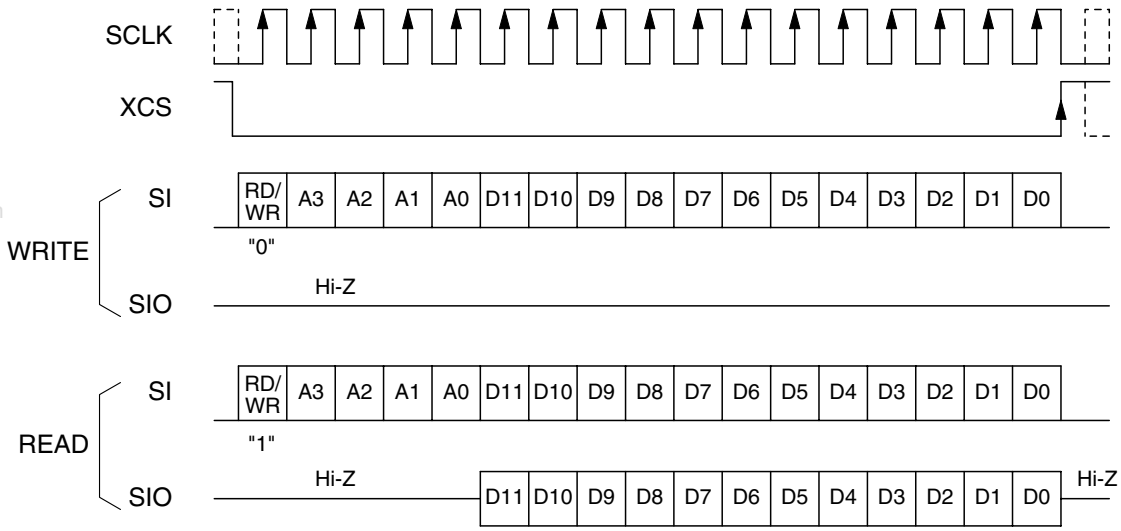
Individual delay timing example (TRACKD = LOW)

■ Mute interval determined by REG 2/H is smaller than that determined by REG 4/H



MCU Interface

The MCU interface is comprised by a 4-wire serial interface.



- The SCLK clock may trace the dotted line path or not, as long as there is 17 SCLK pulses during the XCS LOW-level pulse interval.
- When the RD/WR bit is set to 1 the device enters register read mode, and the register contents addressed by bits A3 to A0 are output as serial data on the SIO pin. In read mode, the SI input data bits D11 to D0 are ignored.
- When the RD/WR bit is set to 0 the device enters register write mode, and the SI input data bits D11 to D0 are written to the register addressed by bits A3 to A0.
- Systems that hold the serial input high-impedance during the D11 to D0 data interval in read mode can bind the SI and SIO pins and function as a 3-wire serial interface.
- In read mode, the output for non-assigned addresses is 0 data.

REG 0/H

A3	0	Intrinsic delay (DIA, DIB)
A2	0	
A1	0	
A0	0	
D11	×	Minimum unit setting: 16 samples 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 16 samples 0000 0000 1000 → 128 samples 0000 0001 0000 → 256 samples 0000 1000 0000 → 2048 samples 0001 0000 0000 → 4096 samples 1000 0000 0000 → 32768 samples 1111 1111 1111 → 65520 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	333.2µs/step @ fs = 48kHz 1365ms/step @ fs = 48kHz 83.3µs/step @ fs = 192kHz 341.2ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 1/H

A3	0	Intrinsic delay (DIC, DID)
A2	0	
A1	0	
A0	1	
D11	×	Minimum unit setting: 16 samples 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 16 samples 0000 0000 1000 → 128 samples 0000 0001 0000 → 256 samples 0000 1000 0000 → 2048 samples 0001 0000 0000 → 4096 samples 1000 0000 0000 → 32768 samples 1111 1111 1111 → 65520 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	333.2µs/step @ fs = 48kHz 1365ms/step @ fs = 48kHz 83.3µs/step @ fs = 192kHz 341.2ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 2/H

A3	0	Individual delay (DIA left-channel)
A2	0	
A1	1	
A0	0	
D11	×	Minimum unit setting: 1 sample 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 1 samples 0000 0000 1000 → 8 samples 0000 0001 0000 → 16 samples 0000 1000 0000 → 128 samples 0001 0000 0000 → 256 samples 1000 0000 0000 → 2048 samples 1111 1111 1111 → 4095 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	20.8µs/step @ fs = 48kHz 85.3ms/step @ fs = 48kHz 5.2µs/step @ fs = 192kHz 21.3ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 3/H

A3	0	Individual delay (DIA right-channel)
A2	0	
A1	1	
A0	1	
D11	×	Minimum unit setting: 1 sample 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 1 samples 0000 0000 1000 → 8 samples 0000 0001 0000 → 16 samples 0000 1000 0000 → 128 samples 0001 0000 0000 → 256 samples 1000 0000 0000 → 2048 samples 1111 1111 1111 → 4095 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	20.8µs/step @ fs = 48kHz 85.3ms/step @ fs = 48kHz 5.2µs/step @ fs = 192kHz 21.3ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 4/H

A3	0	Individual delay (DIB left-channel)
A2	1	
A1	0	
A0	0	
D11	×	Minimum unit setting: 1 sample 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 1 samples 0000 0000 1000 → 8 samples 0000 0001 0000 → 16 samples 0000 1000 0000 → 128 samples 0001 0000 0000 → 256 samples 1000 0000 0000 → 2048 samples 1111 1111 1111 → 4095 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	20.8µs/step @ fs = 48kHz 85.3ms/step @ fs = 48kHz 5.2µs/step @ fs = 192kHz 21.3ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 5/H

A3	0	Individual delay (DIB right-channel)
A2	1	
A1	0	
A0	1	
D11	×	Minimum unit setting: 1 sample 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 1 samples 0000 0000 1000 → 8 samples 0000 0001 0000 → 16 samples 0000 1000 0000 → 128 samples 0001 0000 0000 → 256 samples 1000 0000 0000 → 2048 samples 1111 1111 1111 → 4095 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	20.8µs/step @ fs = 48kHz 85.3ms/step @ fs = 48kHz 5.2µs/step @ fs = 192kHz 21.3ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 6/H

A3	0	Individual delay (DIC left-channel)
A2	1	
A1	1	
A0	0	
D11	×	Minimum unit setting: 1 sample 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 1 samples 0000 0000 1000 → 8 samples 0000 0001 0000 → 16 samples 0000 1000 0000 → 128 samples 0001 0000 0000 → 256 samples 1000 0000 0000 → 2048 samples 1111 1111 1111 → 4095 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	20.8µs/step @ fs = 48kHz 85.3ms/step @ fs = 48kHz 5.2µs/step @ fs = 192kHz 21.3ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 7/H

A3	0	Individual delay (DIC right-channel)
A2	1	
A1	1	
A0	1	
D11	×	Minimum unit setting: 1 sample 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 1 samples 0000 0000 1000 → 8 samples 0000 0001 0000 → 16 samples 0000 1000 0000 → 128 samples 0001 0000 0000 → 256 samples 1000 0000 0000 → 2048 samples 1111 1111 1111 → 4095 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	20.8µs/step @ fs = 48kHz 85.3ms/step @ fs = 48kHz 5.2µs/step @ fs = 192kHz 21.3ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 8/H

A3	1	Individual delay (DID left-channel)
A2	0	
A1	0	
A0	0	
D11	×	Minimum unit setting: 1 sample 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 1 samples 0000 0000 1000 → 8 samples 0000 0001 0000 → 16 samples 0000 1000 0000 → 128 samples 0001 0000 0000 → 256 samples 1000 0000 0000 → 2048 samples 1111 1111 1111 → 4095 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	20.8µs/step @ fs = 48kHz 85.3ms/step @ fs = 48kHz 5.2µs/step @ fs = 192kHz 21.3ms/step @ fs = 192kHz
D1	×	
D0	×	

REG 9/H

A3	1	Individual delay (DID right-channel)
A2	0	
A1	0	
A0	1	
D11	×	Minimum unit setting: 1 sample 0000 0000 0000 → 0 samples (default) 0000 0000 0001 → 1 samples 0000 0000 1000 → 8 samples 0000 0001 0000 → 16 samples 0000 1000 0000 → 128 samples 0001 0000 0000 → 256 samples 1000 0000 0000 → 2048 samples 1111 1111 1111 → 4095 samples
D10	×	
D9	×	
D8	×	
D7	×	
D6	×	
D5	×	
D4	×	
D3	×	
D2	×	20.8µs/step @ fs = 48kHz 85.3ms/step @ fs = 48kHz 5.2µs/step @ fs = 192kHz 21.3ms/step @ fs = 192kHz
D1	×	
D0	×	

REG A/H

A3	1	Miscellaneous settings
A2	0	
A1	1	
A0	0	
D11	L	Do not use
D10	L	Do not use
D9	L	Do not use
D8	L	Do not use
D7	L	Do not use
D6	L	MP0N address shift setting 0
D5	L	MP1N address shift setting 1 (MP0N, MP1N) = (L,L) → × 1 multiplication (MP0N, MP1N) = (L,H) → × 2 multiplication (MP0N, MP1N) = (H,L) → × 4 multiplication (MP0N, MP1N) = (H,H) → × 1 multiplication
D4	L	THROU flag THROU = H: Input data is passed through to the output bypassing delay processing. THROU = L: Normal operating mode (default)
D3	L	TRACKD flag TRACKD = H: REG 3/H to REG5/H follow the REG 2/H contents. REG 7/H to REG9/H follow the REG 6/H contents. TRACKD = L: Normal operating mode (default)
D2	L	TRACKT flag TRACKT = H: REG 1/H follows the REG 0/H contents. TRACKT = L: Normal operating mode (default)
D1	L	PDW flag PDW = H: Issues the power-down command to the SDRAM. PDW = L: Normal operating mode (default)
D0	L	INIT flag INIT = H: Starts the SDRAM initialization process. INIT is set to L when the initialization process ends. INIT = L: Normal operating mode (default)

SDRAM

SDRAM compatibility

The SM5921A transfers data when the SDRAM mode register (MRS) has the following settings. SDRAM devices that support these settings are compatible.

CL ($\overline{\text{CAS}}$ latency) : 2
BL (Burst length) : 2, 8
WT (Wrap type) : Sequential

Connecting to SDRAM

The SM5921A supports 16M/64M/128M (×16 devices) SDRAM. The SDRAM interface is connected as described in the following table.

SDRAM pins	SM5921A pins		
	16M SDRAM connection	64M SDRAM connection	128M SDRAM connection
$\overline{\text{CS}}$	CSN	CSN	CSN
CLK	CLKO	CLKO	CLKO
CKE	CKE	CKE	CKE
BA1	–	LOW-level	LOW-level
BA0 (BA)	BA	BA	BA
A11	–	LOW-level	LOW-level
A10 to A0	A10 to A0	A10 to A0	A10 to A0
$\overline{\text{RAS}}$	RASN	RASN	RASN
$\overline{\text{CAS}}$	CASN	CASN	CASN
$\overline{\text{WE}}$	WEN	WEN	WEN
HDQM	DQM	DQM	DQM
LDQM	DQM	DQM	DQM
DQ15 to DQ0	DQ15 to DQ0	DQ15 to DQ0	DQ15 to DQ0

TIMING DIAGRAMS

Input Timing (WCKI, BCKI, DIA, DIB, DIC, DID pins)

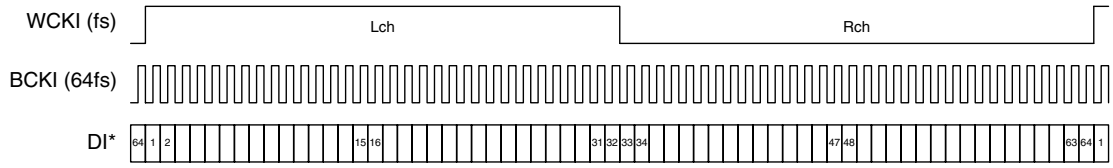


Figure 1. 64fs/slot, WPOLN = H
DI*: DIA, DIB, DIC, DID pins

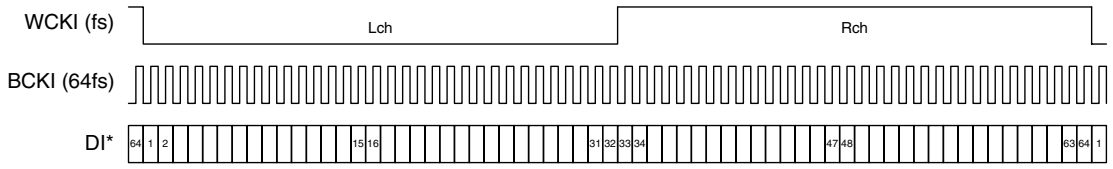


Figure 2. 64fs/slot, WPOLN = L
DI*: DIA, DIB, DIC, DID pins

Output Timing (WCKI, BCKI, DOUTA, DOUTB, DOUTC, DOUTD pins)

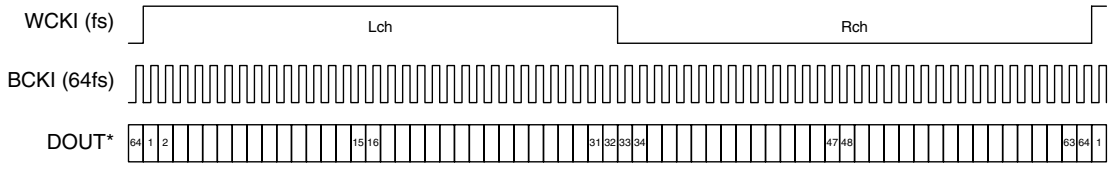


Figure 3. 64fs/slot, WPOLN = H
DOUT*: DOUTA, DOUTB, DOUTC, DOUTD pins

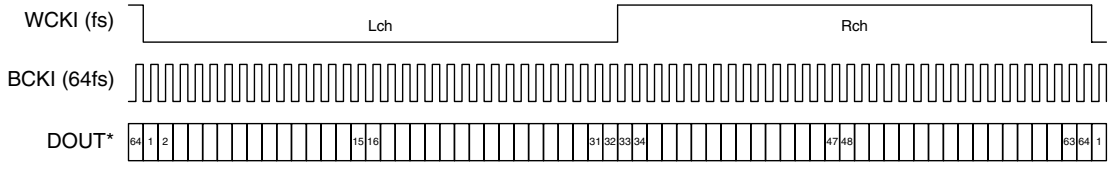
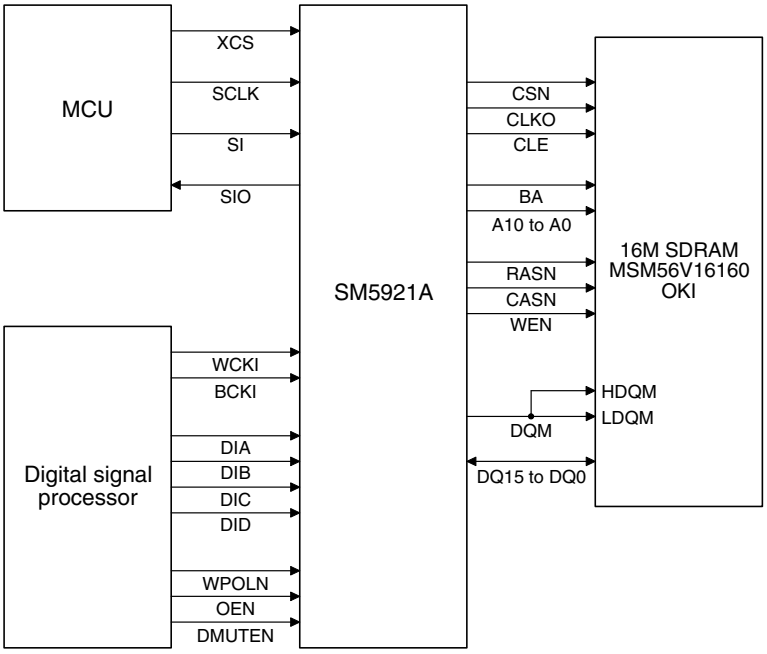


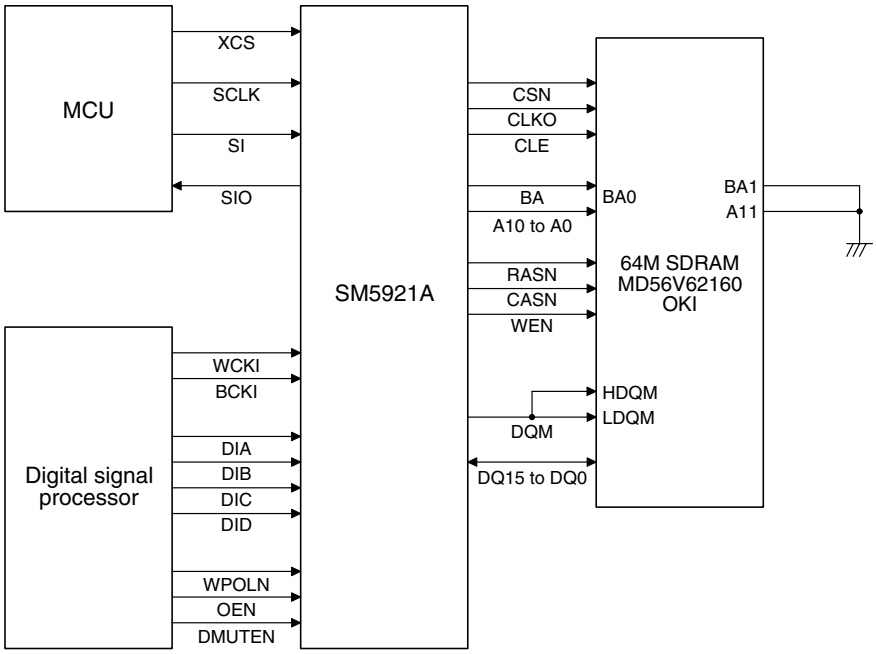
Figure 4. 64fs/slot, WPOLN = L
DOUT*: DOUTA, DOUTB, DOUTC, DOUTD pins

TYPICAL APPLICATION CIRCUITS

16M SDRAM (MSM56V16160) Connection Example



64M SDRAM (MD56V62160) Connection Example



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