

Dual Enhancement Mode MOSFET (N- and P-Channel)

Features

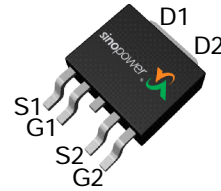
- N-Channel
60V/20A,
 $R_{DS(ON)} = 48m\Omega(\text{max.}) @ V_{GS} = 10V$
 $R_{DS(ON)} = 59m\Omega(\text{max.}) @ V_{GS} = 4.5V$
- P-Channel
-60V/-15A,
 $R_{DS(ON)} = 95m\Omega(\text{max.}) @ V_{GS} = -10V$
 $R_{DS(ON)} = 130m\Omega(\text{max.}) @ V_{GS} = -4.5V$
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)
- ESD protection

Note : The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

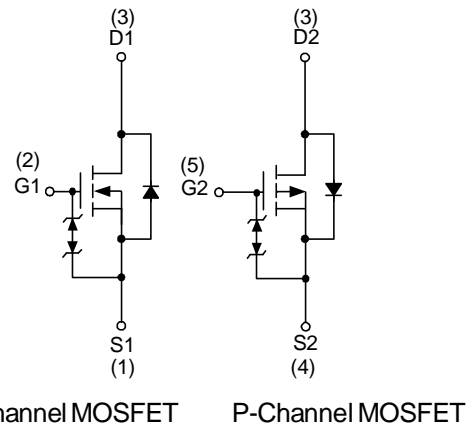
Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

Pin Description



Top View of TO-252-4



N-Channel MOSFET

P-Channel MOSFET

Ordering and Marking Information

<p>SM6042CS □□□-□□□</p> <div style="margin-left: 20px;"> <p>└─ Assembly Material</p> <p>└─ Handling Code</p> <p>└─ Temperature Range</p> <p>└─ Package Code</p> </div>	<p>Package Code U4 : TO-252-4</p> <p>Operating Junction Temperature Range C : -55 to 150 °C</p> <p>Handling Code TR : Tape & Reel (2500ea/reel)</p> <p>Assembly Material G : Halogen and Lead Free Device</p>
<p>SM6042CS U4 :</p> <div style="border: 1px solid black; padding: 2px; display: inline-block;"> <p style="margin: 0; padding: 0;">SM6042CS XXXXX</p> </div>	<p>XXXXX - Lot Code</p>

Note : SINOPOWER lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. SINOPOWER lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. SINOPOWER defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

SINOPOWER reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		N Channel	P Channel	Unit
Common Ratings					
V_{DSS}	Drain-Source Voltage		60	-60	V
V_{GSS}	Gate-Source Voltage		± 20	± 20	
T_J	Maximum Junction Temperature		150		$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-55 to 150		
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$	10	-7.5	A
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	20	-15	
		$T_C=100^\circ\text{C}$	12.8	-9.7	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	35.7	44.6	W
		$T_C=100^\circ\text{C}$	14.2	17.8	
$R_{\theta JC}$	Thermal Resistance-Junction to Case		3.5	2.8	$^\circ\text{C/W}$
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	8.5	-5.7	A
		$T_A=70^\circ\text{C}$	6.8	-4.6	
I_{DM}^a	Pulsed Drain Current	$T_C=25^\circ\text{C}$	80 *	-60 *	
P_D^b	Power Dissipation	$T_A=25^\circ\text{C}$	6.25	6.25	W
		$T_A=70^\circ\text{C}$	4	4	
$R_{\theta JA}^c$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{s}$	20	20	$^\circ\text{C/W}$
		Steady State	60	60	
I_{AS}^d	Avalanche Current, Single pulse	$L=0.5\text{mH}$	8	-10	A
E_{AS}^d	Avalanche Energy, Single pulse	$L=0.5\text{mH}$	16	25	mJ

Note * : Limited by package.

Note a : Pulse width limited by max. junction temperature.

Note b : $t < 10\text{s}$.

Note c : $R_{\theta JA}$ steady state $t=100\text{s}$. $R_{\theta JA}$ is measured with the device mounted on 1in^2 , FR-4 board with 2oz. Copper.

Note d : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_J=25^\circ\text{C}$).

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	N Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=48V, V_{GS}=0V$ $T_J=85^\circ\text{C}$	-	-	1	μA
			-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1	2	3	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 10	μA
$R_{DS(ON)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=10A$	-	40	48	m Ω
		$V_{GS}=4.5V, I_{DS}=8A$	-	45	59	
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD}=5A, V_{GS}=0V$	-	0.8	1.3	V
t_{rr}	Reverse Recovery Time	$I_{DS}=12A, di_{SD}/dt=100A/\mu s$	-	20	-	ns
Q_{rr}	Reverse Recovery Charge		-	20	-	nC
Dynamic Characteristics^e						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$	-	2.8	5.6	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=30V,$ Frequency=1.0MHz	-	540	700	pF
C_{oss}	Output Capacitance		-	56	-	
C_{rss}	Reverse Transfer Capacitance		-	26	-	
$t_{d(ON)}$	Turn-on Delay Time		$V_{DD}=30V, R_L=30\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	-	10	18
t_r	Turn-on Rise Time	-		6	11	
$t_{d(OFF)}$	Turn-off Delay Time	-		21	38	
t_f	Turn-off Fall Time	-		5	9	
Gate Charge Characteristics^e						
Q_g	Total Gate Charge	$V_{DS}=30V, V_{GS}=4.5V,$ $I_{DS}=12A$	-	5.5	-	nC
Q_g	Total Gate Charge	$V_{DS}=30V, V_{GS}=10V,$ $I_{DS}=12A$	-	11.5	16	
Q_{gs}	Gate-Source Charge		-	2.3	-	
Q_{gd}	Gate-Drain Charge		-	2.2	-	
Q_{gth}	Threshold Gate Charge		-	1.9	-	

Note e : Guaranteed by design, not subject to production testing.

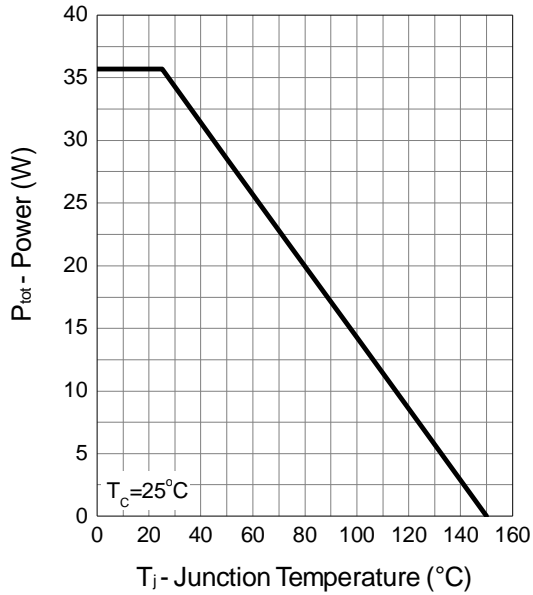
Electrical Characteristics (Cont.) ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	P Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=-250\mu A$	-60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-48V, V_{GS}=0V$ $T_J=85^\circ\text{C}$	-	-	-1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=-250\mu A$	-1	-2	-3	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 10	μA
$R_{DS(ON)}$	Drain-Source On-state Resistance	$V_{GS}=-10V, I_{DS}=-7.5A$ $V_{GS}=-4.5V, I_{DS}=-6.5A$	-	75	95	$m\Omega$
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD}=-1A, V_{GS}=0V$	-	-0.7	-1	V
t_{rr}	Reverse Recovery Time	$I_{DS}=-7.5A,$ $dI_{SD}/dt=100A/\mu s$	-	18	-	ns
Q_{rr}	Reverse Recovery Charge		-	13	-	nC
Dynamic Characteristics^e						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$	-	10	20	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=-30V,$ Frequency=1.0MHz	-	530	690	pF
C_{oss}	Output Capacitance		-	66	-	
C_{riss}	Reverse Transfer Capacitance		-	36	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-30V, R_L=30\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	-	8	15	ns
t_r	Turn-on Rise Time		-	4.5	8	
$t_{d(OFF)}$	Turn-off Delay Time		-	40	72	
t_f	Turn-off Fall Time		-	27	49	
Gate Charge Characteristics^e						
Q_g	Total Gate Charge	$V_{DS}=-30V, V_{GS}=-4.5V,$ $I_{DS}=-7.5A$	-	6	-	nC
Q_g	Total Gate Charge		-	12	17	
Q_{gs}	Gate-Source Charge	$V_{DS}=-30V, V_{GS}=-10V,$ $I_{DS}=-7.5A$	-	1.2	-	
Q_{gd}	Gate-Drain Charge		-	3.6	-	
Q_{gth}	Threshold Gate Charge		-	1	-	

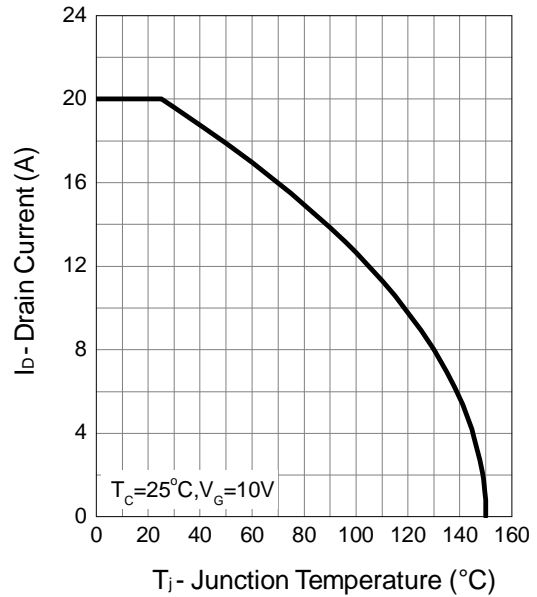
Note e : Guaranteed by design, not subject to production testing.

N Channel Typical Operating Characteristics

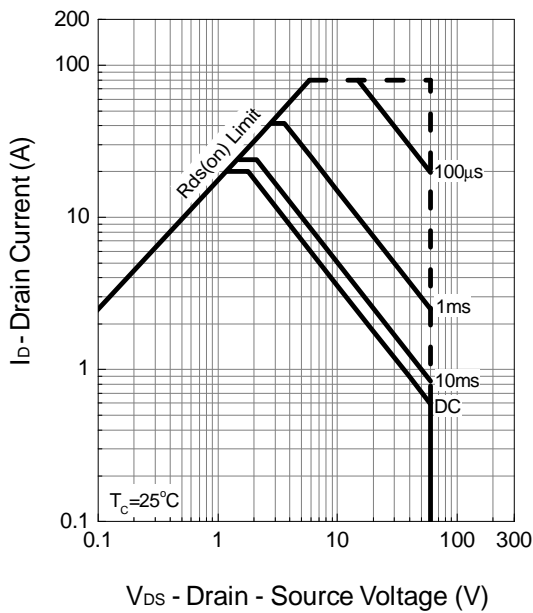
Power Dissipation



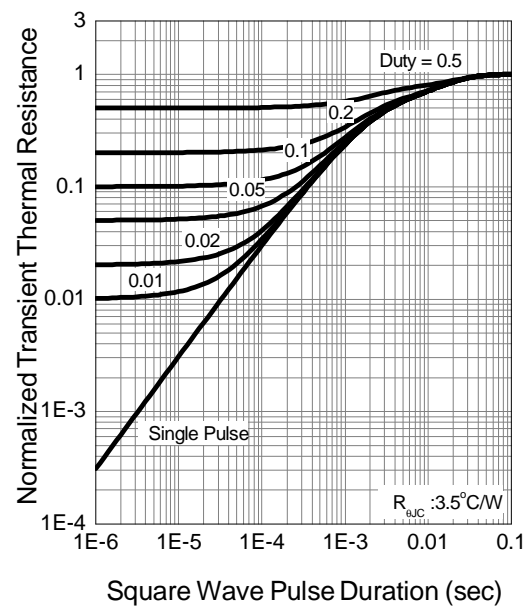
Drain Current



Safe Operation Area

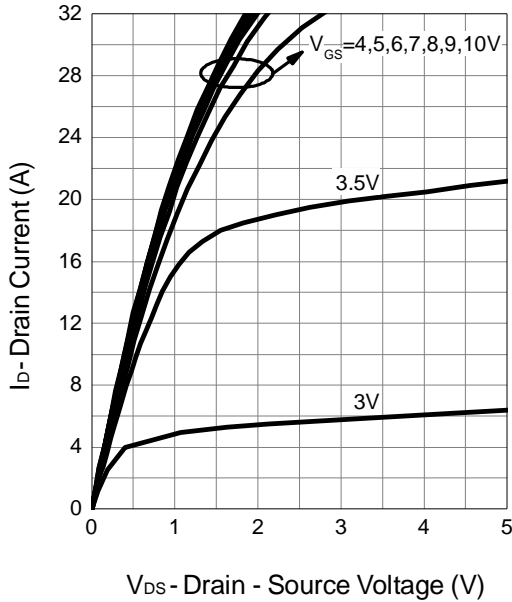


Thermal Transient Impedance

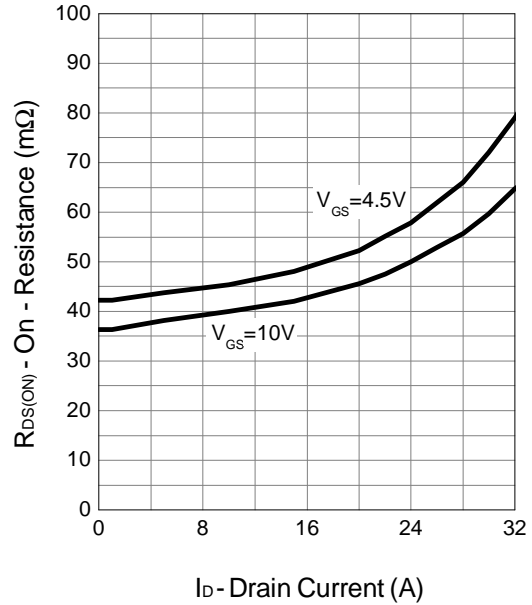


N Channel Typical Operating Characteristics (Cont.)

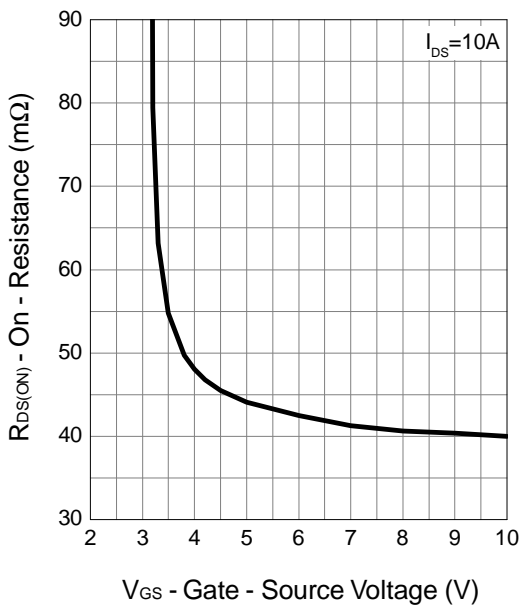
Output Characteristics



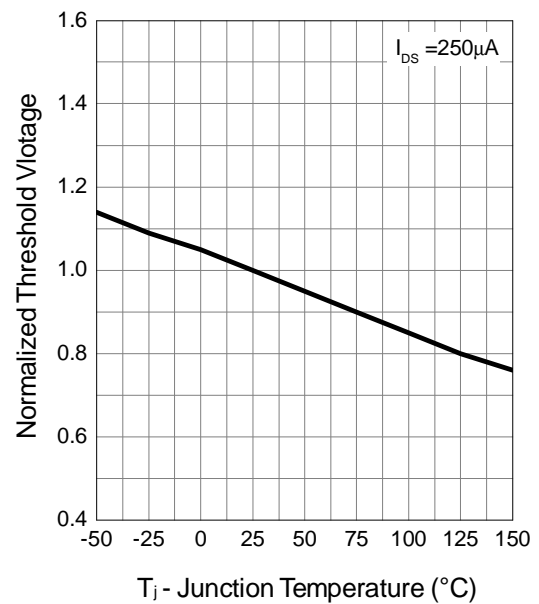
Drain-Source On Resistance



Gate-Source On Resistance

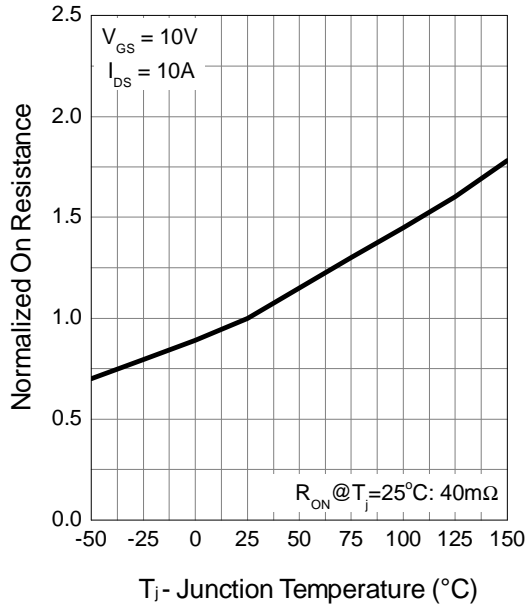


Gate Threshold Voltage

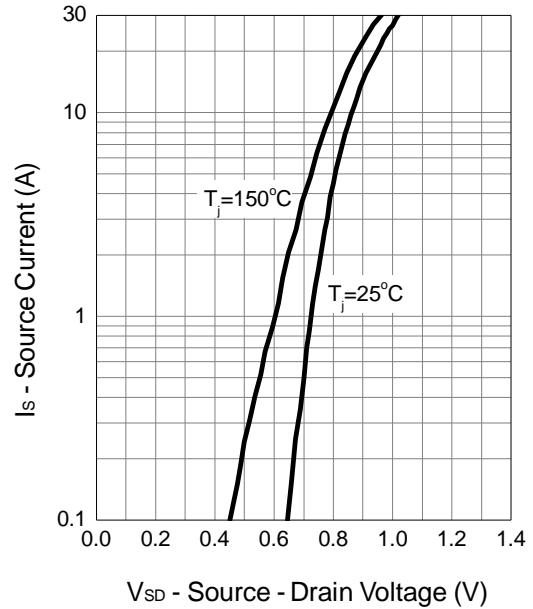


N Channel Typical Operating Characteristics (Cont.)

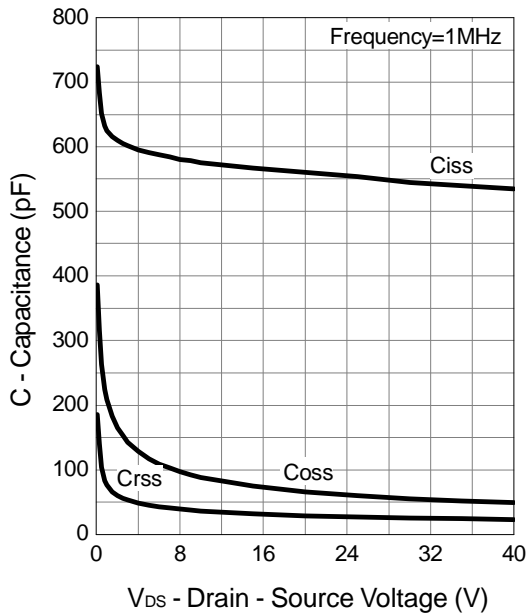
Drain-Source On Resistance



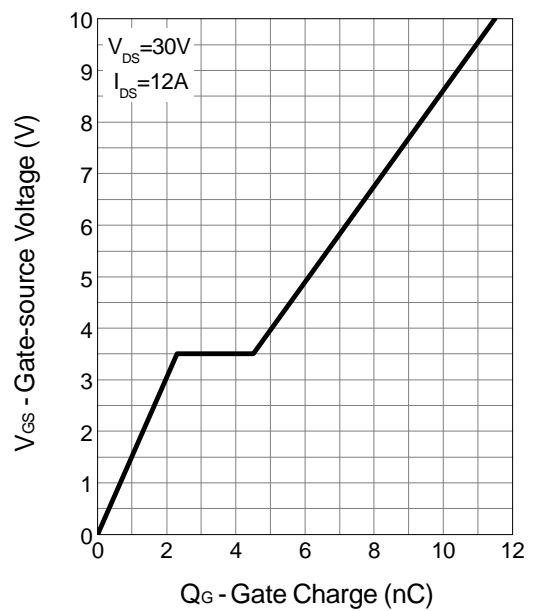
Source-Drain Diode Forward



Capacitance

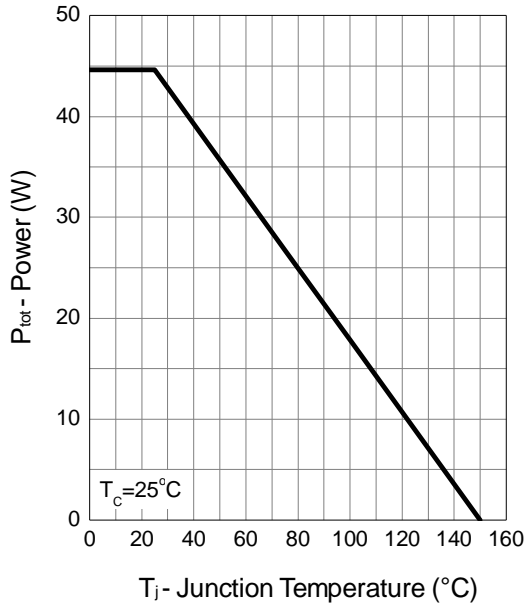


Gate Charge

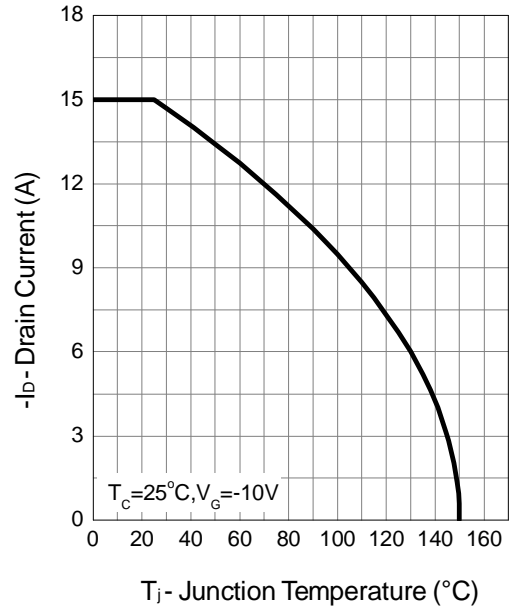


P Channel Typical Operating Characteristics (Cont.)

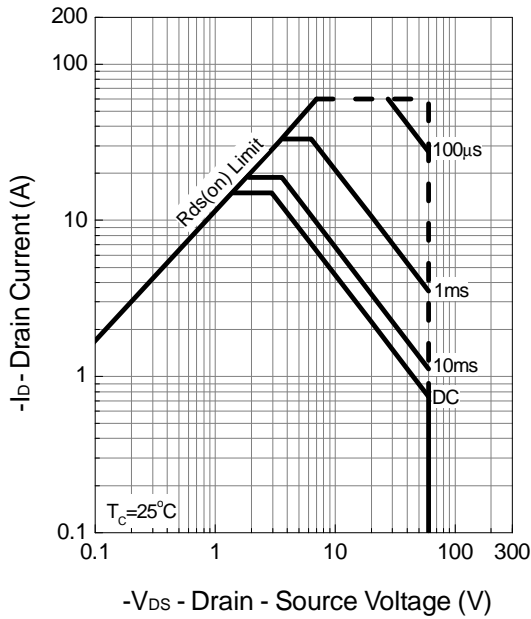
Power Dissipation



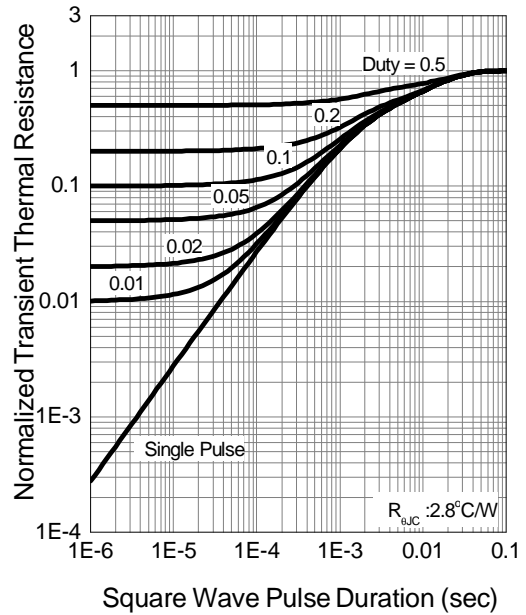
Drain Current



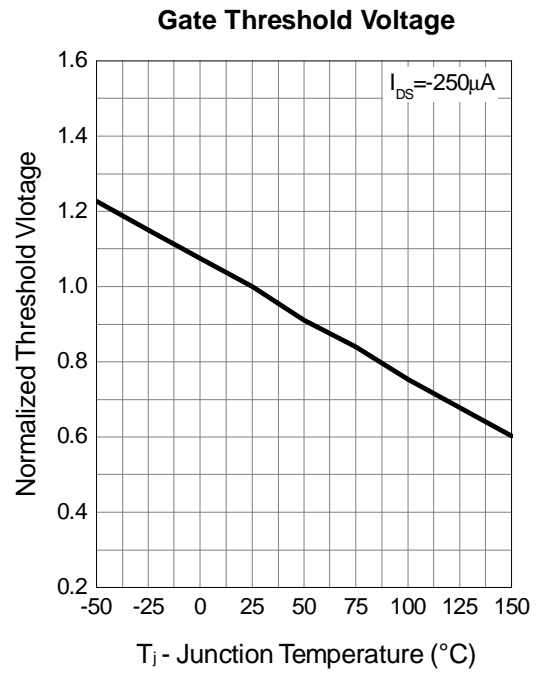
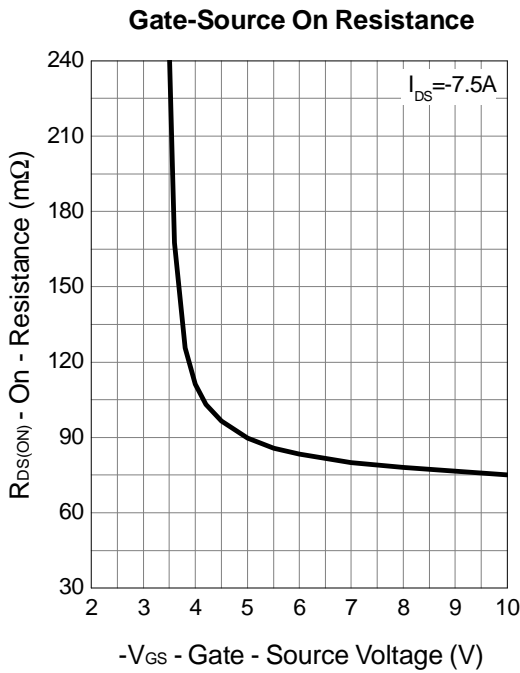
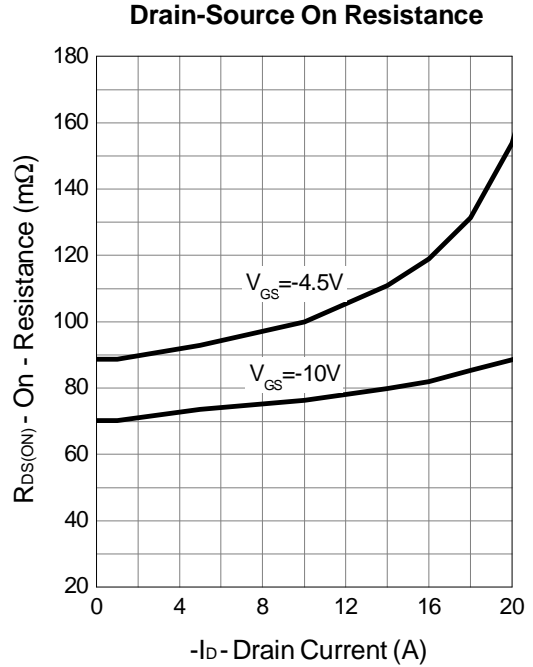
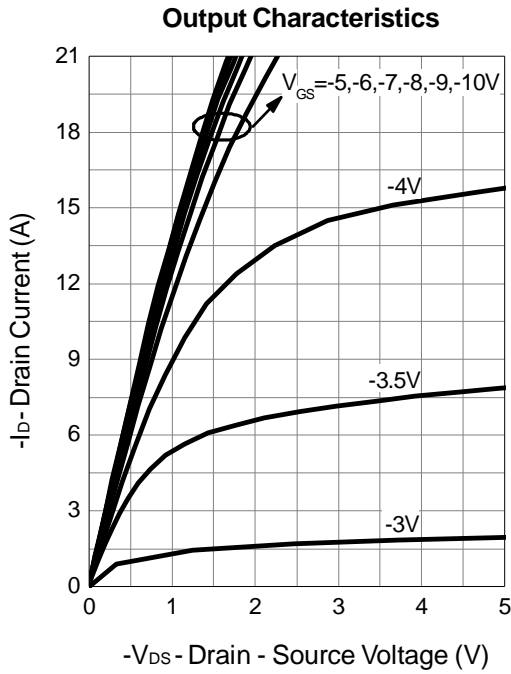
Safe Operation Area



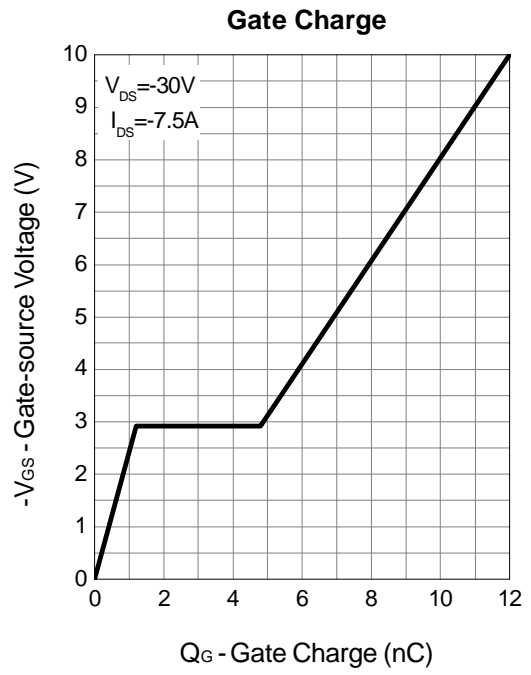
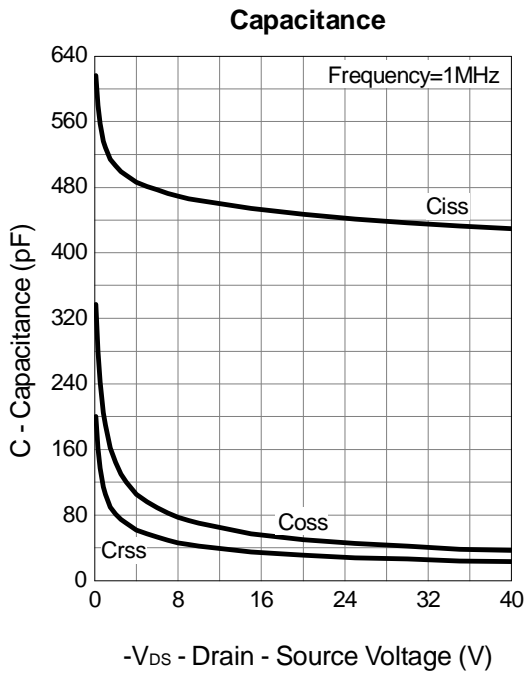
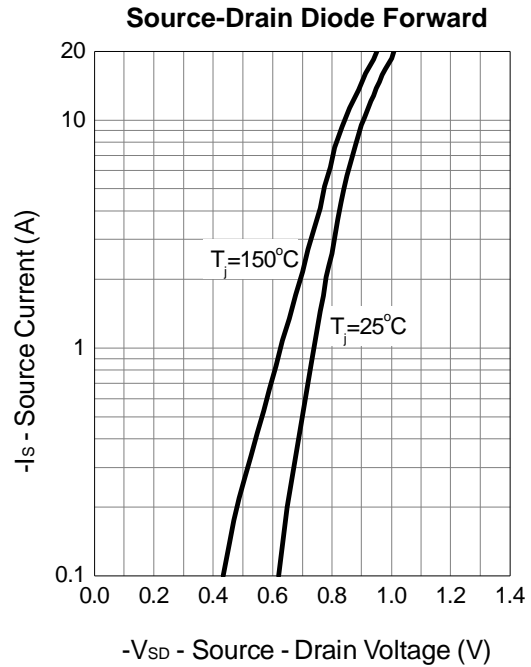
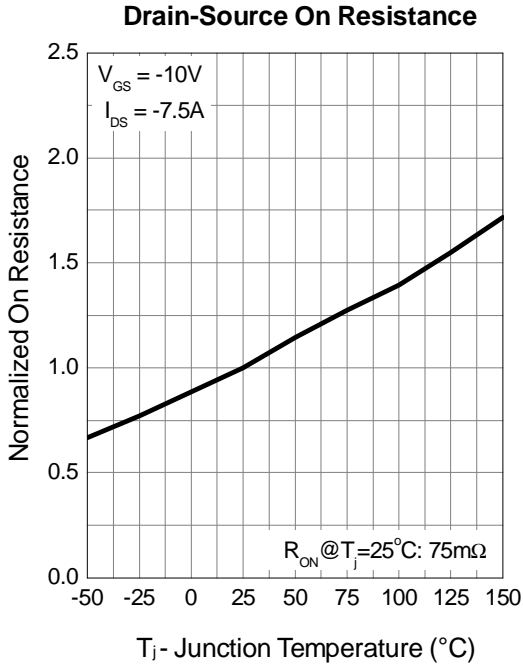
Thermal Transient Impedance



P Channel Typical Operating Characteristics (Cont.)

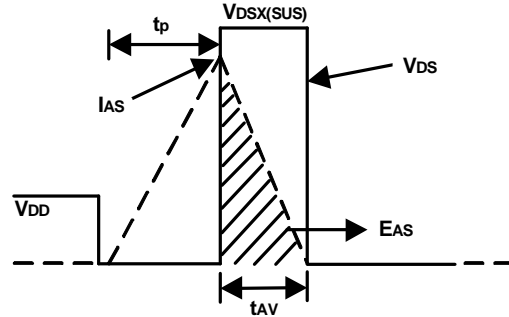
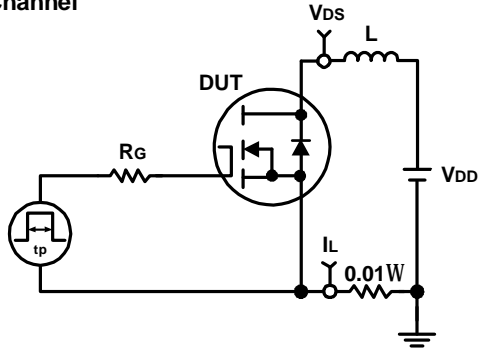


P Channel Typical Operating Characteristics (Cont.)

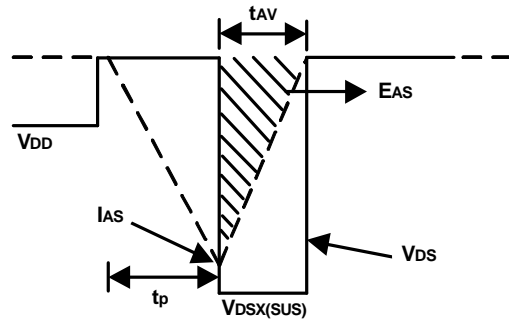
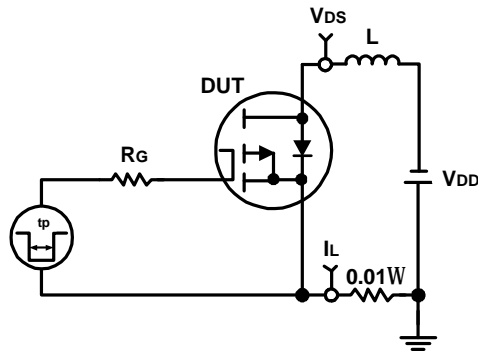


Avalanche Test Circuit and Waveforms

N Channel

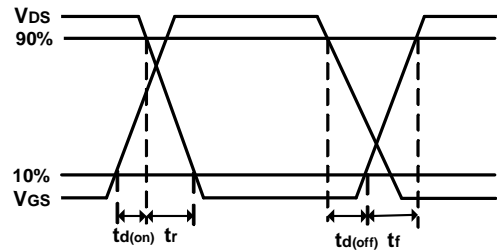
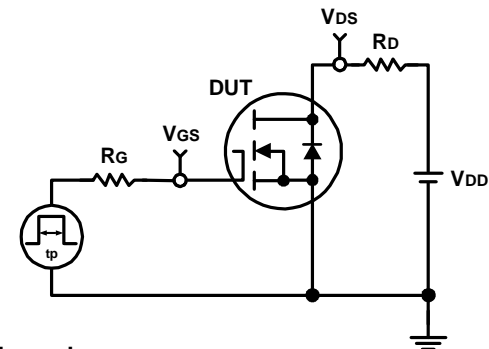


P Channel

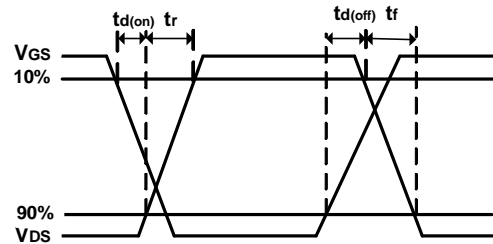
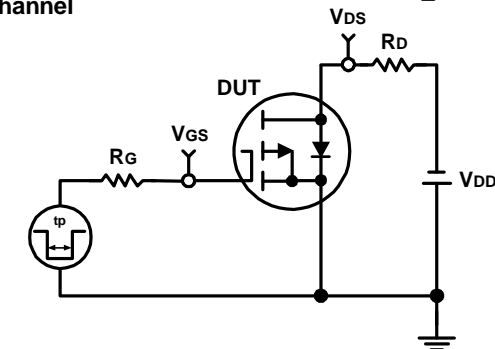


Switching Time Test Circuit and Waveforms

N Channel

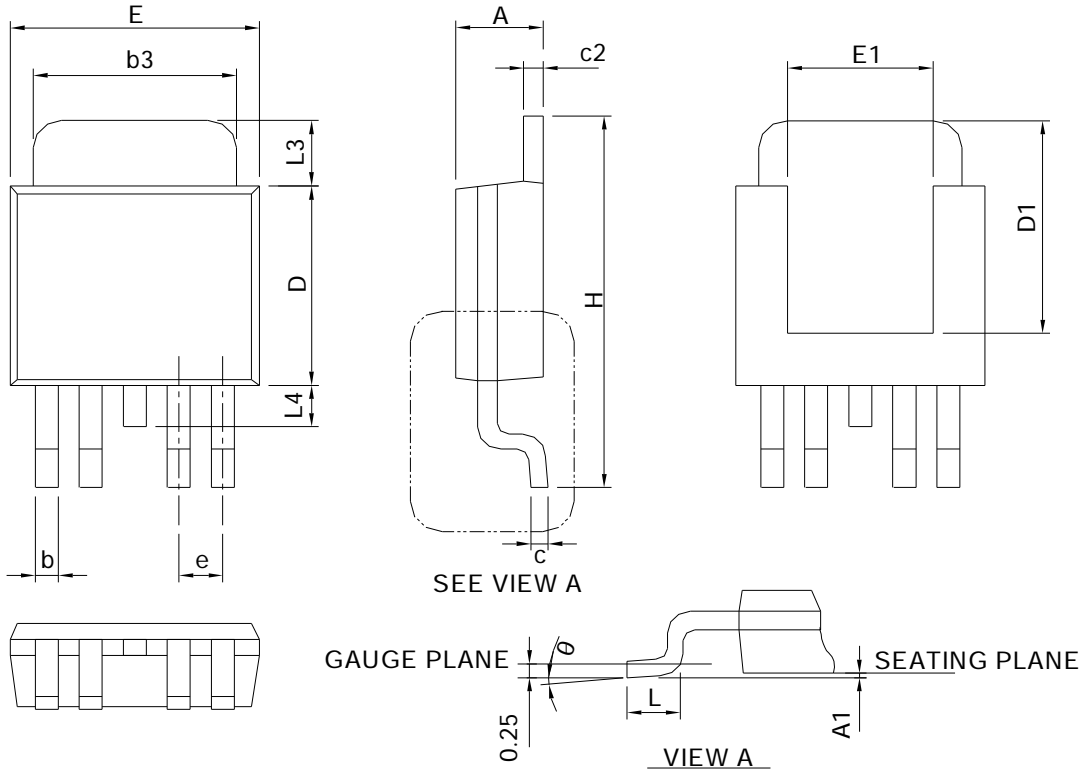


P Channel



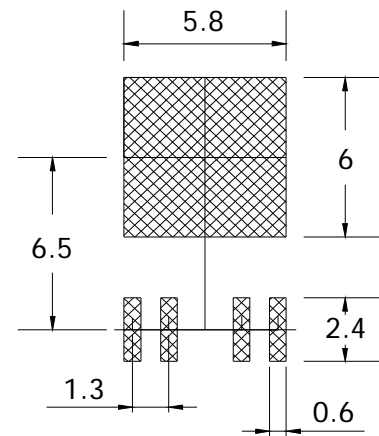
Package Information

TO-252-4



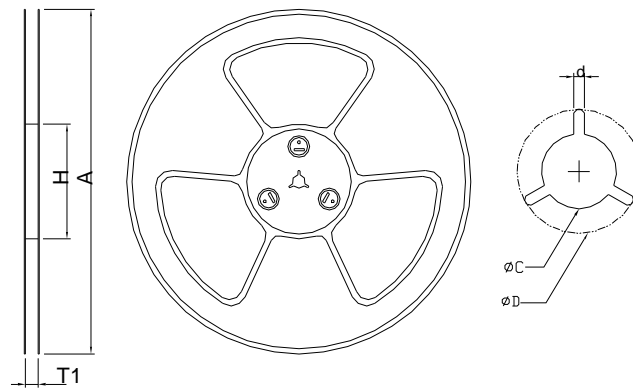
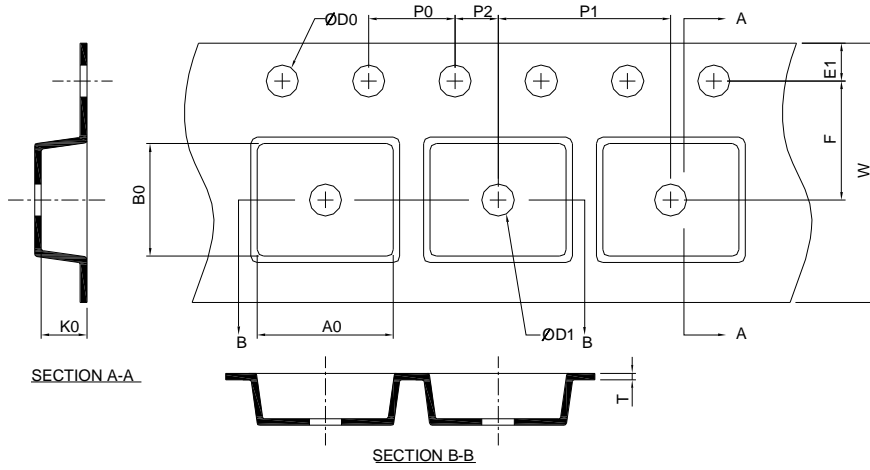
SYMBOL	TO-252-4			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	-	0.2	-	0.008
b	0.50	0.71	0.020	0.028
b3	4.32	5.46	0.170	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	1.30 BSC		0.051 BSC	
H	9.40	10.41	0.370	0.410
L	1.40	1.78	0.055	0.070
L3	0.89	2.03	0.035	0.080
L4	-	1.02	-	0.040
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



UNIT: mm

Carrier Tape & Reel Dimensions

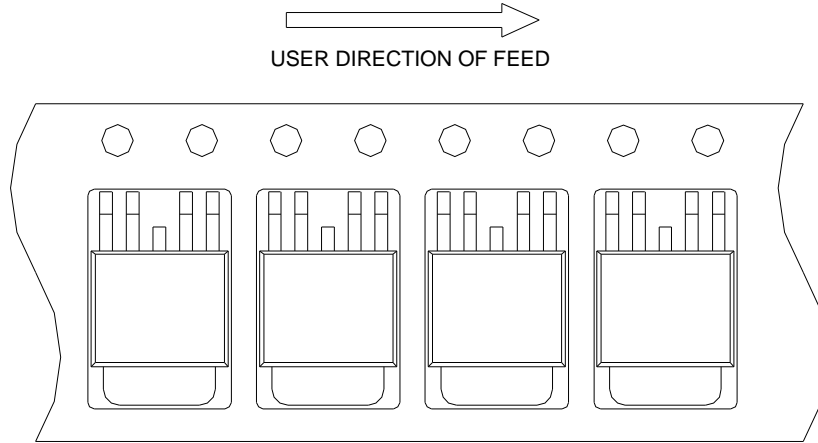


Application	A	H	T1	C	d	D	W	E1	F
TO-252-4	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.80±0.20	10.40±0.20	2.50±0.20

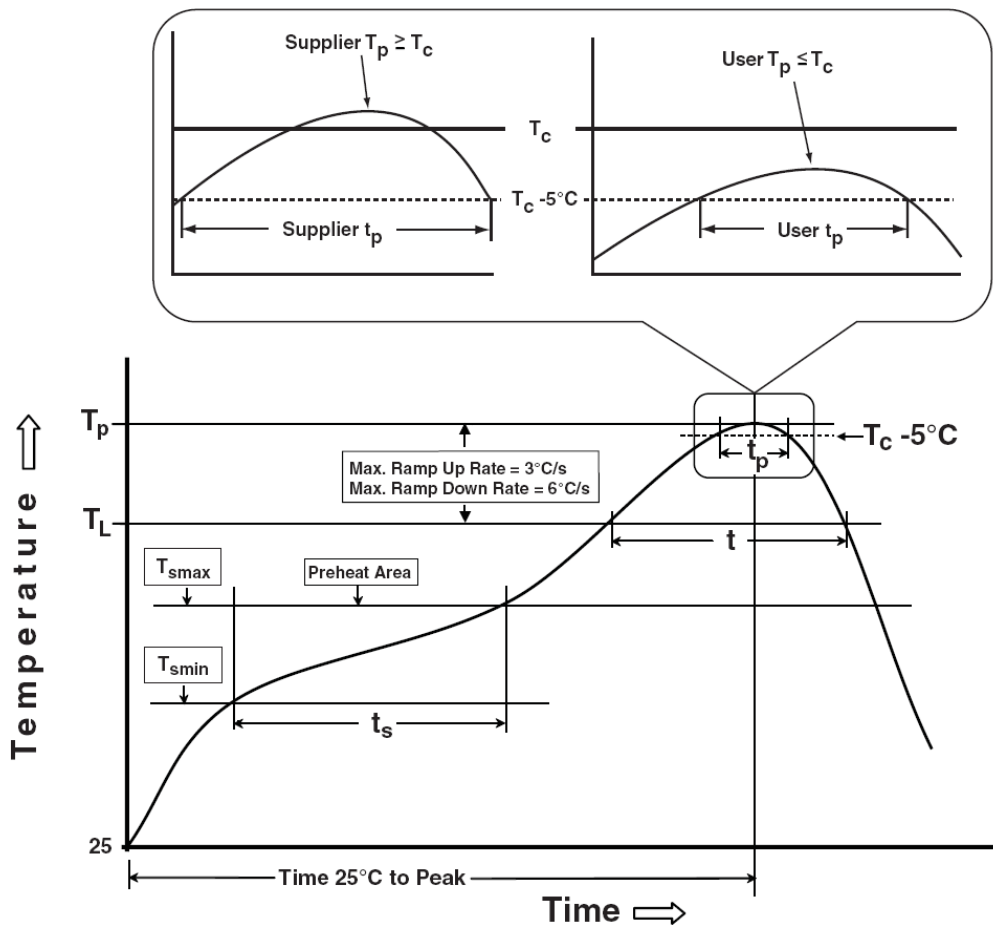
(mm)

Taping Direction Information

TO-252-4



Classification Profile



Disclaimer

Sinopower Semiconductor, Inc. (hereinafter “Sinopower”) has been making great efforts to development high quality and better performance products to satisfy all customers’ needs. However, a product may fail to meet customer’s expectation or malfunction for various situations.

All information which is shown in the datasheet is based on Sinopower’s research and development result, therefore, Sinopower shall reserve the right to adjust the content and monitor the production.

In order to unify the quality and performance, Sinopower has been following JEDEC while defines assembly rule. Notwithstanding all the suppliers basically follow the rule for each product, different processes may cause slightly different results.

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Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HTRB	JESD-22, A108	1000 Hrs, 80% of VDS max @ T_{jmax}
HTGB	JESD-22, A108	1000 Hrs, 100% of VGS max @ T_{jmax}
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C

Customer Service

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