Specification of Programming FLASH

SM7301

1. General Description

The SM7301 is normally shipped with the on-chip FLASH memory array in the erased state (that is, contents = FFH) and ready to be programmed. To programming on-chip FLASH memory, MCU must be in the RESET mode.

2. Pin Assignment and Description

40 Pins DIP	44 Pins QFP	44 Pins PLCC	Name	I/O	Description
1,2,3,4,5,6,7,8	40,41,42,43,44,1,2,3	2,3,4,5,6,7,8,9	P1	I	The low-byte of address (A7-A0), *1
21,22,23,24,25	18,19,20,21,22	24,25,26,27,28	P2	I	The high-byte of address (A12-A8) *1
26,27,28	23,24,25	29,30,31	TST[1:3]	I	Test pin must connect to 0V
32,33,34,35,36,37,38,39	30,31,32,33,34,35,36,37	36,37,38,39,40,41,42,43	P0	I/O	The data bus (D7 – D0)
9	4	10	RES	I	Reset pin, must be in 5V when programming FLASH
19	15	21	X1	I	Crystal in, feed clock into the MCU
31	29	35	EA	I	+11.2V voltage supply in ERASE and PROGRAMMING
40	38	44	VDD	I	+5V voltage supply.
20	16	22	VSS	I	Sink voltage, Ground
30	27	33	ALE	I	Flash chip enable
29	26	32	PSEN	I	Flash data output enable
10	5	11	P3.0	I	Enable Chip-Erase Mode (low active)
13	9	15	P3.3	I	Enable Programming Mode (low active)
14	10	16	P3.4	I	Enable Programming Protect bit (low active)
15	11	17	P3.5	I	Enable Flash Mode Select
11,12	7,8	13,14	P3.1,P3.2	I	Must set the HIGH, When enter Programming FLASH
18	14	20	X2	O	Crystal out, Let floating
16, 17,	12,13	18,19	P3.6, P3.7	O	**Let all unused pins are floating**.
	17,28,39,6	23,34,1,12	P4	O	**Let all unused pins are floating**.

*1 The size of FLASH RAM in SM7301 is 8K bytes. So the address (P2.7-P2.0 P1.7-P1.0) is from 0x0000 to 0x1FFF.

3. Programming FLASH Algorithm

Before programming the SM7301, the address, data and control signals should be set up according the FLASH programming table and Figure 1. To programming the SM7301, take the following the steps.

1. Provide the +5V to VCC
2. Feed clocks into X1 pins and RES pins
3. Wait for 4096 clocks at least.
4. Raise V_{PP} to 11.2V for the ease, programming, and programming protect mode, Wait 10ms for stable power.
5. Activate the correct combination of control signals (P0, P1, P2, P3.0-P3.5 and PSEN)
6. Set ALE to Low

FLASH programming mode table

Mode	RST	PSEN	ALE	P3.0	P3.1	P3.2	P3.3	P3.4	P3.5	Description
Chip Erase	H	H		L	H	H	H	H	L	Erase all area of on-chip FLASH
Program	H	H		H	H	H	L	H	L	Programming data of on-chip FLASH
Protect	H	H		H	H	H	H	L	L	Programming protect bit of on-chip FLASH
Verified	H	L		H	H	H	H	H	H	Read data from on-chip FLASH

*** X1 always feed a clock into it.

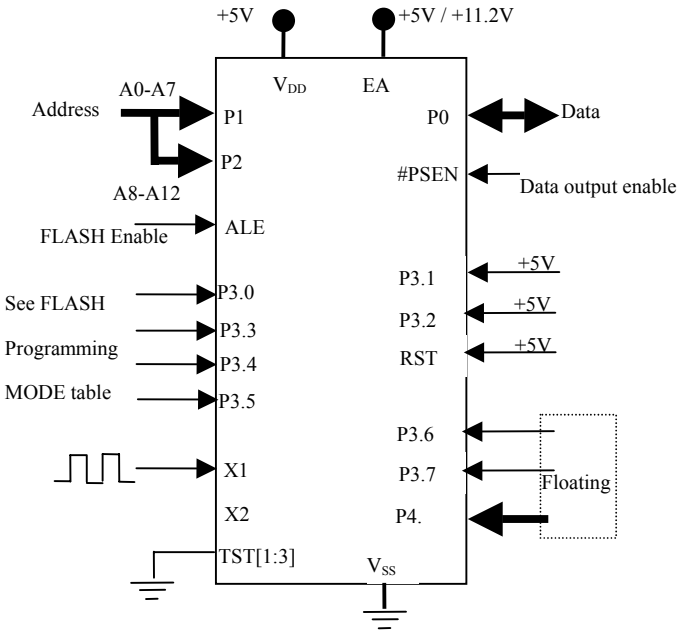


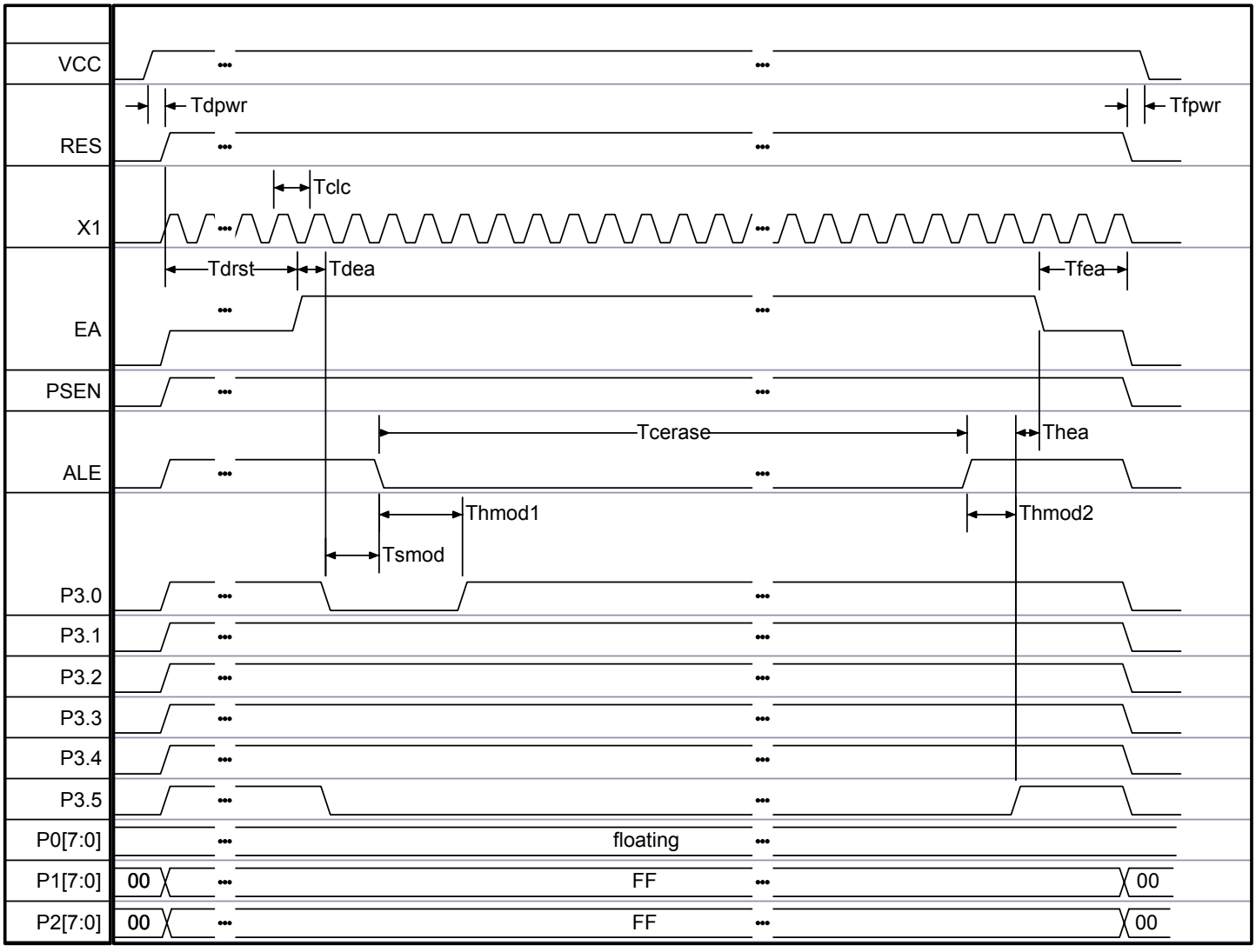
Figure 1. Programming the FLASH Memory

4. DC Characteristics

Symbol	Min	Typ.	Max	Unit	Description
V_{DD}	4.8	5.0	5.2	V	The power must be
V_{EA}	11.0	11.2	11.4	V	The EA should set to 11.2V during the CHIP ERASE, PROGRAM and PROTECT mode
VIH	2.0		V_{DD}+0.5	V	The input high level of input pins
VIL	-0.5		0.8	V	The input low level of input pins

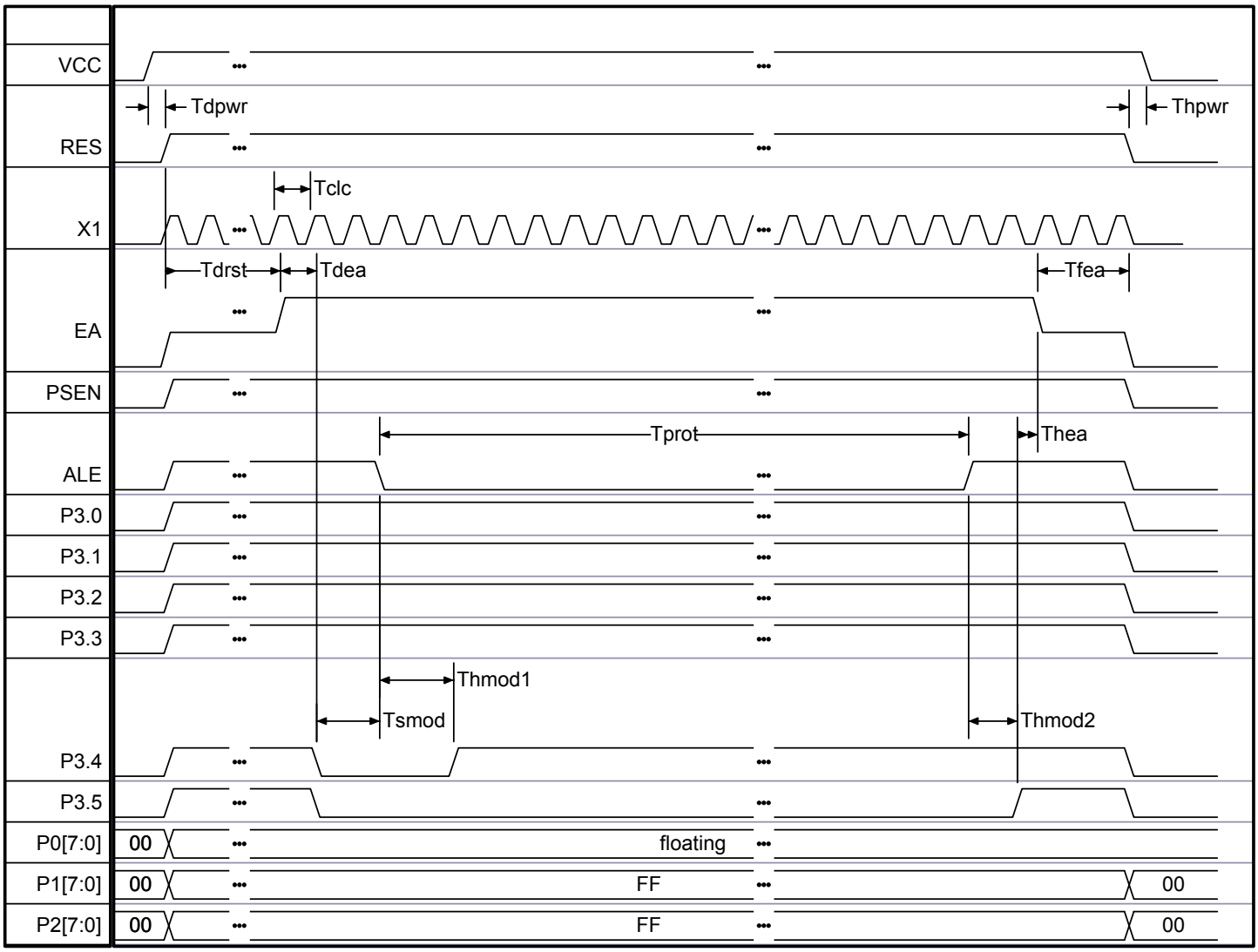
5. AC Characterictics

5.1. Chip Erase Mode



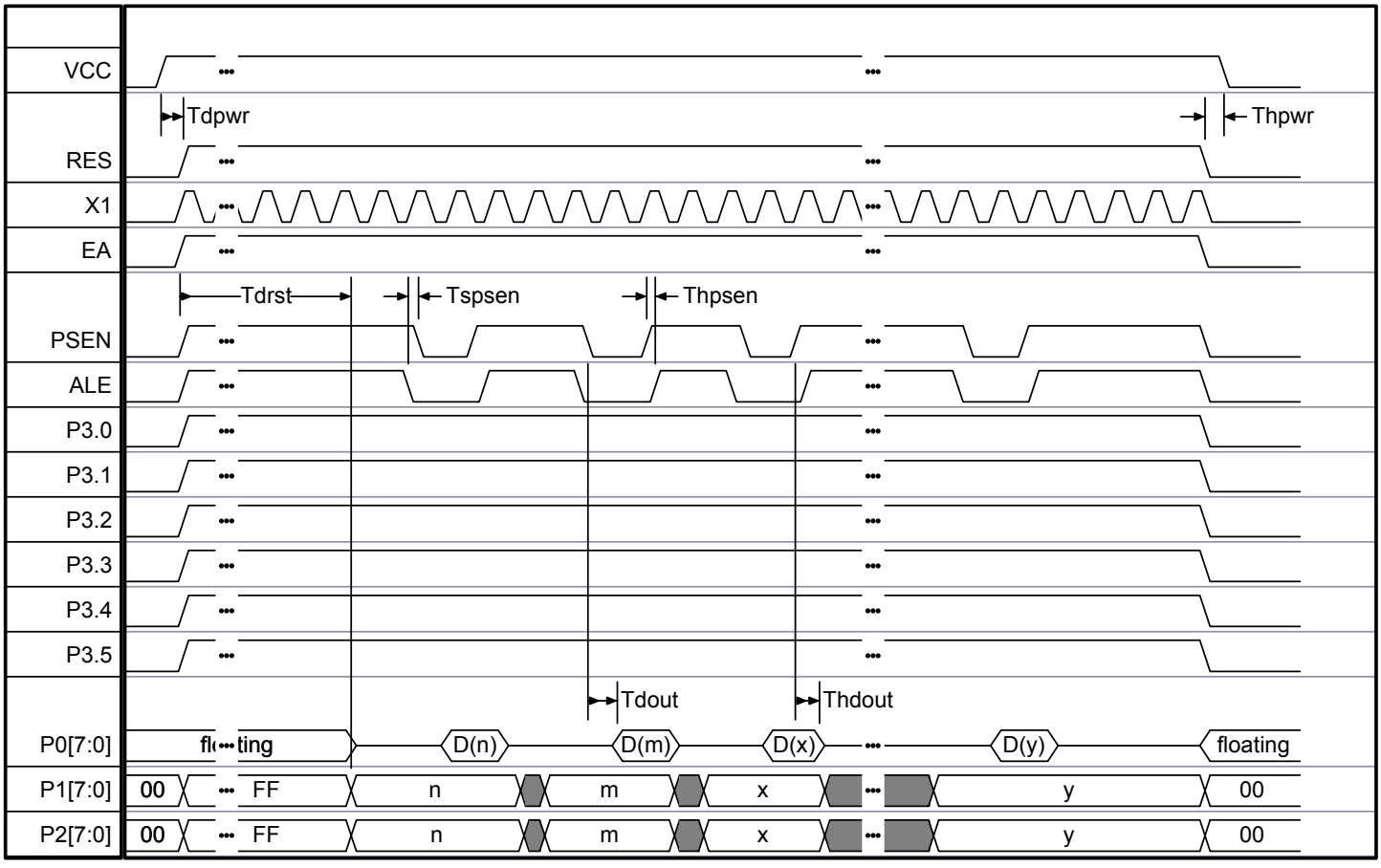
Symbol	Min	Typ	Max	Units	Description
1/Tclc	1		12	MHz	The frequency feed into X1 Pin
Tdrst	4096			Tclc	Wait for timer of reset
Tdpwr	10			ms	Signal delay for waiting the stable power (5V)
Tdea	10			ms	Signal delay for waiting the stable power(11.2V)
Tsmod	5			us	Setup-Time from change of mode pins (P3.0-P3.5) to ALE
Tcrease	1			s	Timing of erasing all area of on-chip FLASH
Thmod1	5			us	Hold time from falling edge of ALE to change of mode pins (P3.0-P3.4)
Thmod2	1		5	us	Hold time from rising edge of ALE to change of P3.5
Thea	1			us	Hold time form model change to release EA (from 11.2V to 5V)
Tfea	10			ms	Hold time for change EA, The voltage of EA must keep 5V in this time.
Thpwr	1			us	Timing between falling edge from falling edge of all signal to falling edge of Vcc

5.2. Protect Mode



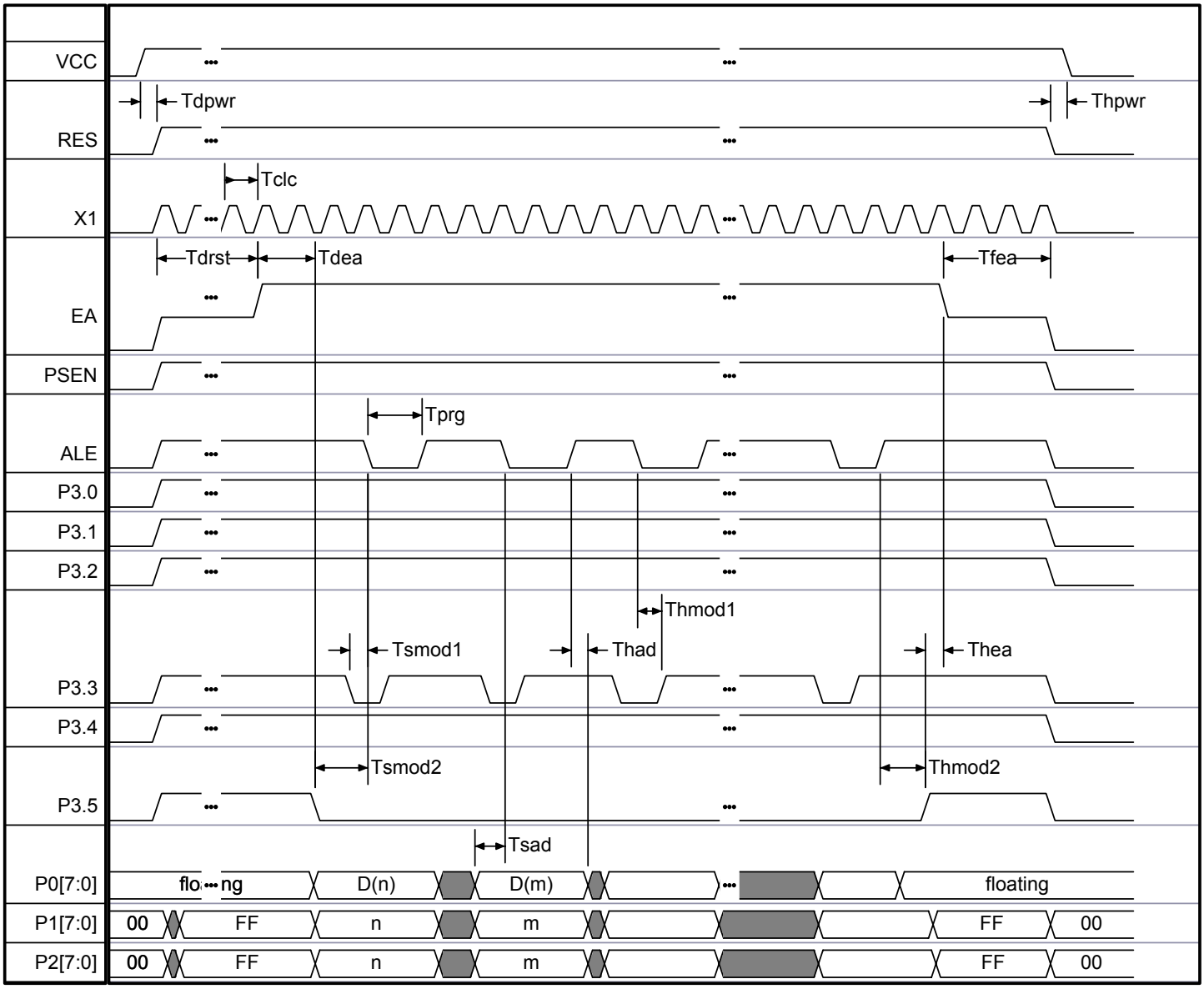
Symbol	Min	Typ	Max	Units	Description
1/Tclc	1		12	MHz	The frequency feed into X1 Pin
Tdrst	4096			Tclc	Wait for timer of reset
Tdpwr	10			ms	Delay for waiting the stable power(5V)
Tdea	10			ms	Delay for waiting the stable power(11.2V)
Tsmod	5			us	Setup timing from change of mode pins (P3.0-P3.5) to ALE
Tprot	200			us	Timing of programming PROTECT bit
Thmod1	5			us	Hold time form falling edge of ALE to falling edge of P3.0-P3.4
Thmod2	1		5	us	Hold time from rising edge of ALE to P3.5
Thea	1			us	Hold time form model change to release EA (from 11.2V to 5V)
Tfea	10			ms	Hold time for change internal voltage from high (11.2) to 5V
Thpwr	1			us	Timing between falling edge of VCC (+5V) and falling edge of all other pins.

5.3. Verified Mode



Symbol	Min	Typ	Max	Units	Description
1/Tclc	1		12	MHz	The frequency feed into X1 Pin
Tdrst	4096			Tclc	Wait for timer of reset
Tdpwr	10			ms	Delay for waiting the stable power(5V)
Tdpsen	1			us	Setup up timing for PSEN to ALE
Thpsen	1			us	Hold timing from edge of ALE to change of psen
Tsad	1			us	Setup timing from ADDRESS to ALE
Thad	1			us	Hold timing from edge of ALE to ADDRESS
Tdout	1			us	Data output delay
Thdout			10	ns	Data bus hold timing
Thpwr	1			us	Timing between falling edge of VCC (+5V) and falling edge of all other pins.

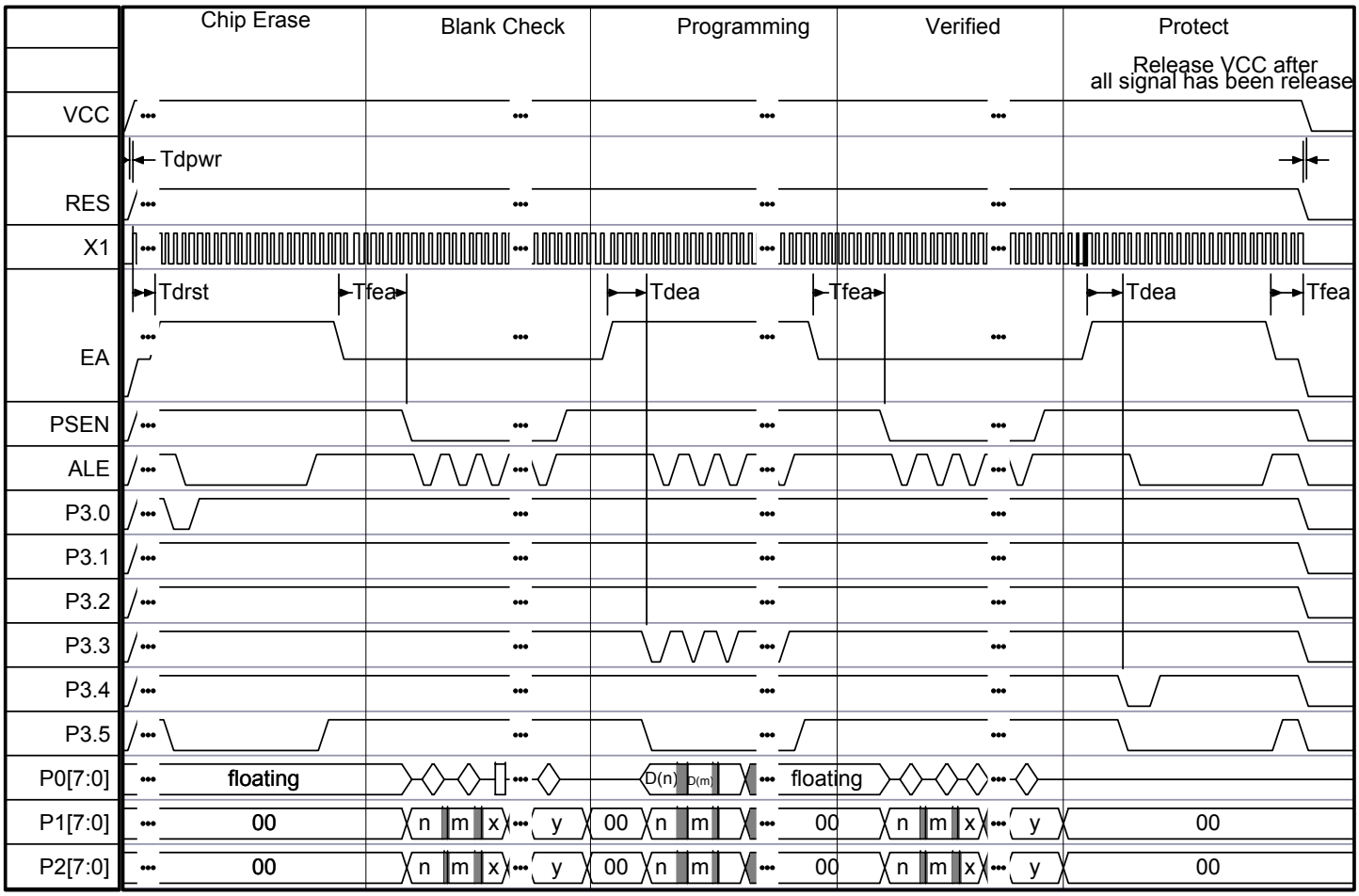
5.4. Programming Mode



Symbol	Min	Typ	Max	Units	Description
1/Tclc	1		12	MHz	The frequency feed into X1 Pin
Tdrst	4096			Tclc	Wait for timer of reset
Tdpwr	10			ms	Delay for waiting the stable power(5V)
Tdea	10			ms	Delay for waiting the stable power(11.2V)
Tsmod	1			us	Setup time from change of mode pins (P3.0-P3.5) to ALE
Tprg	35			us	Timing for program 1 byte
Thmod	1			us	Hold time from edge of ALE to change of mode pins (P3.0-P3.5)

Symbol	Min	Typ	Max	Units	Description
Tsad	1			us	Setup time from the edge of ADDRESS and DATA to ALE
Thad	1			us	Hold time from the edge of ALE to ADDRESS and DATA
Thea	1			us	Hold time form model change to release EA (from 11.2V to 5V)
Tfea	10			ms	Hold time for change for EA change form 11.2V -> 5V -.> 0V
Thpwr	1			us	Timing between falling edge of VCC (+5V) and falling edge of all other pins.

5.5. Combine All Mode



Symbol	Min	Typ	Max	Units	Description
1/Tclc	1		12	MHz	The frequency feed into X1 Pin
Tdpwr	10			ms	Delay for waiting the stable power(5V)
Tdrst	4096			Tclc	Wait for timer of reset
Tdea	10			ms	Delay from the rising of EA (from 5V to 11.2V) to any change of P3.0-P3.5
Thea	10			ms	Hold timing from falling edge of EA (from 11.2V to 5V) to any other pin change.
Tfea	10			ms	Hold timing of EA form 11.2V -> 5V -> 0V
Thpwr	1			us	Timing between falling edge of VCC (+5V) and falling edge of all other pins.