

Dual Enhancement Mode MOSFET (N-and P-Channel)

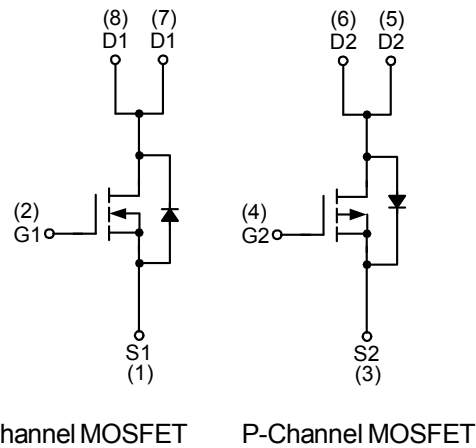
Features

- N Channel**
 30V/20A^a,
 $R_{DS(ON)} = 9.6m\Omega$ (max.) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 13m\Omega$ (max.) @ $V_{GS} = 4.5V$
- P Channel**
 -30V/-20A^a,
 $R_{DS(ON)} = 19m\Omega$ (max.) @ $V_{GS} = -10V$
 $R_{DS(ON)} = 34m\Omega$ (max.) @ $V_{GS} = -4.5V$
- 100% UIS + R_g Tested
- Reliable and Rugged
- Lead Free Available (RoHS Compliant)


Applications

- Synchronous Rectification.
- Motor Control.
- High Current, High Speed Switching.
- Portable equipment application.

Pin Description



Ordering and Marking Information

<p>SM7309CS □□□-□□□</p> <div style="margin-left: 20px;"> <p>└─ Assembly Material</p> <p>└─ Handling Code</p> <p>└─ Temperature Range</p> <p>└─ Package Code</p> </div>	<p>Package Code KP : DFN5x6C-8_EP2</p> <p>Operating Junction Temperature Range C : -55 to 150 °C</p> <p>Handling Code TR : Tape & Reel</p> <p>Assembly Material G : Halogen and Lead Free Device</p>
<p>SM7309CS KP :</p> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 10px;">  </div>	<p>XXXXX - Date Code</p>

Note : SINOPOWER lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. SINOPOWER lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. SINOPOWER defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

SINOPOWER reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		N Channel	P Channel	Unit
Common Ratings					
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		± 20	± 25	
T_J	Maximum Junction Temperature		150		$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-55 to 150		
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$	3	-3	A
I_D	Continuous Drain Current(Wire Bond Limited)	$T_C=25^\circ\text{C}$	20 ^a	-20 ^a	A
		$T_C=100^\circ\text{C}$	20 ^a	-16	
I_D	Continuous Drain Current(Silicon Limited)	$T_C=25^\circ\text{C}$	35	-25	A
		$T_C=100^\circ\text{C}$	22	-16	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	19	19	W
		$T_C=100^\circ\text{C}$	7.7	7.7	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	Steady State	6.5	6.5	$^\circ\text{C/W}$
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	9.3	-6.8	A
		$T_A=70^\circ\text{C}$	7.4	-5.4	
I_{DM}^a	Pulsed Drain Current	$T_A=25^\circ\text{C}$	37	-28	A
P_D	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	1.42	1.42	W
		$T_A=70^\circ\text{C}$	0.9	0.9	
$R_{\theta JA}^b$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{s}$	45	45	$^\circ\text{C/W}$
		Steady State	88	88	$^\circ\text{C/W}$
I_{AS}^c	Avalanche Current, Single pulse	$L=0.1\text{mH}$	23	-24	A
E_{AS}^c	Avalanche Energy, Single pulse	$L=0.1\text{mH}$	26.45	-28.8	mJ

Note a : Max. continuous current is limited by bonding wire.

Note b : Pulse width limited by max. junction temperature.

Note c : Surface Mounted on 1in^2 pad area, steady state $t = 999\text{s}$.

Note d : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_J=25^\circ\text{C}$)

N Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	N Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V	-	-	1	μA
		T _J =85°C	-	-	30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1.5	1.8	2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^e	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =8A	-	8	9.6	mΩ
		T _J =125°C	-	11.9	-	
		V _{GS} =4.5V, I _{DS} =5A	-	10	13	
Gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =5A	-	15	-	S
Diode Characteristics						
V _{SD} ^e	Diode Forward Voltage	I _{SD} =3A, V _{GS} =0V	-	0.75	1.1	V
t _{rr}	Reverse Recovery Time	I _{SD} =8A, dI _{SD} /dt=100A/μs	-	11.7	-	ns
t _a	Charge Time		-	4.8	-	
t _b	Discharge Time		-	6.9	-	
Q _{rr}	Reverse Recovery Charge		-	1.7	-	
Dynamic Characteristics^f						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	0.9	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, Frequency=1.0MHz	-	940	-	pF
C _{oss}	Output Capacitance		-	150	-	
C _{rss}	Reverse Transfer Capacitance		-	100	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =15V, R _L =15Ω, I _{DS} =1A, V _{GEN} =10V, R _G =1Ω	-	11.9	-	ns
t _r	Turn-on Rise Time		-	10.1	-	
t _{d(OFF)}	Turn-off Delay Time		-	22	-	
t _f	Turn-off Fall Time		-	5	-	
Gate Charge Characteristics^f						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _{DS} =8A	-	8.7	-	nC
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _{DS} =8A	-	18	-	
Q _{gth}	Threshold Gate Charge		-	1.24	-	
Q _{gs}	Gate-Source Charge		-	2	-	
Q _{gd}	Gate-Drain Charge		-	4	-	

Note e : Pulse test ; pulse width≤300μs, duty cycle≤2%.

Note f : Guaranteed by design, not subject to production testing.

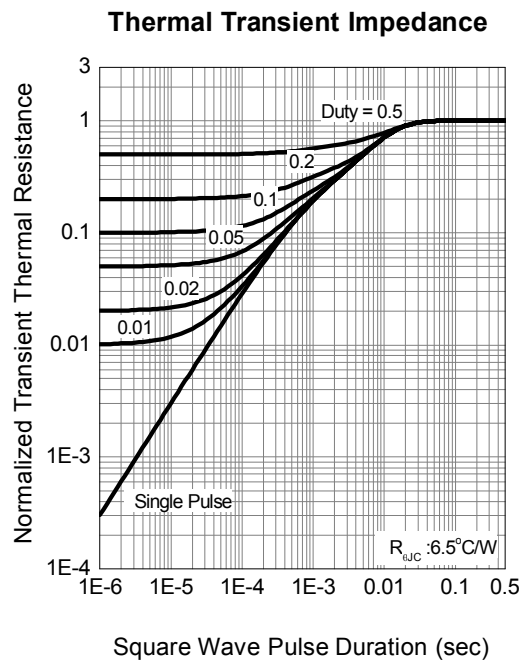
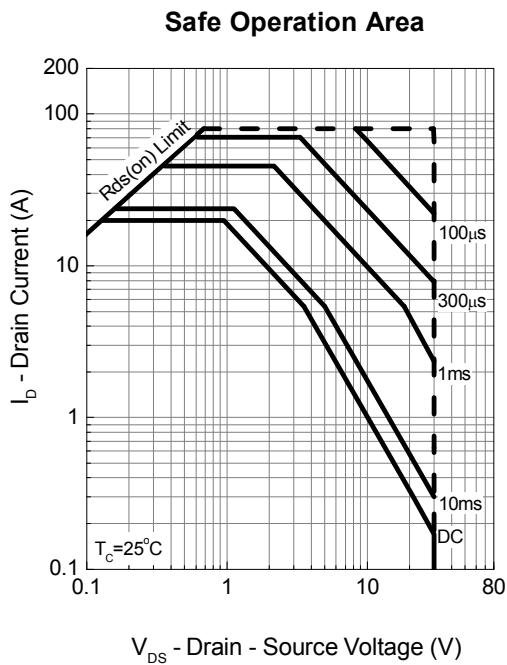
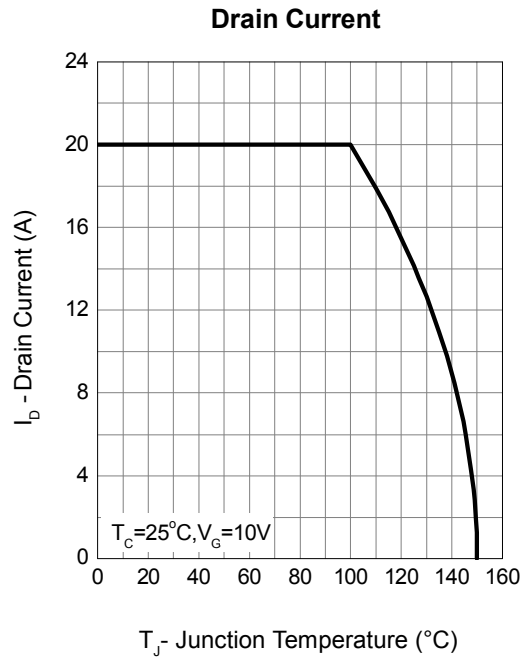
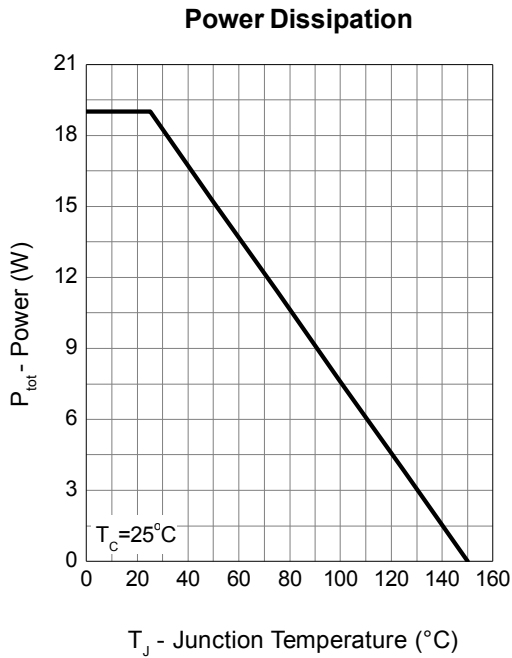
P Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	P Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250μA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V T _J =85°C	-	-	-1	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250μA	-1.5	-2	-2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^e	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-10A T _J =125°C	-	15	19	mΩ
		V _{GS} =-4.5V, I _{DS} =-5A	-	25	34	
Gfs	Forward Transconductance	V _{DS} =5V, I _{DS} =5A	-	13	-	S
Diode Characteristics						
V _{SD} ^e	Diode Forward Voltage	I _{SD} =-1A, V _{GS} =0V	-	-0.75	-1	V
t _{rr}	Reverse Recovery Time	I _{SD} =-10A, dI _{SD} /dt=100A/μs	-	26	-	ns
t _a	Charge Time		-	8	-	
t _b	Discharge Time		-	18	-	
Q _{rr}	Reverse Recovery Charge		-	7	-	nC
Dynamic Characteristics^f						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	3.4	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, Frequency=1.0MHz	-	1000	-	pF
C _{oss}	Output Capacitance		-	210	-	
C _{rss}	Reverse Transfer Capacitance		-	150	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =-15V, R _L =15Ω, I _{DS} =-1A, V _{GEN} =-10V, R _G =6Ω	-	11	-	ns
t _r	Turn-on Rise Time		-	12	-	
t _{d(OFF)}	Turn-off Delay Time		-	26	-	
t _f	Turn-off Fall Time		-	12	-	
Gate Charge Characteristics^f						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-4.5V, I _{DS} =-10A	-	9.6	-	nC
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _{DS} =-10A	-	21	-	
Q _{gth}	Threshold Gate Charge		-	1.5	-	
Q _{gs}	Gate-Source Charge		-	3.5	-	
Q _{gd}	Gate-Drain Charge		-	5.9	-	

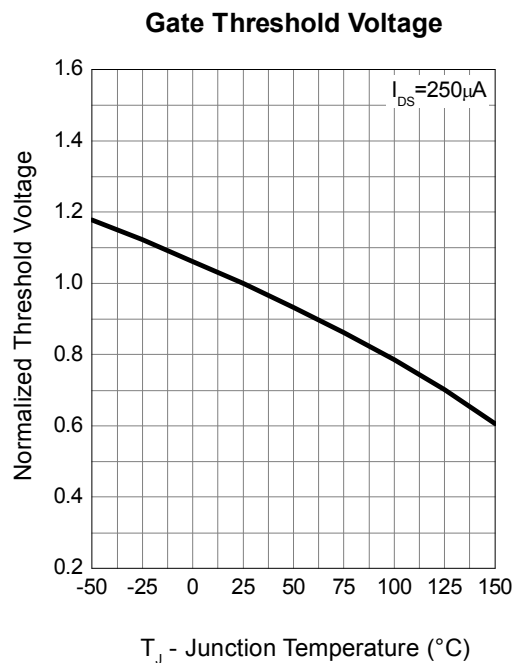
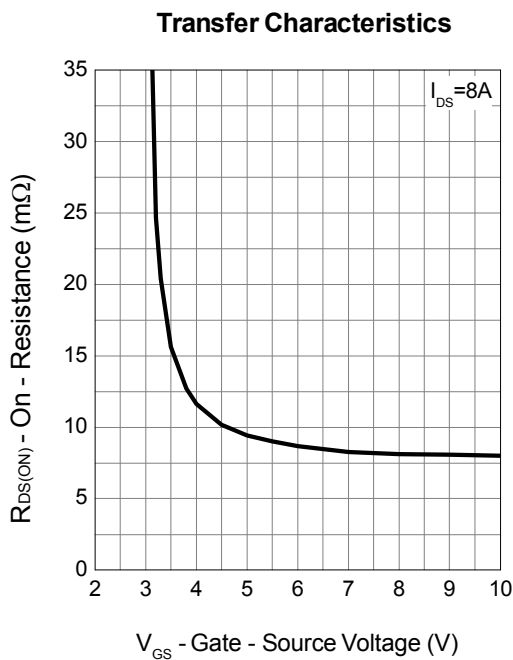
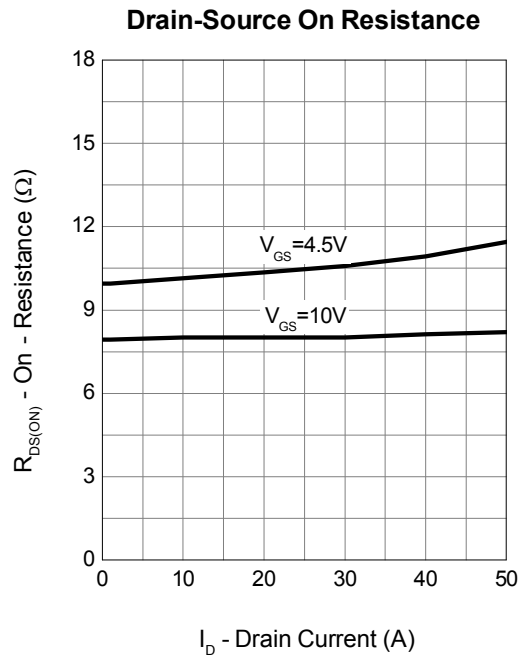
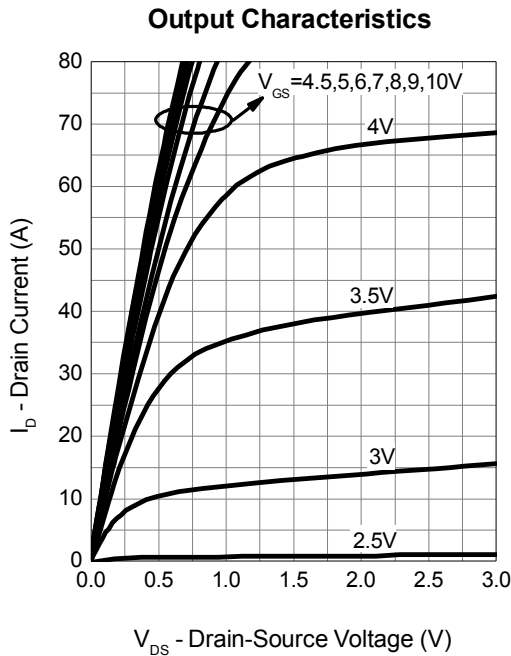
Note e : Pulse test ; pulse width ≤ 300μs, duty cycle ≤ 2%.

Note f : Guaranteed by design, not subject to production testing.

N Channel Typical Operating Characteristics

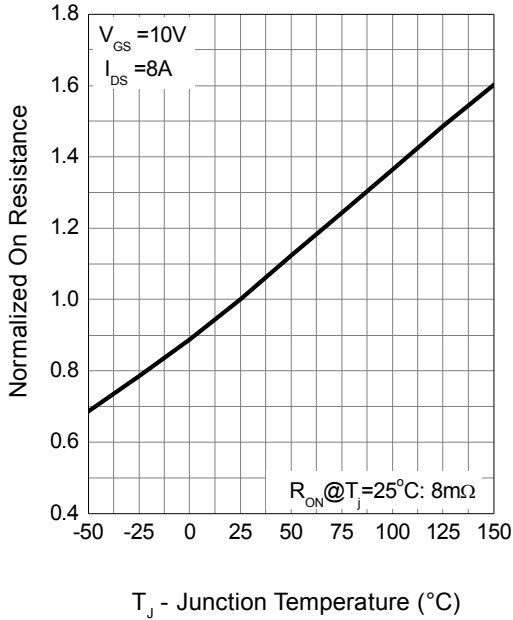


N Channel Typical Operating Characteristics (Cont.)

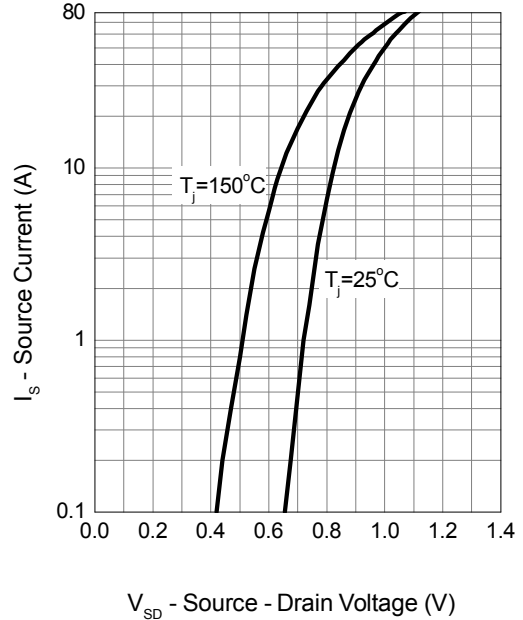


N Channel Typical Operating Characteristics (Cont.)

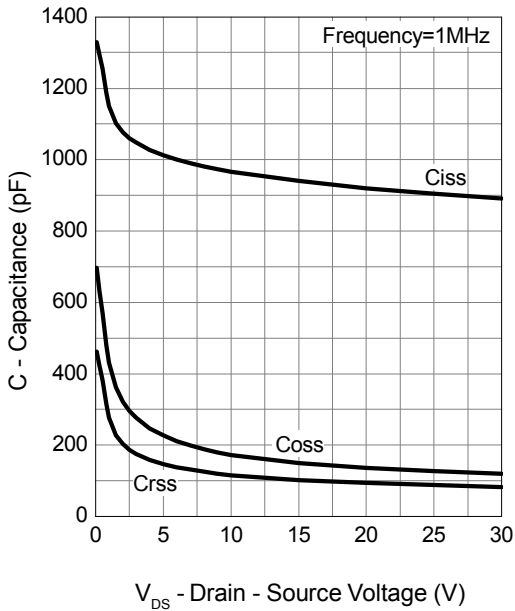
Drain-Source On Resistance



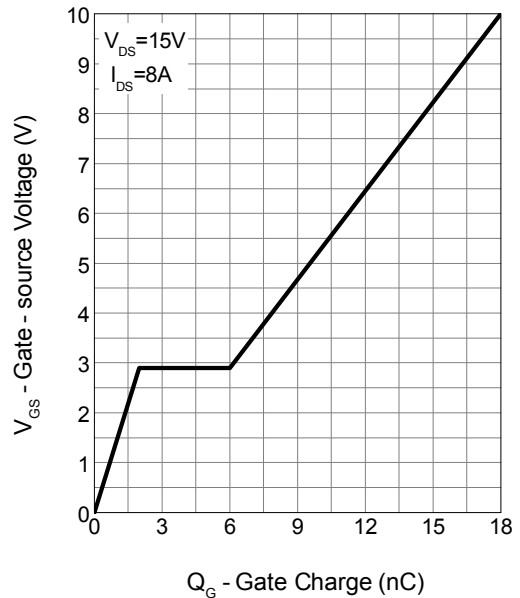
Source-Drain Diode Forward



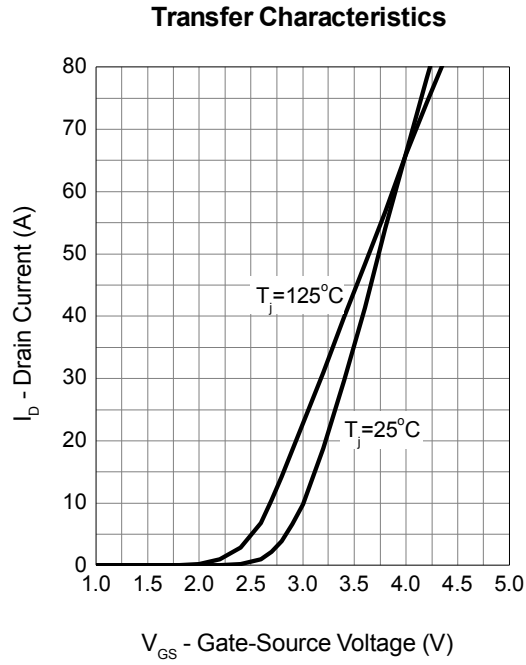
Capacitance



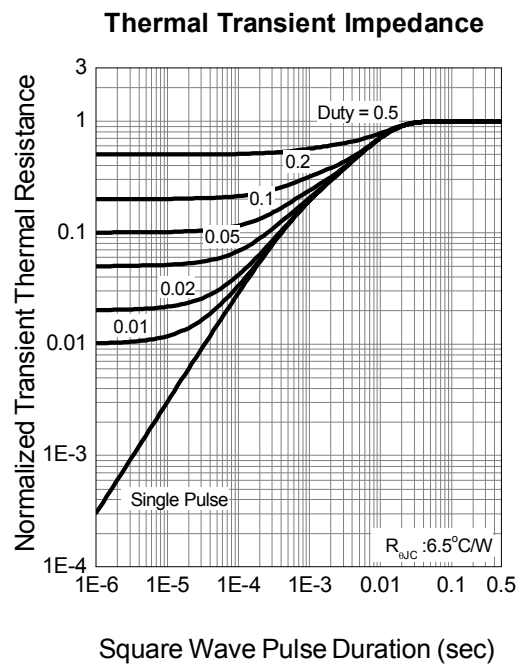
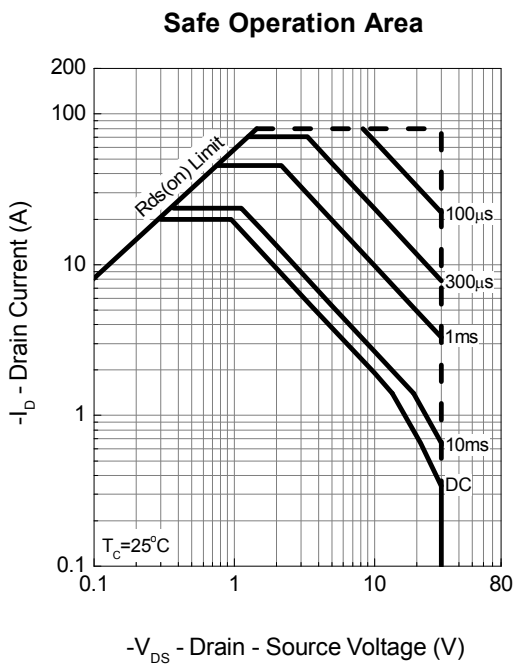
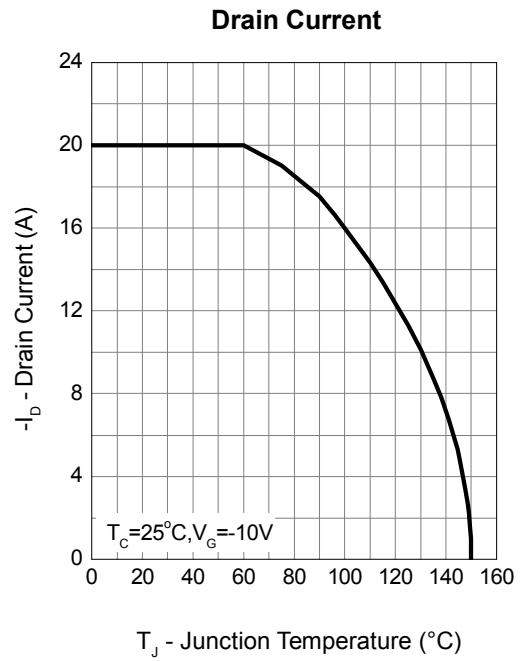
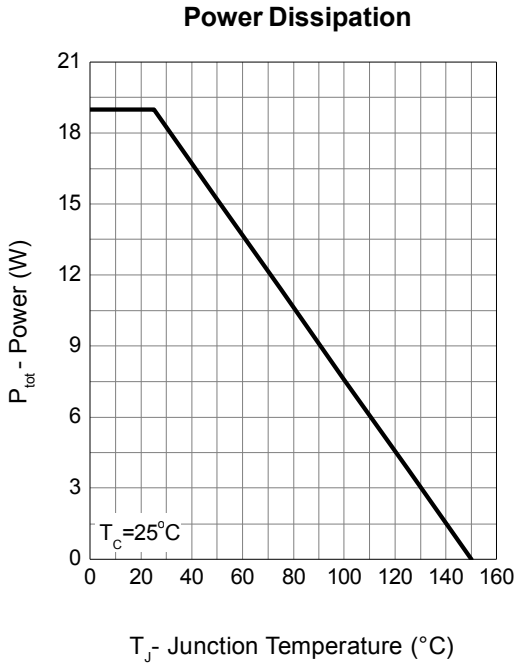
Gate Charge



N Channel Typical Operating Characteristics (Cont.)

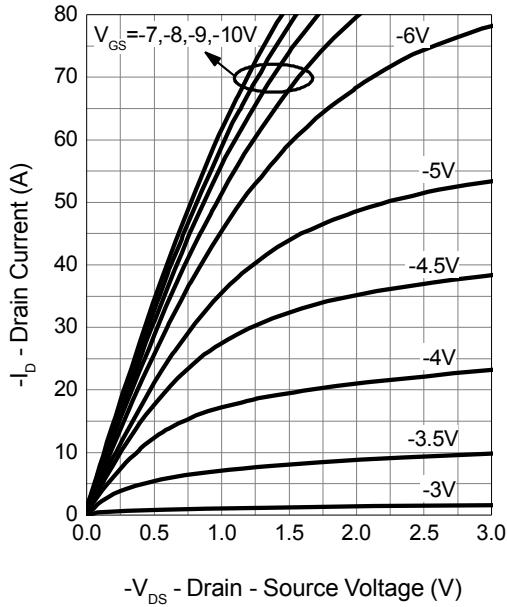


P Channel Typical Operating Characteristics

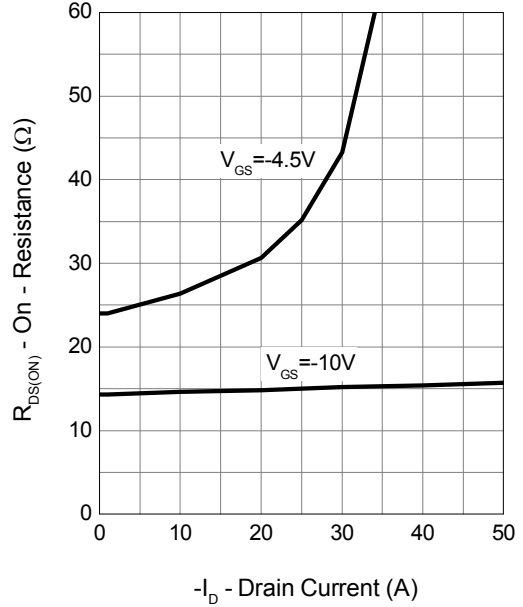


P Channel Typical Operating Characteristics (Cont.)

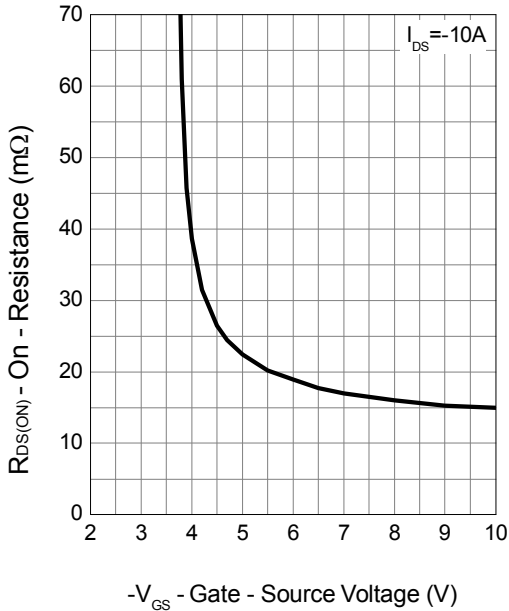
Output Characteristics



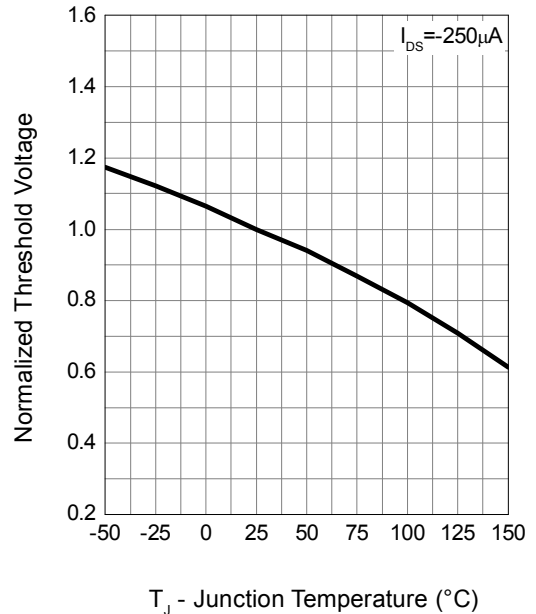
Drain-Source On Resistance



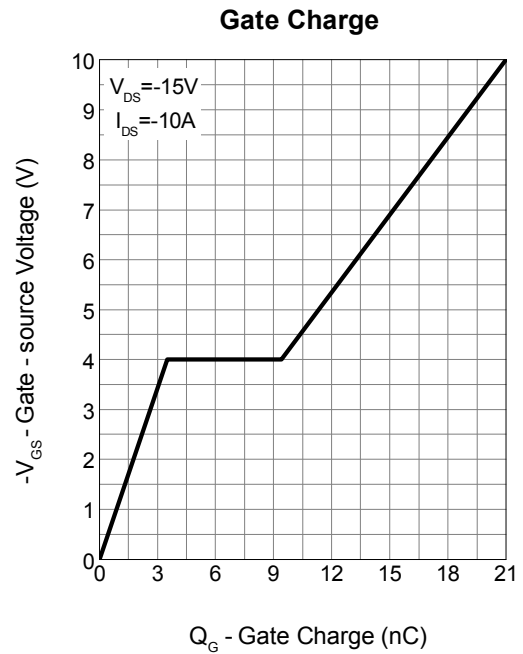
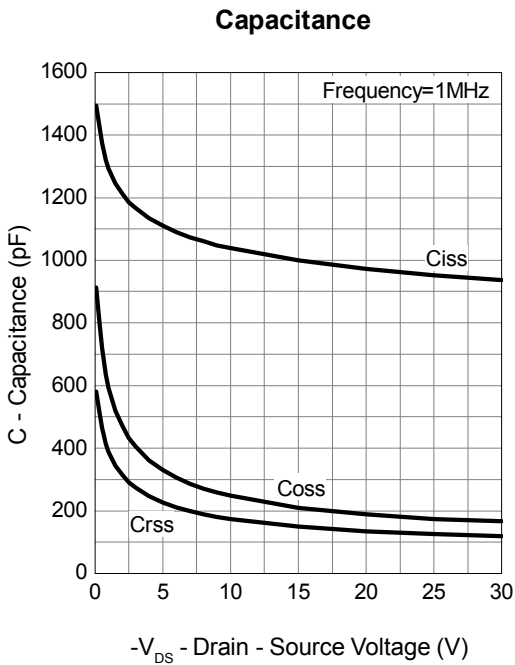
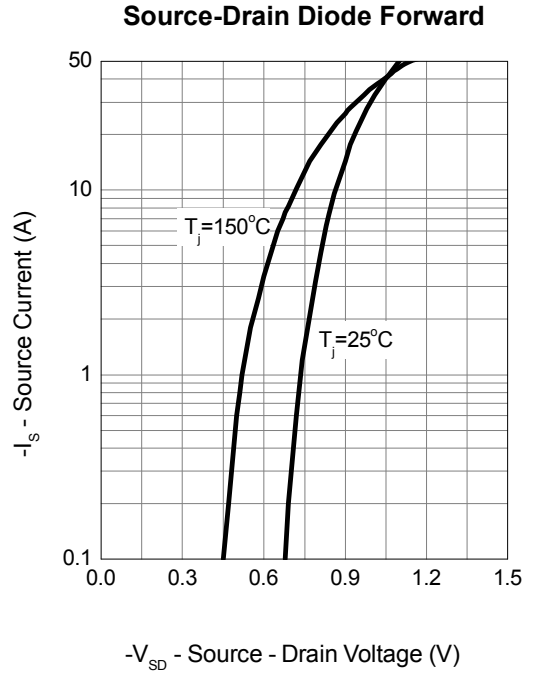
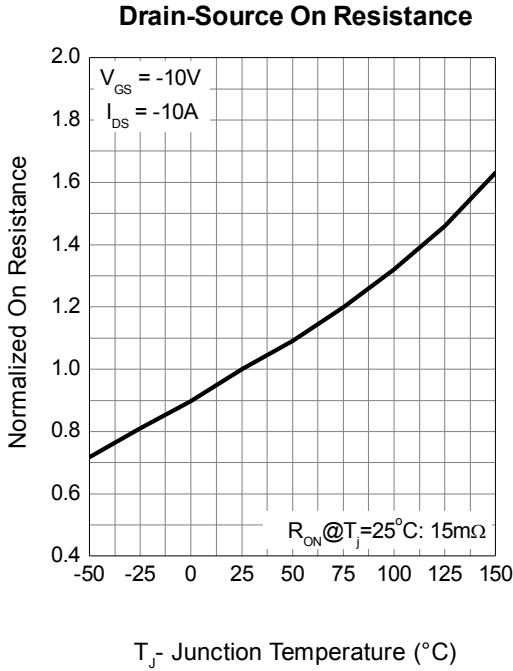
Transfer Characteristics



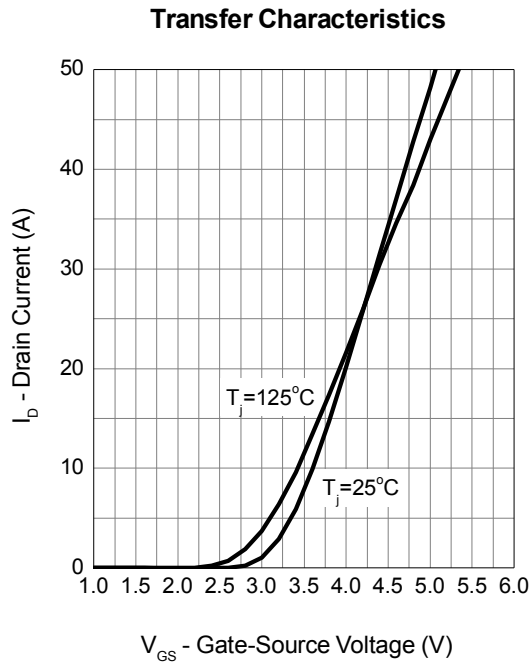
Gate Threshold Voltage



P Channel Typical Operating Characteristics (Cont.)

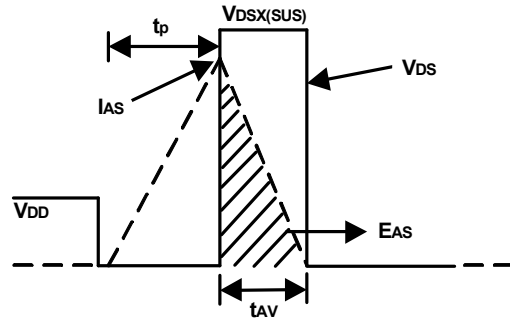
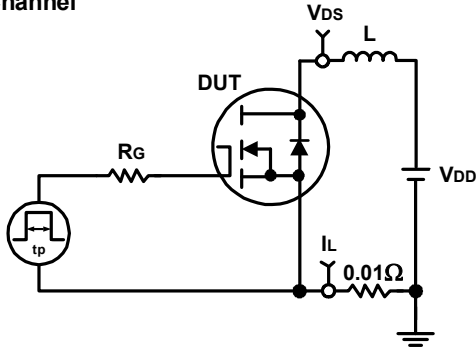


P Channel Typical Operating Characteristics (Cont.)

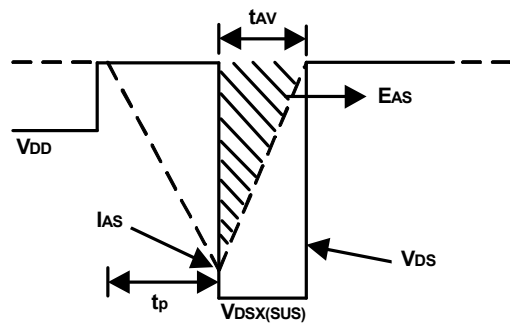
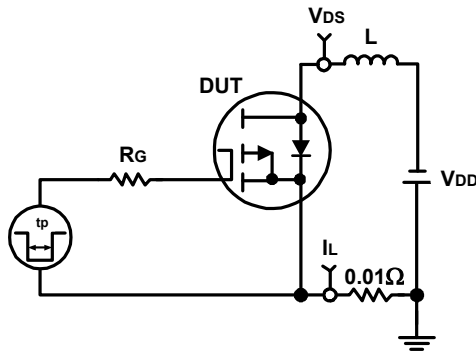


Avalanche Test Circuit and Waveforms

N Channel

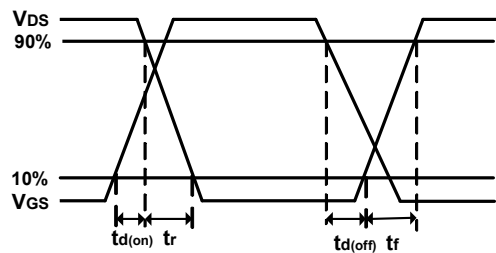
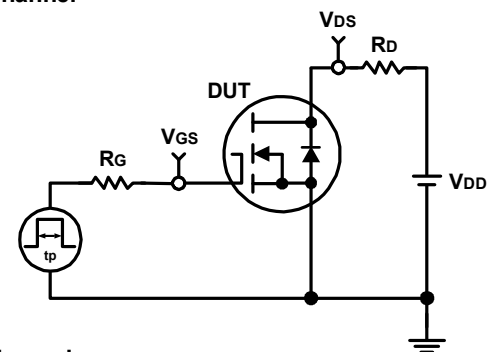


P Channel

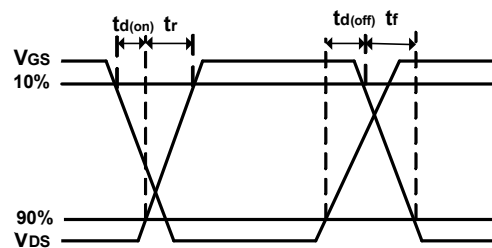
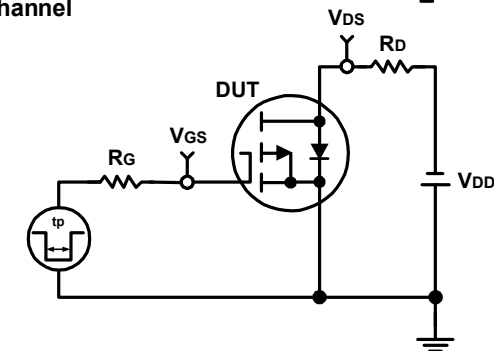


Switching Time Test Circuit and Waveforms

N Channel



P Channel



Disclaimer

Sinopower Semiconductor, Inc. (hereinafter “Sinopower”) has been making great efforts to development high quality and better performance products to satisfy all customers’ needs. However, a product may fail to meet customer’s expectation or malfunction for various situations.

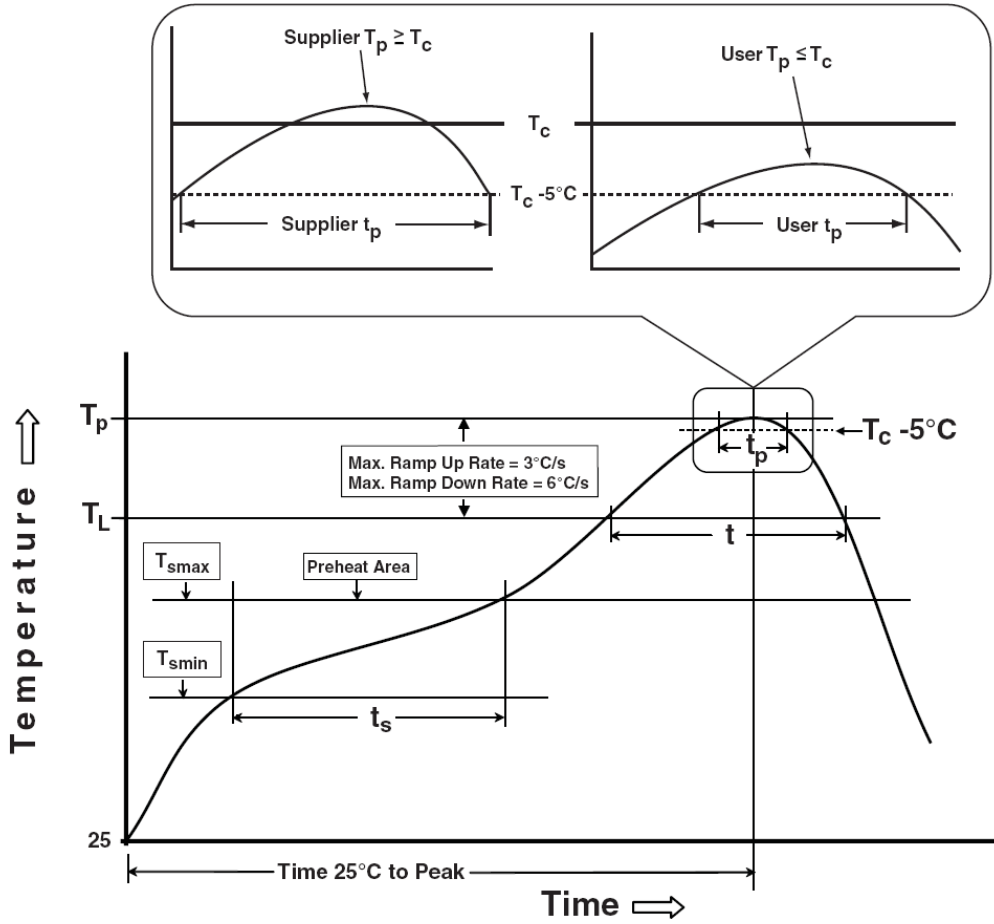
All information which is shown in the datasheet is based on Sinopower’s research and development result, therefore, Sinopower shall reserve the right to adjust the content and monitor the production.

In order to unify the quality and performance, Sinopower has been following JEDEC while defines assembly rule. Notwithstanding all the suppliers basically follow the rule for each product, different processes may cause slightly different results.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the products. Sinopower does not grant customers explicitly or implicitly, any license to use or exercise intellectual property or other rights held by Sinopower and other parties. Sinopower shall bear no responsible whatsoever for any dispute arising from the use of such technical information.

The products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability, such as the failure or malfunction of which any may result in a direct threat to human life or a risk of human injury. Sinopower shall bear no responsibility in any way for use of any of the products for the above special purposes. If a product is intended to use for any such special purpose, such as vehicle, military, or medical controller relevant applications, please contact Sinopower sales representative before purchasing.

Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HTRB	JESD-22, A108	1000 Hrs, 80% of VDS max @ T_{jmax}
HTGB	JESD-22, A108	1000 Hrs, 100% of VGS max @ T_{jmax}
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C

Customer Service

Sinopower Semiconductor, Inc.

5F, No. 6, Dusing 1St Rd., Hsinchu Science Park,

Hsinchu, 30078, Taiwan

TEL: 886-3-5635818 Fax: 886-3-5635080