LYNX FAMILY

SM750

Lynx Express 2D Multimedia Mobile Display Controller Datasheet

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Revision No.	Date	Note
0.1	June 2009	First release
0.2	Dec 2009	Second release
0.3	April 2010	Third release
0.4	June 2010	Forth release
0.5	Dec 2010	Design CD update
1.0	May 2011	Add marking and ordering information
1.1	Aug 2011	- Update Figure 12, the ending address of the 2D Engine Data Port change to “0x120000” from “0x150000” - Update CSR08 register descriptions and power-on default value - Add MVDD and MVDD2 DC characteristics in Table 18 and Table 19
1.2	Jan 2012	- Added Standard VGA Register in 2.3.
1.3	Jun 2012	- Updated Top Marking in 13.2 - Updated Product Ordering Information in 14
1.4	Sep 2012	- Fixed bit names in 2.2, 3.2, 4.1, 6.2, 7, and 9.3

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1. General Description

1.1 Overview

The SM750 is a PCI Express 2D multimedia mobile display controller device, packaged in a 265-pin BGA. Designed to complement needs for the embedded industry, it provides video and 2D capability. To help reduce system costs, it supports a wide variety of I/O, including analog RGB and digital LCD Panel interfaces, two Zoom Video interfaces, and Pulse Width Modulation (PWM). There are additional GPIO bits that can be used to interface to external devices as well.

The 2D engine includes a front-end color space conversion with 4:1 and 1:8 scaling support. The video engine supports two different video outputs (Dual Monitor), at 8-bit, 16-bit, or 32-bit per pixel and a 3-color hardware cursor per video output. The LCD panel video pipe supports a back-end YUV color space conversion with 4:1 and 1:212 scaling. A Zoom Video (ZV) port is also included to interface to external circuitry for MPEG decode or TV input.

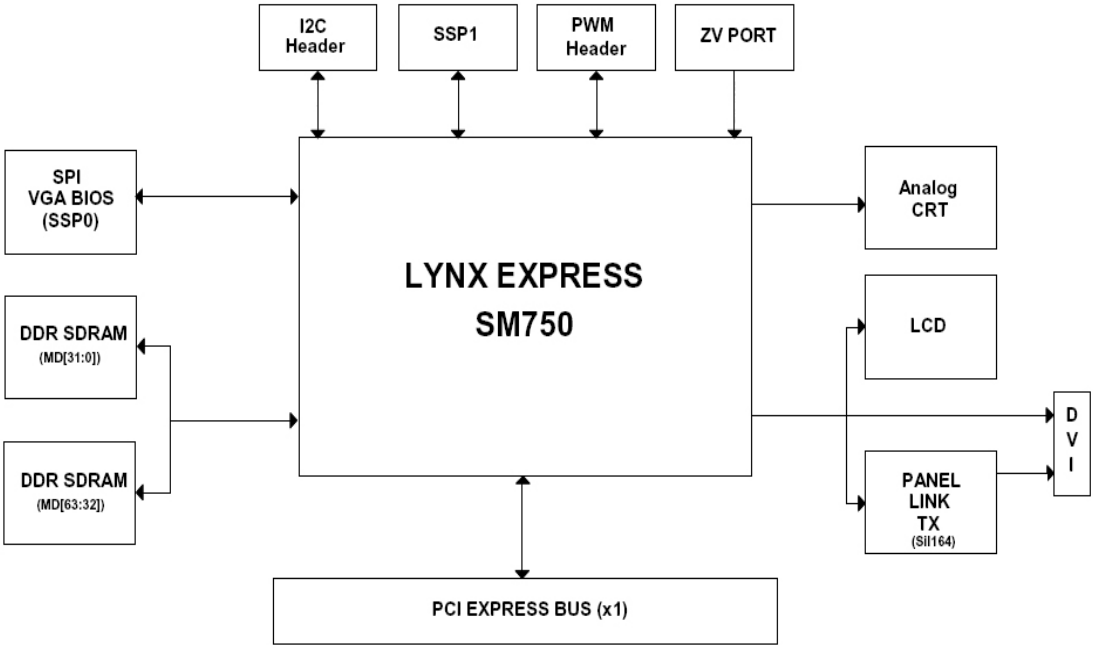


Figure 1: System Block Diagram

Features	Benefits
High Performance and Power Managed 2D	Desktop level 2D performance within the power budget of a low power consumption system
Multiple Display Support Under Major OSs	• Applications available at the same time across multiple display devices (CRT1+CRT2, LCD1+LCD2, CRT+LCD) • Single chip implementation ideal for various system form factors
Dual Digital LCD Support	• Independent display support for digital LCD displays • Dual 18-bit digital LCD outputs
Adaptive Power Management • With dynamic functional block power down and clock control	Reduces average power consumption when in operation mode
Multiple Independent Hardware Video Windows	Independent full screen, motion video for separate displays
128-bit Single Clock Cycle Drawing Engine	No compromise 2D graphics performance for various system form factors
High Performance DDR Memory Interface	Delivers up to 1.3GB/s bandwidth with 32-bit memory interface and 2.6GB/s bandwidth with 64-bit memory interface to support multiple display functions and display outputs
PCI Express 1.1 x1 Lane Support	Provides interface capability for today's most popular PC graphic busses
Digital LCD Panel Support up to 1920x1440	Supports all panel requirements for various system form factors
Dual 300 MHz 24-bit RAMDACs	• Supports resolutions up to 1920x1440 for CRT display • Supports dual CRT outputs
7 Video Display Layers	Provides 7 layers of display frame includes graphics, videos, alphas, and cursors
General Purpose I/O	Provides programmable I/O for customize application
Dual Zoom Video Port	Provides support for camera, TV tuner input, or video output from various video decoders
Hardware Support LCD Landscape or Portrait Rotation	Portrait view for desktop publishing, word processing applications
ACPI Compliant	Meets WHQL certification requirements
Software Support for Microsoft Windows XP, 2003, 2008, Vista, Windows 7, Windows CE, and various Linux	Complete OS software support

1.2 Pins

1.2.1 Pin Descriptions

The following table provides brief description of each BGA ball of the SM750. Signal names with # following are active “LOW” signals, whereas signal names without # following are active “HIGH” signals. Also the following abbreviations are used for Pin Type.

I-Input Signal

O-Output Signal

I/O-Input or Output Signal

Internal pull-downs for TEST[2:0] and GPIO[31:0] pads are all 85K-ohm resistors.

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
Host Interface (8)					
TX+, TX-	A8, B8	DO	Differential Out	—	SM750 PCIe differential transmit pair
RX+, RX-	A10, B10	DI	Differential In	—	SM750 PCIe differential receive pair
REFCLK+, REFCLK-	A12, B12	DI	Differential In	—	PCIe reference clock differential pair
REXT	D11	I	CMOS 3.3V	TBD	Required to connect to a 191ohm pull-down resistor
RST#	C13	I	CMOS 3.3V	TBD	PCIe fundamental reset
Clock Interface (11)					
PLL_AGND	B14, B17	I	0V	—	PLL analog ground
PLL_DGND	B15, B16	I	0V	—	PLL digital ground
PLLPWR_A	A14	I	3.3V	—	PLLA analog power
PLLPWR_DA	A15	I	3.3V	—	PLLA digital power
PLLPWR_BC	A19	I	3.3V	—	PLLB and PLLC analog power
PLLPWR_DBC	A18	I	3.3V	—	PLLB and PLLC digital power
TESTCLK	C14	I	CMOS 3.3V	TBD	For testing purposes
XTALIN	A17	I	CMOS 3.3V	TBD	14.31818 MHz crystal input connection
XTALOUT	A16	O	CMOS 3.3V	TBD	14.31818 MHz crystal output connection
Test Interface (3)					
TEST[2:0]	M17, L17, L18	I	CMOS 3.3V	TBD	Test mode selection TEST[2:0] have weak internal pull-down resistors.

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
Memory Interface (104)					
BA[1:0]	J3, J4	O	CMOS 2.5V	TBD	DDR bank address
CAS#	J1	O	CMOS 2.5V	TBD	DDR column address strobe
CKE	K2	O	CMOS 2.5V	TBD	DDR clock enable
CS#	K3	O	CMOS 2.5V	TBD	DDR chip select
DQM[7:0]#	V3, R1, G2, E2, V8, C4, V6, C6	O	CMOS 2.5V	TBD	DDR data mask
DQS[7:0]#	W3, T1, G1, E1, W8, C3, W6, D6	O	CMOS 2.5V	TBD	DDR data strobe
MA[12:0]	P2, P3, P4, N1, N2, N3, N4, M1, M2, M3, M4, L3, L4	O	CMOS 2.5V	TBD	DDR address bus
MD[31:0]	W10, V10, W9, V9, U9, T9, U8, T8, B1, A1, B2, A2, B3, A3, B4, A4, W7, V7, U7, U6, T6, V5, U5, T5, D5, C5, B5, A5, B6, A6, D7, C7	I/O	CMOS 2.5V	TBD	DDR data bus [31:0]
MD[63:32]	W5, W4, V4, U4, W1, W2, V1, V2, U1, U2, U3, T2, T3, T4, R2, R3, H2, H3, H4, G3, G4, F1, F2, F3, E4, E3, D4, D3, D1, D2, C1, C2	I/O	CMOS 2.5V	TBD	DDR data bus [63:32]
MVREF[1:0]	P1, H1	I	1.25V	—	DDR voltage reference
RAS#	J2	O	CMOS 2.5V	TBD	DDR row address strobe
SCK+, SCK-	K1, L1	O	CMOS 2.5V	TBD	DDR differential clock
WE#	L2	O	CMOS 2.5V	TBD	DDR write enable

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
Flat Panel Interface (31)					
BIAS	T18	O	CMOS 3.3V	TBD	Flat panel voltage bias enable
FP[23:0]	U17, T16, U16, V16, T15, U15, V15, W15, U14, V14, W14, T13, U13, V13, W13, T12, U12, V12, W12, U11, V11, W11, T10, U10	O	CMOS 3.3V	TBD	Flat panel data bus [23:0]
FP_DISP	R17	O	CMOS 3.3V	TBD	Flat panel display enable
FP_HSYNC	M18	O	CMOS 3.3V	TBD	Flat panel horizontal sync
FP_VSYNC	N18	O	CMOS 3.3V	TBD	Flat panel vertical sync
FPCLK	W16	O	CMOS 3.3V	TBD	Flat panel pixel clock
FPEN	T17	O	CMOS 3.3V	TBD	Flat panel enable
VDEN	U18	O	CMOS 3.3V	TBD	Flat panel VDD enable
CRT0 Interface (6)					
B0	W19	O	Analog	—	CRT0 blue output
CRT_HSYNC	V17	O	CMOS 3.3V	TBD	CRT0 horizontal sync
CRT_VSYNC	W17	O	CMOS 3.3V	TBD	CRT0 vertical sync
G0	V19	O	Analog	—	CRT0 green output
IREF0	R19	I	Analog	—	CRT0 IREF output
R0	U19	O	Analog	—	CRT0 red output
CRT1 Interface (4)					
B1	N19	O	Analog	—	CRT1 blue output
G1	M19	O	Analog	—	CRT1 green output
IREF1	J19	I	Analog	—	CRT1 IREF output
R1	L19	O	Analog	—	CRT1 red output
Video Port Interface (3)					
VP_CLK	H19	I	CMOS 3.3V	TBD	Video port clock
VP_HREF	F19	I	CMOS 3.3V	TBD	Video port horizontal reference
VP_VSYNC	G19	I	CMOS 3.3V	TBD	Video port vertical sync

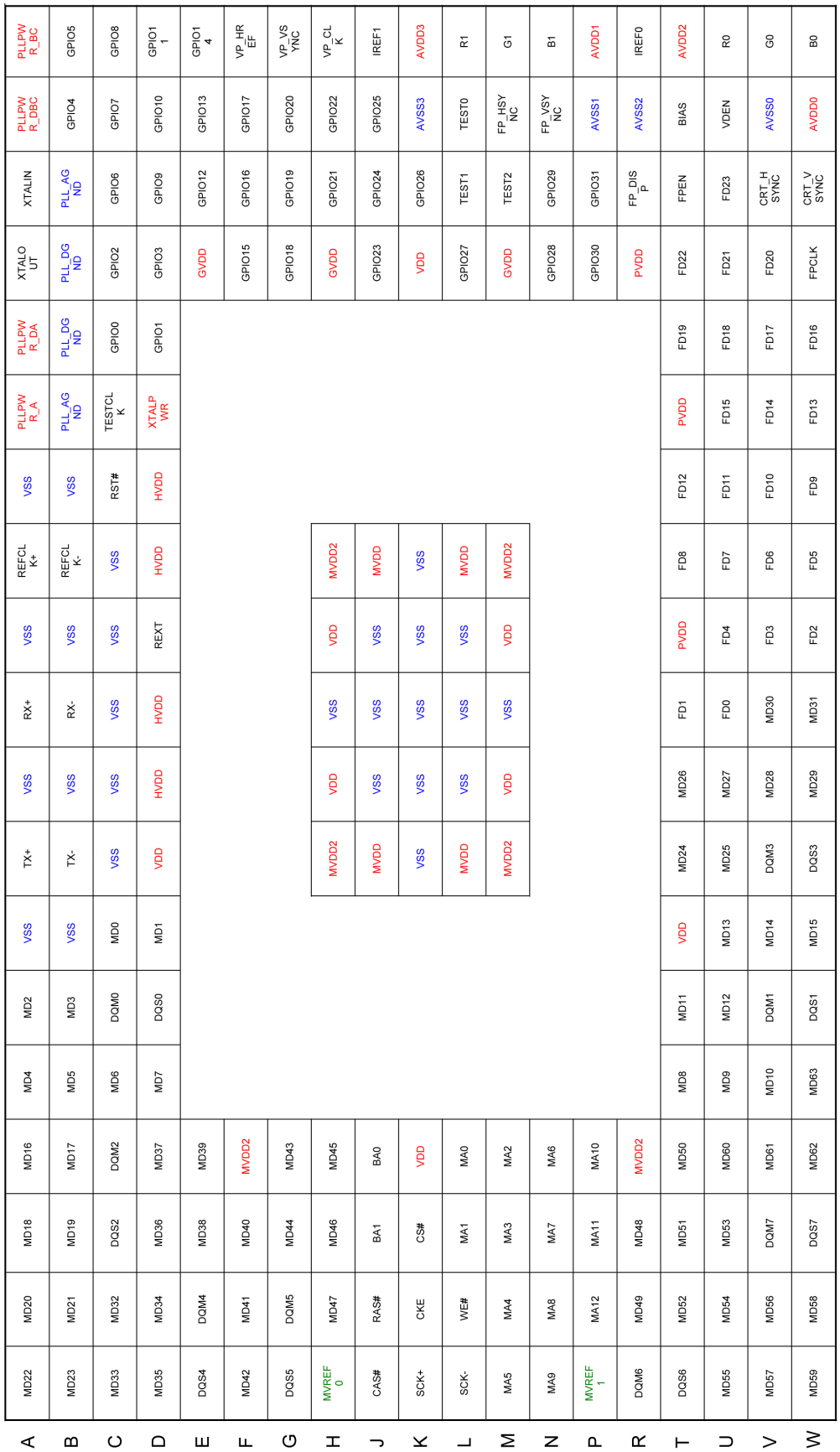
Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
GPIO Interface (32) – All 32 GPIO pins have weak internal pull-down resistors.					
GPIO[7:0]	C18, C17, B19, B18, D16, C16, D15, C15	I/O	CMOS 3.3V	TBD	GPIO[7:0] / Video Port D[7:0]
GPIO[15:8]	F16, E19, E18, E17, D19, D18, D17, C19	I/O	CMOS 3.3V	TBD	GPIO[15:8] / Video Port D[15:8] / FD[31:24]
GPIO16	F17	I/O	CMOS 3.3V	TBD	GPIO16 / CLKIN / FDSCLK1
GPIO[19:17]	G17, G16, F18	I/O	CMOS 3.3V	TBD	GPIO[19:17] / PWM[2:0]
GPIO20	G18	I/O	CMOS 3.3V	TBD	GPIO20 / SSP0 TXD
GPIO21	H17	I/O	CMOS 3.3V	TBD	GPIO21 / SSP0 RXD
GPIO22	H18	I/O	CMOS 3.3V	TBD	GPIO22 / SSP0 SFOUT
GPIO23	J16	I/O	CMOS 3.3V	TBD	GPIO23 / SSP0 SFIN
GPIO24	J17	I/O	CMOS 3.3V	TBD	GPIO24 / SSP0 CLK
GPIO25	J18	I/O	CMOS 3.3V	TBD	GPIO25 / SSP1 TXD / FD32
GPIO26	K17	I/O	CMOS 3.3V	TBD	GPIO26 / SSP1 RXD / FD33
GPIO27	L16	I/O	CMOS 3.3V	TBD	GPIO27 / SSP1 SFOUT / FD34
GPIO28	N16	I/O	CMOS 3.3V	TBD	GPIO28 / SSP1 SFIN / FD35
GPIO29	N17	I/O	CMOS 3.3V	TBD	GPIO29 / SSP1 CLK
GPIO30	P16	I/O	CMOS 3.3V	TBD	GPIO30 / I^2C SCL
GPIO31	P17	I/O	CMOS 3.3V	TBD	GPIO31 / I^2C SDA
Power and Ground (63)					
AVDD0	W18	I	1.2V	—	DAC0 Analog Power, 1.2V
AVDD1	P19	I	1.2V	—	DAC1 Analog Power, 1.2V
AVDD2	T19	I	3.3V	—	DAC0 Analog Power, 3.3V
AVDD3	K19	I	3.3V	—	DAC1 Analog Power, 3.3V
AVSS0	V18	I	0V	—	DAC0 Analog Ground for AVDD0
AVSS1	P18	I	0V	—	DAC1 Analog Ground for AVDD1
AVSS2	R18	I	0V	—	DAC0 Analog Ground for AVDD2
AVSS3	K18	I	0V	—	DAC1 Analog Ground for AVDD3

Signal Name	Pin Number	Type	Pad	IOL (ma)	Description
VSS	A7, A9, A11, A13, B7, B9, B11, B13, C8, C9, C10, C11, C12, H10, J9, J10, J11, K8, K9, K10, K11, K12, L9, L10, L11, M10	I	0V	—	Core Ground
GVDD	E16, H16, M16	I	3.3V	—	GPIO Power
HVDD	D9, D10, D12, D13	I	3.3V	—	Host Power
MVDD	J8, J12, L8, L12	I	2.5V	—	DDR Core Power
MVDD2	F4, H8, H12, M8, M12, R4	I	2.5V	—	DDR I/O Power
PVDD	R16, T11, T14	I	3.3V	—	LCD Panel I/O Power
VDD	D8, H9, H11, K4, K16, M9, M11, T7	I	1.2V	—	Core Power
XTALPWR	D14	I	3.3V	—	Crystal Power

Table 1: Pin Description

1.2.2 *Package Information*

SM750 Pin Diagram for 265 BGA Package



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	MD22	MD20	MD18	MD16	MD4	MD2	VSS	TX+	VSS	RX+	VSS	REFCLK+	VSS	PLLPWR_A	PLLPWR_DA	XTALOUT	XTALIN	PLLPWR_DBC	PLLPWR_BC
B	MD23	MD21	MD19	MD17	MD5	MD3	VSS	TX-	VSS	RX-	VSS	REFCLK-	VSS	PLL_AGND	PLL_DGND	PLL_DGND	PLL_AGND	GPIO4	GPIO5
C	MD33	MD32	DQS2	DQM2	MD6	DQM0	MD0	VSS	VSS	VSS	VSS	VSS	RST#	TESTCLK	GPIO0	GPIO2	GPIO6	GPIO7	GPIO8
D	MD35	MD34	MD36	MD37	MD7	DQS0	MD1	VDD	HVDD	HVDD	REXT	HVDD	HVDD	XTALPWR	GPIO1	GPIO3	GPIO9	GPIO10	GPIO11
E	DQS4	DQM4	MD38	MD39												GVDD	GPIO12	GPIO13	GPIO14
F	MD42	MD41	MD40	MVDD2												GPIO15	GPIO16	GPIO17	VP_HREF
G	DQS5	DQM5	MD44	MD43												GPIO18	GPIO19	GPIO20	VP_VSYNC
H	MVREF0	MD47	MD46	MD45				MVDD2	VDD	VSS	VDD	MVDD2				GVDD	GPIO21	GPIO22	VP_CLK
J	CAS#	RAS#	BA1	BA0				MVDD	VSS	VSS	VSS	MVDD				GPIO23	GPIO24	GPIO25	IREF1
K	SCK+	CKE	CS#	VDD				VSS	VSS	VSS	VSS	VSS				VDD	GPIO26	AVSS3	AVDD3
L	SCK-	WE#	MA1	MA0				MVDD	VSS	VSS	VSS	MVDD				GPIO27	TEST1	TEST0	R1
M	MA5	MA4	MA3	MA2				MVDD2	VDD	VSS	VDD	MVDD2				GVDD	TEST2	FP_HSYNC	G1
N	MA9	MA8	MA7	MA6												GPIO28	GPIO29	FP_VSYNC	B1
P	MVREF1	MA12	MA11	MA10												GPIO30	GPIO31	AVSS1	AVDD1
R	DQM6	MD49	MD48	MVDD2												PVDD	FP_DISP	AVSS2	IREF0
T	DQS6	MD52	MD51	MD50	MD8	MD11	VDD	MD24	MD26	FD1	PVDD	FD8	FD12	PVDD	FD19	FD22	FPEN	BIAS	AVDD2
U	MD55	MD54	MD53	MD60	MD9	MD12	MD13	MD25	MD27	FD0	FD4	FD7	FD11	FD15	FD18	FD21	FD23	VDEN	R0
V	MD57	MD56	DQM7	MD61	MD10	DQM1	MD14	DQM3	MD28	MD30	FD3	FD6	FD10	FD14	FD17	FD20	CRT_HSYNC	AVSS0	G0
W	MD59	MD58	DQS7	MD62	MD63	DQS1	MD15	DQS3	MD29	MD31	FD2	FD5	FD9	FD13	FD16	FPCLK	CRT_VSYNC	AVDD0	B0

1.3 Internal Block Description

1.3.1 PCI Express Interface

SM750 provides a glue-less interface to the PCI Express system bus. The device is fully compliant with PCI Express 1.1. SM750 PCI Express Interface Unit supports PCI Express x1 lane operation. To maximize performance, the Interface Unit also supports burst write and burst read. The Interface Unit decodes I/O read, I/O write, memory read, memory write, memory mapped access, 2D Drawing Engine access, VAG access, and others.

SM750 has an internal HIF (Host Interface) bus, which is designed to transfer data between the PCI Express Interface Unit and other functional blocks. The PCI Express Interface Unit controls the HIF bus protocol to effectively deliver I/O and memory cycles to each function block.

Communication between the system bus and SM750 is a dual-simplex communication channel that consists two, low-voltage, differentially driven signals pairs: a Transmit pair and a Receive pair as show in the figure below.

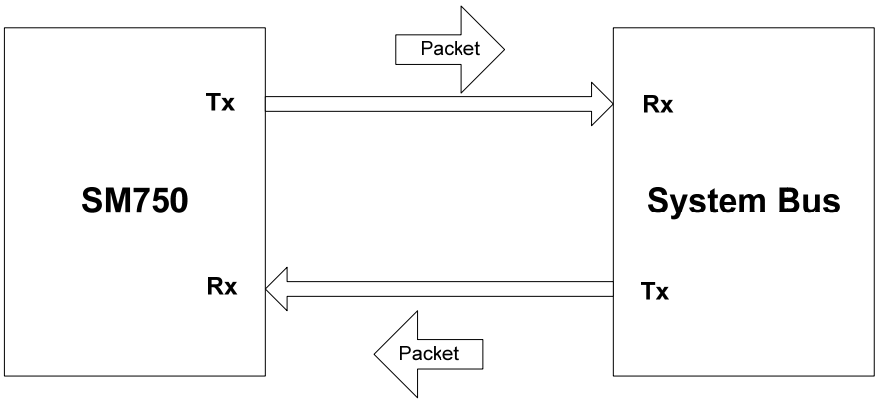


Figure 2: PCI Express Interface

Interfacing to PCI Express Device

This section provides information for interfacing the SM750 to PCI Express 1.1 complaint devices. It covers these topics:

- Hardware Connections
- Expansion Connector
- Configuration Header
- Power Supply Considerations
- Board Layout Considerations

Hardware Connections

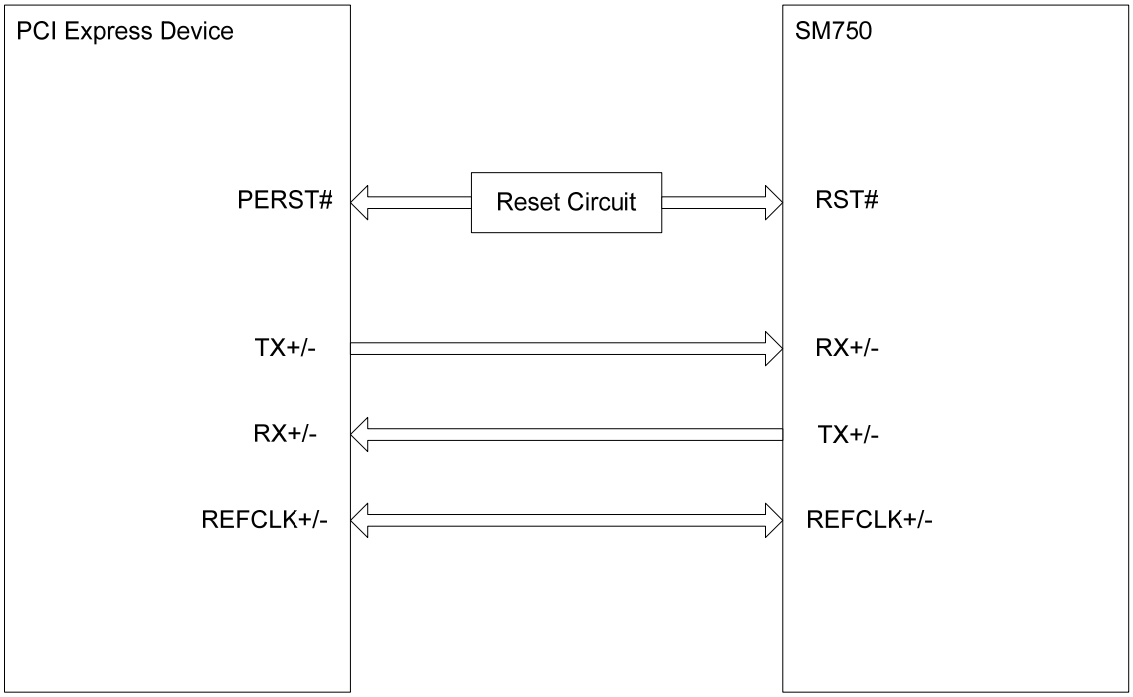


Figure 3: SM750 Connections to PCI Express Device

Expansion Connector

Table 2 shows the connections from the SM750 to the PCI Express Expansion Connector. The 3.3V supply is the preferred design.

Pin	Side A	Side B
1	PRSNT1#	+12V
2	+12V	+12V
3	+12V	+12V
4	GND	GND
5	JTAG2	SMCLK
6	JTAG3	SMDAT
7	JTAG4	GND
8	JTAG5	+3.3V

Pin	Side A	Side B
9	+3.3v	JTAG1
10	+3.3V	3.3V AUX
11	RST#	WAKE#
12	GND	RESERVED
13	REFCLK+	GND
14	REFCLK-	TX+
15	GND	TX-
16	RX+	GND
17	RX-	PRSNT2#
18	GND	GND

Table 2: SM750 PCI Express Connector Mapping

Configuration Header

Table 3 shows the Configuration Space Header.

Address (hex)	Field Definitions			
	31:24	**23:16**	**15:8**	**7:0**
00	Device ID		Vendor ID	
04	Status		Command	
08	Class Code			Revision ID
0C	BIST	Header Type	Master Latency Timer	Cache Line Size
10	Base Address Registers			
14				
18				
1C				
20				
24				
28	Cardbus CIS Pointer			
2C	Subsystem ID		Subsystem Vendor ID	
30	Expansion ROM Base Address			
34	Reserved			Capabilities Pointer
38	Reserved			
3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

Table 3: Type 00 PCI Configuration Header Values

Power Supply Considerations

Figure 5 shows the power supply connections to the SM750 in a PCI Express design.

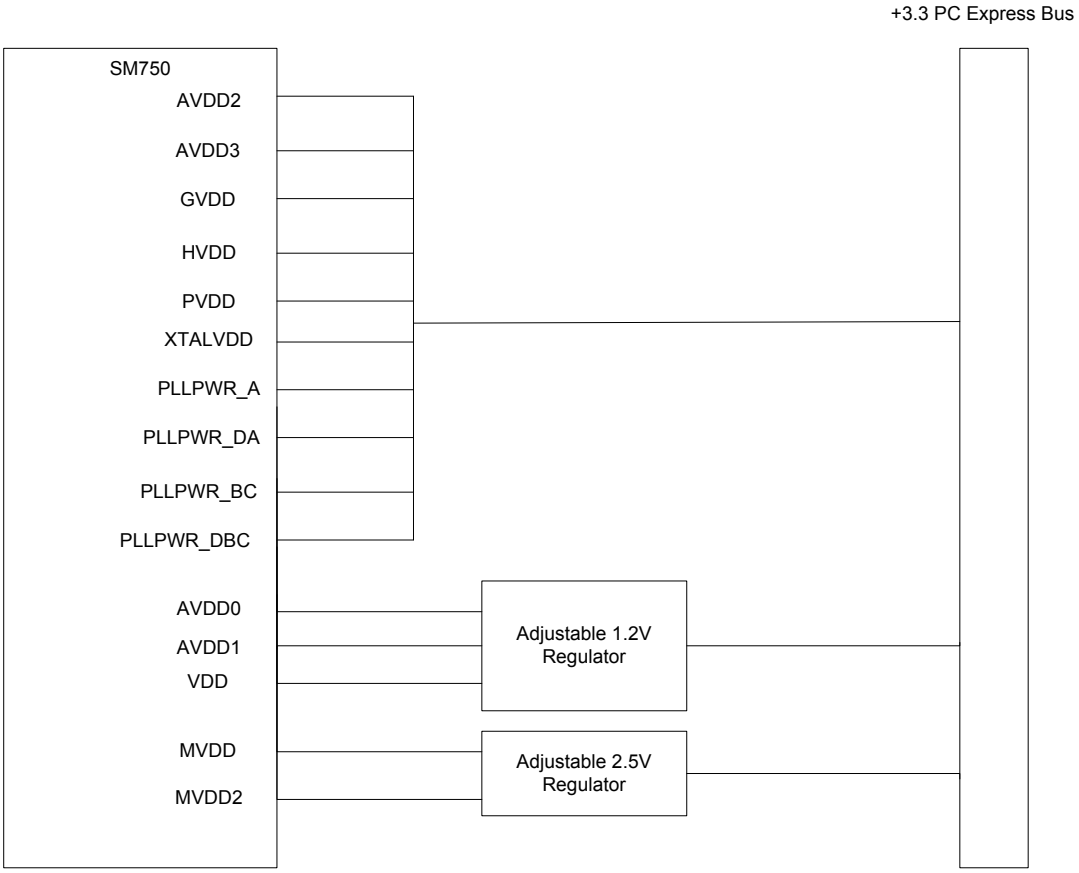


Figure 4: Power Supply Connections for SM750 in PCI Express Design

Board Layout Considerations

PC Board requirements are as follows:

- The unloaded characteristic impedance of shared PCI Express signal traces must be controlled to be in the range of 60 to 100 ohms.
- Trace velocity should be between 150 and 190 ps/inch.
- Six layers are required. The rest area must be covered with ground on both sides, top and bottom.

PCI Express Bus Interface requirements are as follows:

- Set VCC and GND plane. A split power planes is permitted; for this board, 3.3V is the main plane.
- Signal traces must remain entirely over either the 3.3V plane.
- Signals that cross from one domain to the other should be routed on the opposite side of the board.
- If some signal traces are routed on layer 3 or 4, they cannot be overlaid.
- The maximum trace length for all 32-bit interfaces is 1.5 inches.
- Traces must be at least 7 mils wide.
- The length of the PCI Express clock trace should be 2.5 inches +/- 0.1 inches.

1.3.2 *Display Memory Interface*

The SM750 supports embedded DDR memory or external DDR memory setup. It includes a local memory interface to drive an external local memory of 8 to 64 Mbytes in size. This chapter provides basic information for designing an embedded local memory or an external local memory setup. For detailed timing information, consult the documentation provided by the memory device manufacture.

This chapter contains the following sections:

- Memory Architectures
- Local Memory Interface Signals
- Configuring the Local Memory Interface

Memory Architectures

SM750 supports 16Mbytes of embedded DDR memory that clocked up to 145 MHz. The device's embedded memory supports a 32-bit DDR memory interface, so it provides up to 1.3GB/s of memory bandwidth.

SM750 also supports an independent 64-bit external DDR memory interface that supports up to 64Mbytes of external DDR memory. Therefore, with a 64-bit external DDR memory setup, it provides up to 2.6GB/s of memory bandwidth.

Figure 6 shows the three possible memory setups. (A) 32-bit embedded DDR memory, (B) 32-bit external DDR memory, and (C) 64-bit external DDR memory setups.

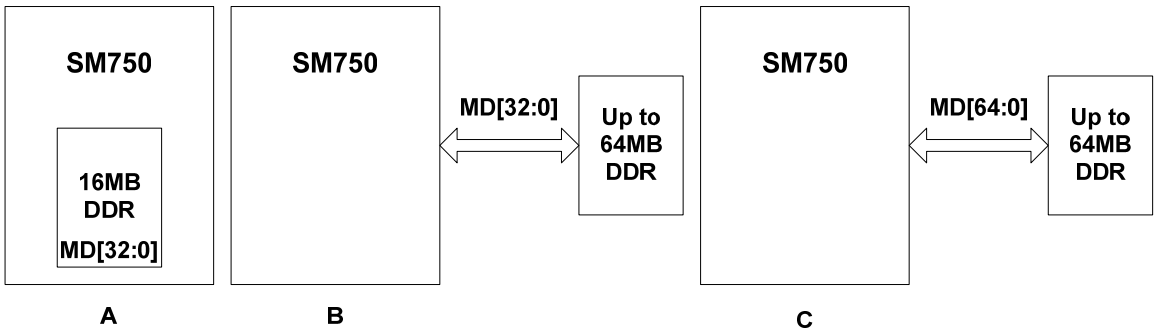


Figure 5: Memory Setups

Local Memory Interface Signals

Figure 7 shows the connection diagram for a typical DDR memory setup organized as two pieces of 16M x 16 DDR SDRAMs.

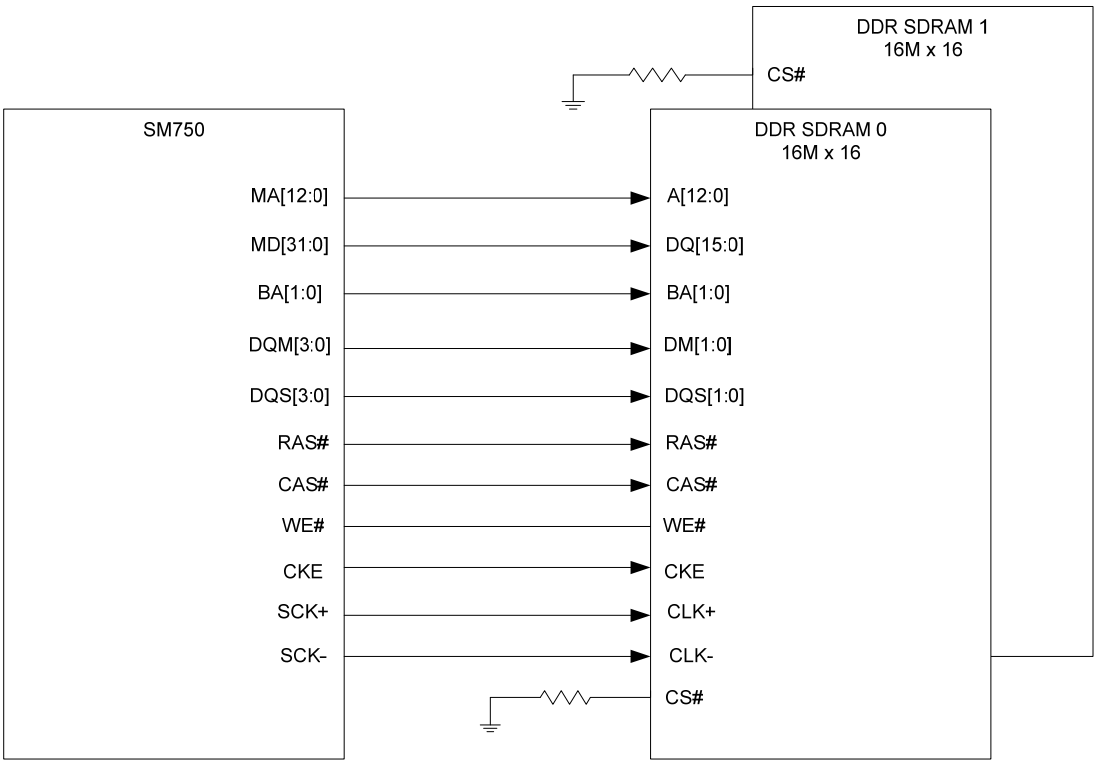


Figure 6: Typical DDR Memory Setup

Configuring the Local Memory Interface

The configuration of the local memory interface can be set through power-on strap pins or using Miscellaneous Control Register MMIO_base + 0x000004. This section discusses the bits and strap-pins that control parameters for the local memory interface.

Memory Size

The SM750 must be configured with the size of local memory. Bits [13:12] of the Miscellaneous Control Register set the size of the local memory as shown in Table 3. The size of the local memory can also be determined by the power-on configuration values of Memory Address pins MA[6:5] as shown in Table 3; however, writing a value to the Miscellaneous Control Register will override the power-on configuration setting.

Miscellaneous Control Register Bit or Memory Address Pin at Power-On		Memory Size in Mbytes
Bit 13 or MA6	Bit 12 or MA5	
0	0	16MB
0	1	32MB
1	0	64MB
1	1	8MB

Table 4: Configuring the Size of Local Memory

Memory Device Architecture

The SM750 must be configured for the physical architecture of the memory devices used in the local memory, including the column size and memory bus width.

Bit [15:14] of the Miscellaneous Control Register set the column size of the local memory as shown in Table 4. The column size can also be determined by power-on configuration values of Memory Address pins MA[8:7] as shown in Table 4; however, writing a value to the Miscellaneous Control Register will override the power-on configuration setting.

Bit 1 of the Miscellaneous Control Register set the width of the memory interface data bus as shown in Table 5. The memory interface data bus width can also be determined by power-on configuration values of Memory Address pins MA1 as shown in Table 5; however, writing a value to the Miscellaneous Control Register will override the power-on configuration setting.

Miscellaneous Control Register Bit or Memory Address Pin at Power-On		Column Size
Bit 15 or MA8	Bit 14 or MA7	
0	0	256 words
0	1	512 words
1	X	1024 words

Table 5: Configuring the Column Size of Local Memory

Miscellaneous Control Register Bit or Memory Address Pin at Power-On	Memory Bus Width
Bit 1 or MA1	
0	32-bit
1	64-bit

Table 6: Configuring the Memory Bus Width

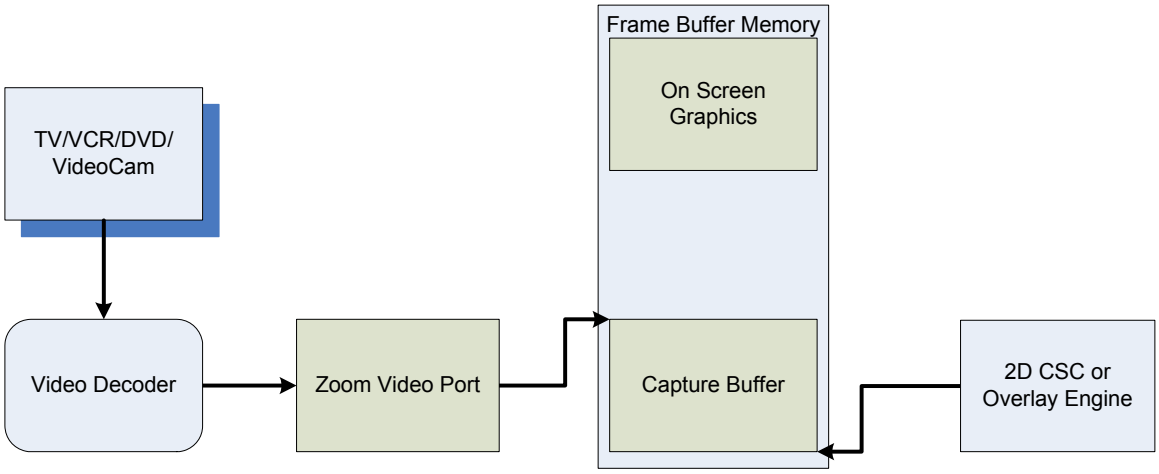
1.3.3 Zoom Video Port

The SM750 includes two Zoom Video (ZV) ports to allow the use of external MPEG decoders for DVD playback, external TV tuners, and other sources. This interface supports the YUV 4:2:2, YUV 4:2:2 with byte swap and RGB 5:6:5 data formats. It also supports ITU656-8 bit.

The standard ZV port uses an 8-bit interface at 65 MHz. However, if desired, an extra 8 bits in the GPIO interface may be used to interface to ICs that only support a 16-bit ZV interface or uses the extra 8 bits for the second ZV port input. The pins used for the ZV interface are designated GPIO pins.

Note that the ZV input to video display path is as follows: ZV port → capture → frame buffer → video scalar → display. The capture portion supports a 1:1 or 2:1 reducing. In addition, the video scalar allows arbitrary scaling from 1:1 to 4:1 on shrinking and 1:1 to 1:212 on expansion; however, the quality of the expansion is degraded beyond 1:8. This will easily allow 4:3 and 16:9 conversion, full screen PAL, and picture-in-picture.

See Chapter 9 for more information about the ZV Port registers.



1.3.4 2D Engine

The SM750 provides industry-leading 2D acceleration through the combination of an optimized 128-bit 2D drawing engine and a high bandwidth link to local frame memory. The 2D engine also contains a command interpreter (an enhanced DMA engine) that can intelligently fetch operands out of the frame buffer at up to 600MB/s. The command interpreter can conditionally branch to another location in memory, wait for status from another module, etc. as it fetches and interprets commands.

The 2D drawing engine also contains a color space conversion unit. The color space conversion unit allows for direct translation from many YUV formats into RGB. The 2D drawing engine also contains a bi-linear scalar, which supports 4:1 shrink and 1:216 stretch.

As noted previously, the SM750 supports embedded memory in 32-bit modes. With 32 bits of DDR running at 145 MHz, the SM750's DMA engine has 1.2GB/s of memory bandwidth to use for fetching 2D operands and data. This high memory bandwidth allows the 2D engine to run at full speed without costly waits or pipeline stalls from the frame buffer.

The 2D drawing engine understands the following commands:

1. BitBlt (from system/local memory to system/local memory) with 256 raster operations. Pattern is selectable between 8x8 monochrome pattern, 8x8 color pattern or another surface located in either system or local memory.
2. Transparent BitBlt with the same capabilities as the previous command, but only the source or destination can be transparent (either ColorKey or ChromaKey).
3. Alpha BitBlt with a constant alpha value.

4.Rotation BitBlt for any block size. This feature allows high speeds conversion between landscape and portrait display without the need for special software drivers. (90°, 180°, 270°.)

5.YUV to 16-bit/32-bit RGB Blt conversion with 1:216 stretch or 4:1 shrink to provide high speeds video in common format.

6.Auto-wrapping for smooth scrolling support for navigational or other data.

7.Support for tiled memory to optimize performance for 2D operations and rotation.

As noted previously, the 2D Drawing Engine has a 112 MHz clock and a 128-bit wide memory access path.
With 8-bpp colors, the 2D engine can process 2400M pixels/s, and with 16-bpp the 2D engine can process 1200M pixels/s.

See Chapter 5 for more information about the 2D Drawing Engine.

1.3.5 Video Display Layers

As shown in Figure 8, the SM750 supports seven layers of display frames (2x hardware cursor, primary graphics, video, video alpha, alpha, and secondary graphics). (See Chapter 6 for more information about the Display Controller.)

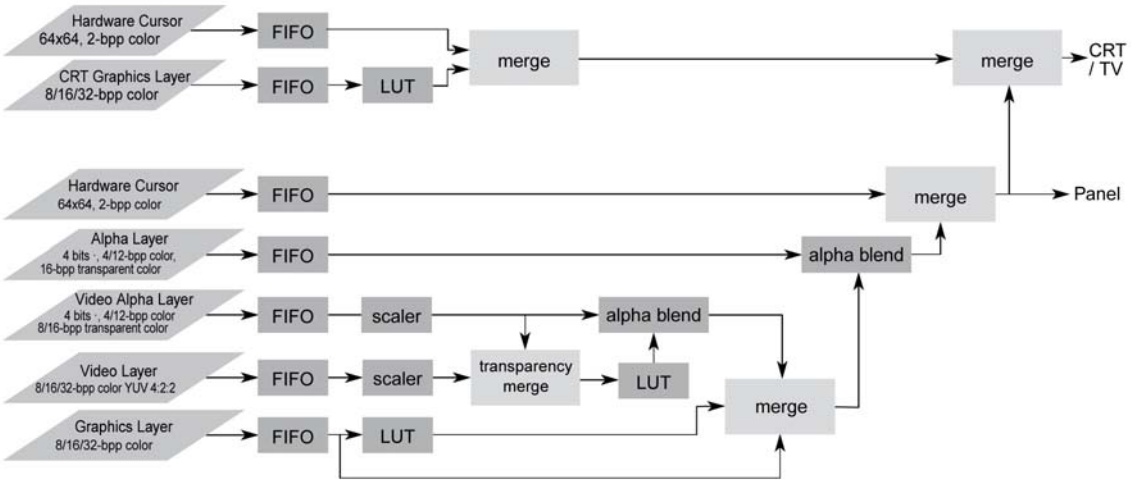


Figure 7: Video Layers and Data Processing

Layer #7: Secondary Hardware Cursor

To display a cursor on the analog output for multi-monitor function.

- One single 64x64 pixel cursor 2-bpp color [1:0] (00 = transparent, 01 = color0, 10 = color1, 11 = color2), is mapped into a 32-bit RGB 8:8:8 color map.

Layer #6: Secondary Graphics

To display text or drawings on the analog output (CRT) for multi-monitor function.

- 8-bpp (index into RGB 8:8:8 lookup table).
- 16-bpp RGB 5:6:5.
- 32-bpp RGB 8:8:8.

Layer #5: Primary Hardware Cursor

To display a cursor on the digital output.

- One single 64x64 pixel cursor 2-bpp color [1:0] (00 = transparent, 01 = color0, 10 = color1, 11 = color2), is mapped into a 32-bit RGB 8:8:8 color map.

Layer #4: Alpha

To alpha-blend and/or color-key an image on top of the Primary Graphics and Video layer outputs.

- 16-bpp (4-bit alpha, 4-bit Red, 4-bit Green, 4-bit Blue) or RGB 5:6:5.
- 16-bit transparency register (with 16-bit RGB 5:6:5 mode); if a color matches the register's value it is transparent.
- 8-bit index (αI 4:4 mode)

Layer #3: Video Alpha

To alpha-blend and/or color-key an image on top of the Video layer output.

- Supports bi-linear scale up or down.
- 8-bpp (4-bit alpha, 4-bit index color), or 8-bit index (index into RGB 8:8:8 lookup table).
- 16-bpp (4-bit alpha, 4-bit Red, 4-bit Green, 4-bit Blue) or RGB 5:6:5.
- 8-bit transparency register (with 8-bit index), or 16-bit transparency register (with 16-bit RGB 5:6:5 mode); if a color matches the register's value it is transparent.
- 4-bit planar blending register (in 16-bit RGB 5:6:5 mode only) to blend all pixels on the plane (that are non-transparent) to one planar alpha value.

Layer #2: Video

To overlay video image or graphics on top of Primary Graphics layer.

- Supports bi-linear scale up or down.
- 16-bpp RGB 5:6:5 or YUV 4:2:2.

Layer #1: Primary Graphics

To display text or drawings on the primary output (LCD panel).

- Support smooth scrolling and auto-wrapping.
- 8-bit index (index into RGB 8:8:8 lookup table).
- 16-bpp RGB 5:6:5.
- 32-bpp RGB 8:8:8.
- 8-bit (with 8-bit index), 16-bit (with 16-bit RGB 5:6:5), or 32-bit (with 32-bit RGB 8:8:8) color key register. If the color value matches the register's value, the color is transparent and the pixel from the Primary Video layer is shown instead.

Terminology

Some definitions of terms used above:

bpp – bits per pixel.

RGB – Red, Green, Blue.

RGB 5:6:5 – 16-bit color mode, where Red has 5 bits, Green has 6 bits, and Blue has 5 bits.

RGB 8:8:8 – 32-bit color mode, where Red has 8 bits, Green has 8 bits, and Blue has 8 bits. The upper 8 bits are unused.

Alpha – A means of blending two layers together. The fundamental equation is (α * c) + (1 - α) * (original pixel), where c is the 4-bit color that points into the 18-bit lookup table. In practical terms, 4-bit alpha blending means that for two given display layers, one layer is dominant (e.g. video layer) and the other layer (e.g. video alpha) has 16 levels of transparency from 100% to 0% that may be applied to the colors in that layer.

LUT – Lookup table; a means to map an 8-bit color index into a 24-bit color space, thus a smaller number of simultaneous colors (8-bit) but with a wide range of colors (24-bit) to choose from.

Display Resolution

The SM750 supports display resolutions up to 1920 x 1440. 16:9 formats in this range (e.g. 800 x 480, 1024 x 600, 1280 x 768, and etc.) are supported. Note that there are trade-offs between the maximum resolution, the number of active video layers, and the frame memory choice.

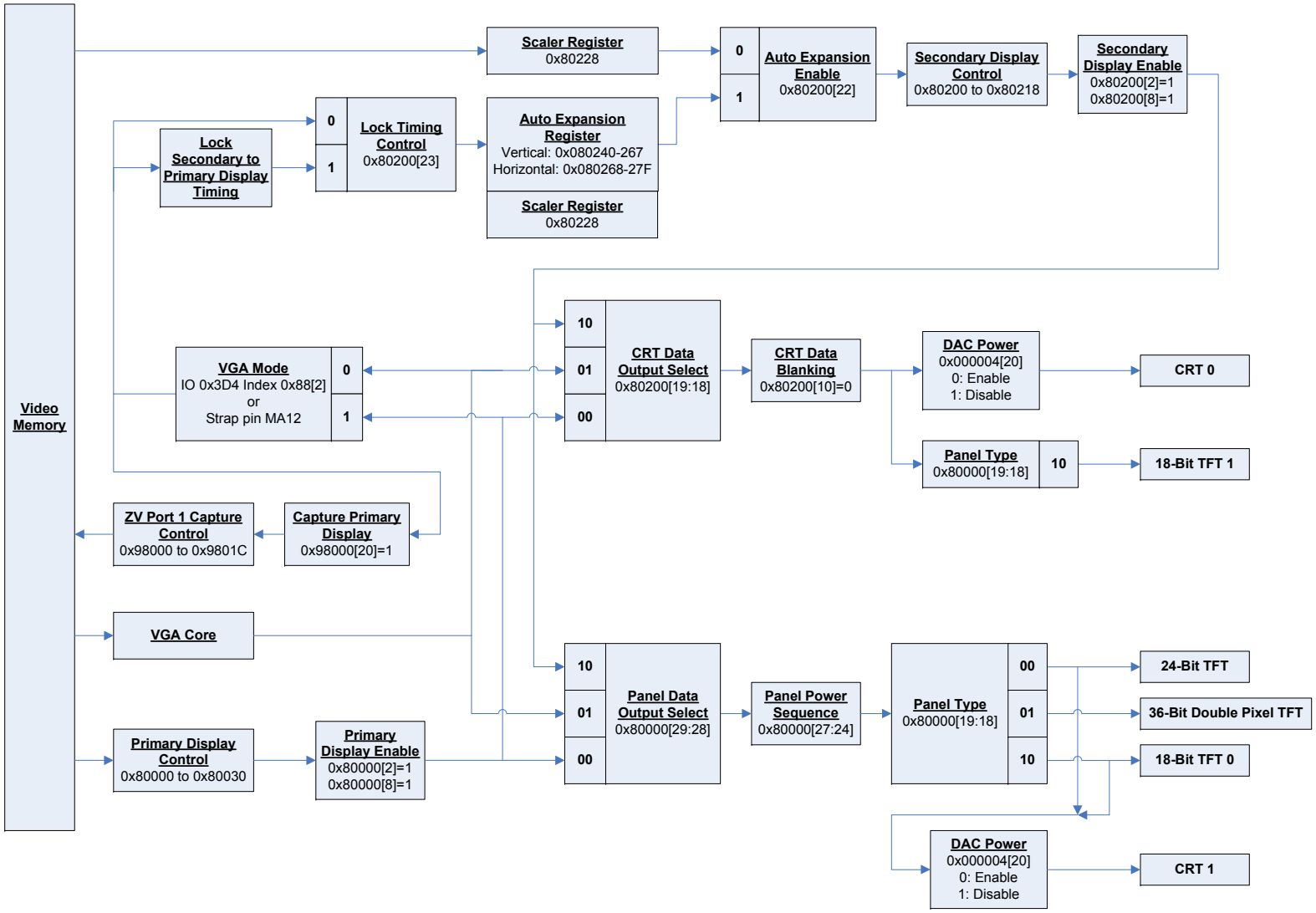
Dual Display

The SM750 supports Dual Display, i.e. two different displays of the same or different resolutions.

Only the panel pipe supports the video and alpha planes. However, since these planes fetch data from the frame buffer memory as well, there might not be enough bandwidth to enable the video and alpha planes in Dual Display mode.

In order to display video on the panel pipe in Dual Display mode and on the CRT pipe in any mode, the 2D Engine's Color Space Conversion and Stretching functionality should be used.

The SM750 supports Dual Display in several combinations: CRT, LCD, LCD+CRT, or LCD1+LCD2; the figure below shows the relationship between each display in respect to the frame buffer.



1.3.6 LCD Panel

The SM750 integrates a concurrent video processor to control LCD displays. The SM750 LCD interface can be configured to drive one of the following:

- An 18-bit or 24-bit active matrix (TFT) panel
- An 36-bit (18-bit x 2) active matrix (TFT) panel
- Two independent 18-bit active matrix (TFT) panels

The maximum supported panel size is 1920x1440. Figure 9 shows a typical interface between the SM750 and a 24-bit TFT panel. Note the following with regards to this interface:

1. The timings of VDEN, FPEN, and BIAS are fully controlled by software.
2. The TFT panel does not use Vbias. The BIAS control used here controls the On/Off switch of the backlights. Program its timing so backlight is on after 12V is applied to the inverter.
3. The SM750 provides three PWM signals that can be used to control brightness.

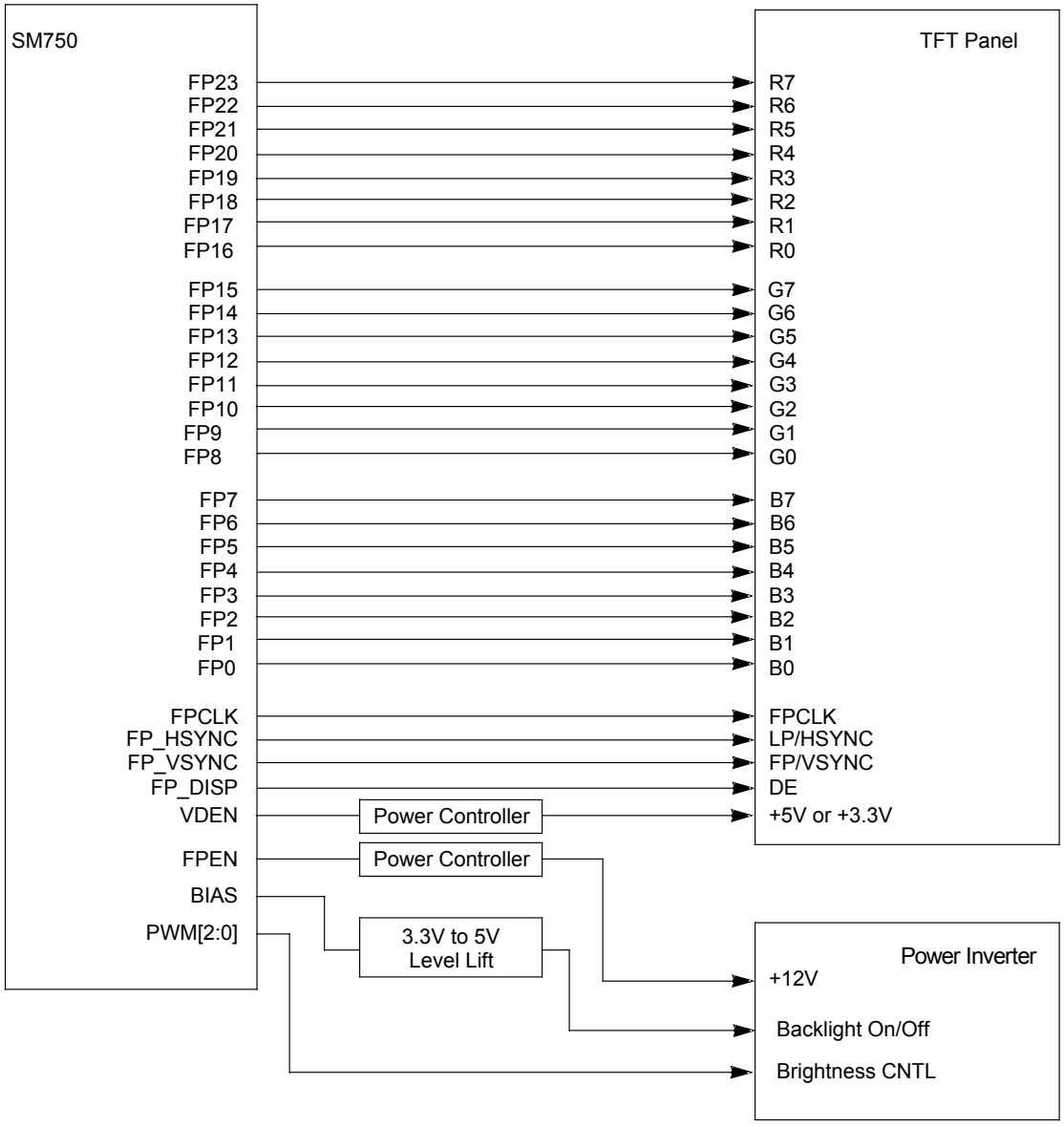


Figure 8: Typical 24-bit TFT Panel Interface

Figure 10 shows a typical interface between the SM750 and two independent 18-bit TFT panels.

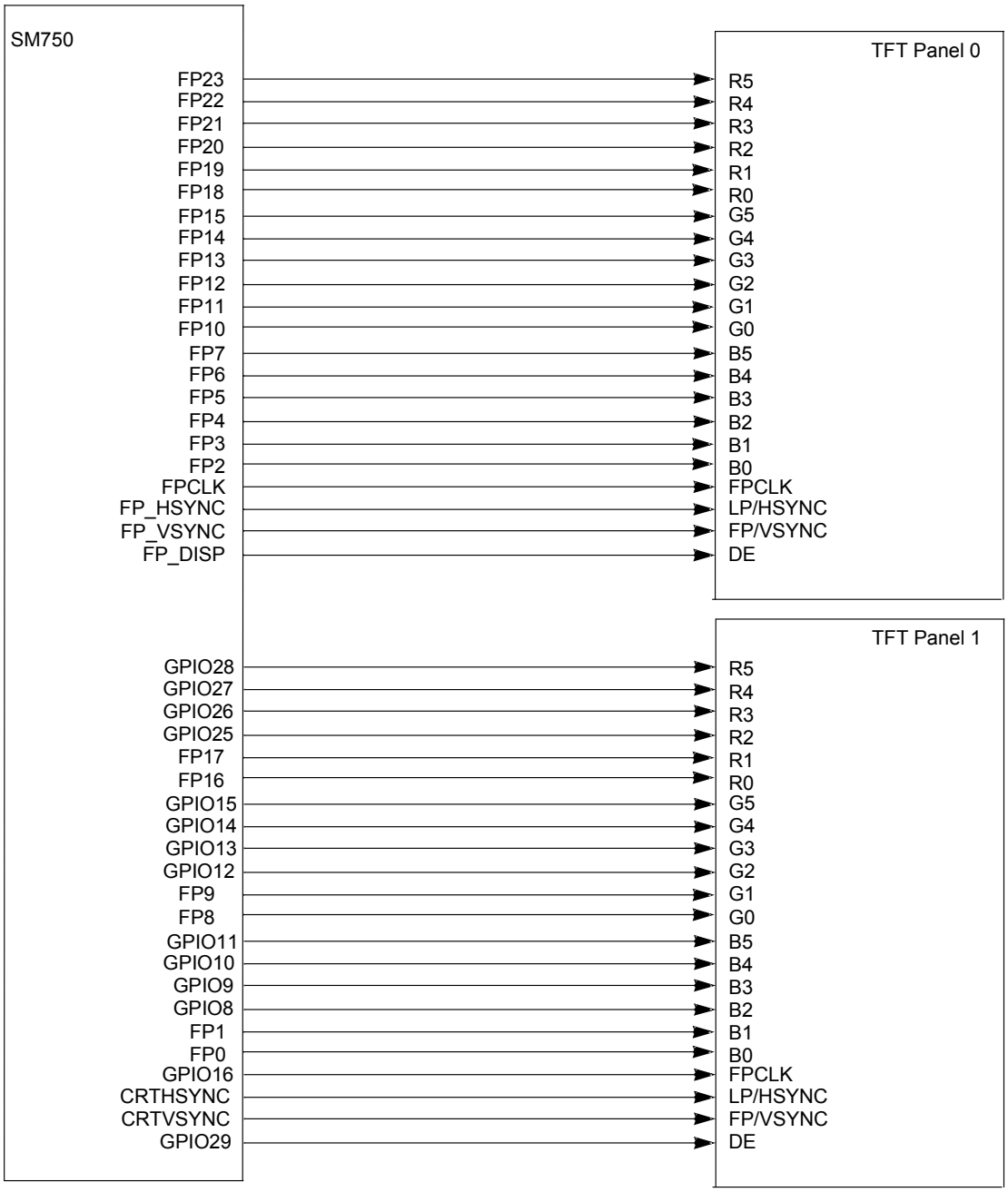


Figure 9: Typical Two 18-bit TFT Panels Interface

Table 6 compares the display data between different TFT modes.

SM750 Pin Name	Single TFT		Dual TFT		
	18-bit	24-bit	18-bit x 2	TFT 0	TFT 1
FPHSYNC	HSYNC	HSYNC	HSYNC	HSYNC	
FPVSYNC	VSYNC	VSYNC	VSYNC	VSYNC	
FPCLK	CLK	CLK	CLK	CLK	
FPDISP	DE	DE	DE	DE	
CRTHSYNC					HSYNC
CRTVSYNC					VSYNC
GPIO16					CLK
GPIO29					DE
GPIO28 (FDATA35)			RB5		R5
GPIO27 (FDATA34)			RB4		R4
GPIO26 (FDATA33)			RB3		R3
GPIO25 (FDATA32)			RB2		R2
GPIO15 (FDATA31)			GB5		G5
GPIO14 (FDATA30)			GB4		G4
GPIO13 (FDATA29)			GB3		G3
GPIO12 (FDATA28)			GB2		G2
GPIO11 (FDATA27)			BB5		B5
GPIO10 (FDATA26)			BB4		B4
GPIO9 (FDATA25)			BB3		B3
GPIO8 (FDATA24)			BB2		B2
FDATA23	R5	R7	RA5	R5	
FDATA22	R4	R6	RA4	R4	
FDATA21	R3	R5	RA3	R3	
FDATA20	R2	R4	RA2	R2	
FDATA19	R1	R3	RA1	R1	
FDATA18	R0	R2	RA0	R0	
FDATA17		R1	RB1		R1
FDATA16		R0	RB0		R0

SM750 Pin Name	Single TFT			Dual TFT	
	18-bit	24-bit	18-bit x 2	TFT 0	TFT 1
FDATA15	G5	G7	GA5	G5	
FDATA14	G4	G6	GA4	G4	
FDATA13	G3	G5	GA3	G3	
FDATA12	G2	G4	GA2	G2	
FDATA11	G1	G3	GA1	G1	
FDATA10	G0	G2	GA0	G0	
FDATA9		G1	GB1		G1
FDATA8		G0	GB0		G0
FDATA7	B5	B7	BA5	B5	
FDATA6	B4	B6	BA4	B4	
FDATA5	B3	B5	BA3	B3	
FDATA4	B2	B4	BA2	B2	
FDATA3	B1	B3	BA1	B1	
FDATA2	B0	B2	BA0	B0	
FDATA1		B1	BB1		B1
FDATA0		B0	BB0		B0

Table 7: Display data between the different TFT modes

1.3.7 Analog RGB (Analog LCD or CRT)

The analog RGB block contains a 24-bit DAC (RGB 8:8:8) to drive an external analog RGB interface. The 300 MHz DAC easily supports the maximum resolution of 1920 x 1440.

1.3.8 GPIO

The SM750 provides 32 bits of GPIO. The table below shows the layout of these bits.

31	30	29	……	25	24	……	20	19	18	17	16	15	……	8	7	……	0
I^2C		SSP1 or FD[35:32]			SSP0			PWM[2:0]			CLKIN or FDSCLK1	ZV Port[15:8] or FD[31:24]			ZV Port[7:0]		

ZV Port

Most ZV-compatible ICs support an 8-bit wide ZV port. The SM750 includes this functionality using GPIO pins 7:0. However, some ICs may only support a 16-bit ZV interface. To support these ICs, GPIO bits 15:8 may be used to add the extra 8 bits to the ZV interface.

PWM

Three independent PWM outputs are provided for generic use. Each output has its own control register. Two PWMs have each three independently selectable frequencies. The third PWM has three selectable frequency multiples that are synchronized to the Video Sync signal.

1.3.9 Strap Pins

MA pins 0 through 12 controls the power-on configuration for the SM750 according to table below:

Pin Name	Default Strapping	Register Bit(s)	Description
BA[1:0]	Pulled-down	MMIO_base + 0x000088[5:4]	Panel Size Selection: 00: 640x480 01: 800x600 10: 1024x768 11: 1280x1024
MA0	Pulled-down	MMIO_base + 0x000004[0]	Embedded Memory Control: (This bit is used to disable embedded local memory) 0: Enable. 1: Disable.
MA1	Pulled-down	MMIO_base + 0x000004[1]	Memory Data Bus Width Selection: 0: 32-bit Memory Data Bus. 1: 64-bit Memory Data Bus.
MA2	Pulled-down	MMIO_base + 0x000004[2]	DDR Drive Strength Selection: 0: Normal DDR Driver Strength. 1: Low DDR Drive Strength.
MA3	Pulled-down	MMIO_base + 0x000004[3]	DDR DLL Selection: 0: DDR DLL Enabled. 1: DDR DLL Disabled.
MA4	Pulled-down	MMIO_base + 0x000004[4]	DDR CAS Selection: 0: 2.5 CAS Latency Clocks. 1: 3 CAS Latency Clocks.
MA[6:5]	Pulled-down	MMIO_base + 0x000004[13:12]	Memory Size Selection: 00: 16MB 01: 32MB 10: 64MB 11: 8MB
MA[8:7]	Pulled-down	MMIO_base + 0x000004[15:14]	Memory Column Size Selection: 00: 256 01: 512 1x: 1024

Pin Name	Default Strapping	Register Bit(s)	Description
MA9	Pulled-down	MMIO_base + 0x000004[16]	Test Clock Selection: 0: Normal XTAL input. 1: Test Clock input.
MA10	Pulled-down		Reserved (must be 0)
MA11	Pulled-down	MMIO_base + 0x000088[0]	Prefetch Selection: 0: Enable Prefetch. 1: Disable Prefetch.
MA12	Pulled-down	MMIO_base + 0x000088[2]	VGA Mode Selection: 0: VGA mode. 1: Non-VGA mode.

1.3.10 DMA Controller

The SM750 supports a DMA controller that can move data from one memory bus to another. DMA1 is used to transfer data between or within memory buses.

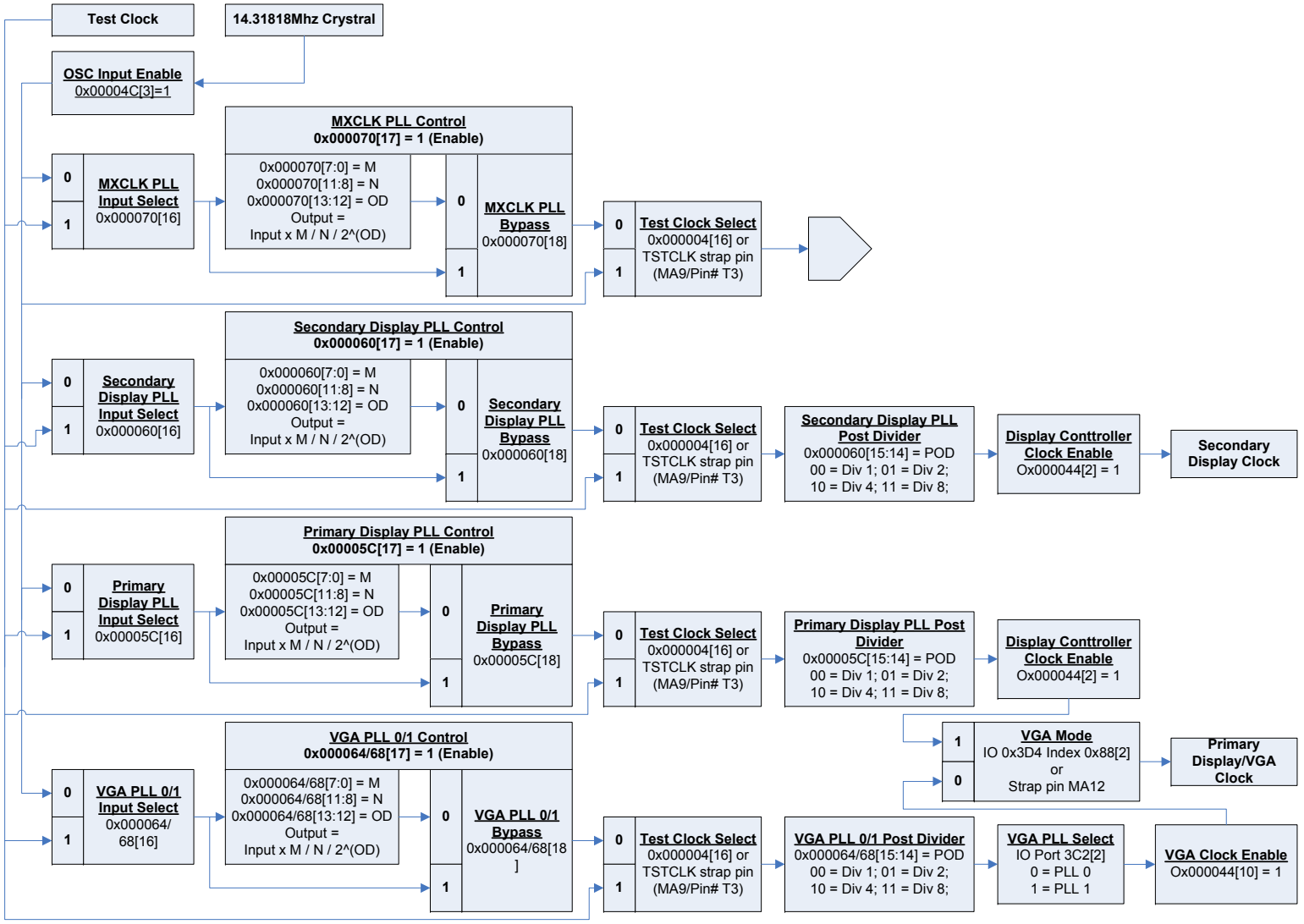
1.3.11 Interrupt Controller

Because the SM750 has only one interrupt to the PCI Express bus, all internal interrupts are shared without priority.

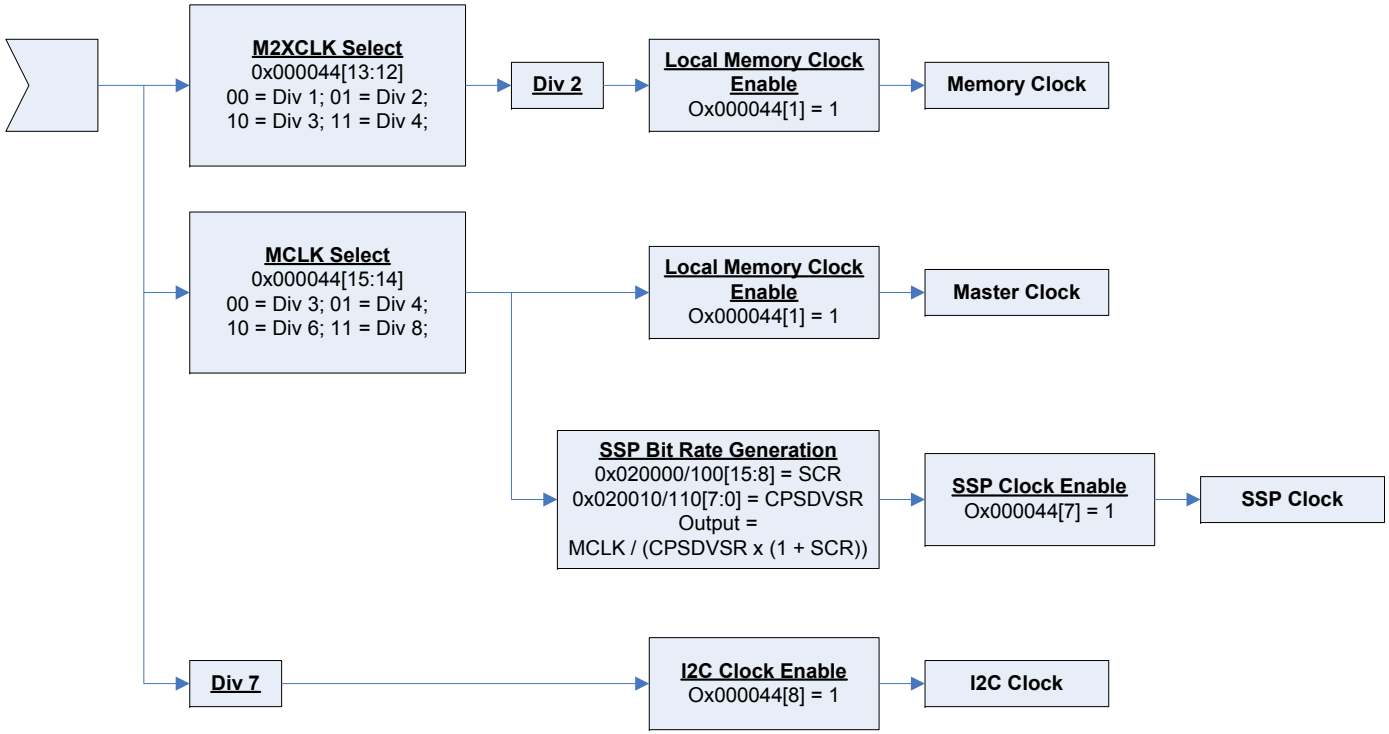
One interrupt status register specifies which module(s) generated the interrupts and the software drivers are responsible for clearing the interrupt at the source. The Host Interrupt remains asserted as long as there is any bit set in the System Interrupt Status register.

1.3.12 Clock Control

The SM750 has one oscillator input and one external clock input. The figure below shows the clock tree for the SM750.



Connecting to the MXCLK PLL Post Divider from the above figure, the figure below shows the detail clock tree for the master clock.



1.3.13 *Power Management*

Figure 11 shows the possible power states the SM750 supports.

During power-on reset, the SM750 comes up in a predefined state with all I/O turned off, and running the lowest possible clock. The software is responsible for programming the Mode 0 power state to the requested state after power-on and transition into the Mode 0 power state.

The Mode 0 and Mode 1 power states are the same and fully under software control. Whenever the software decides that the SM750 must go into a different state, the software programs the non-active power state and transitions into that state. This way there are an infinite number of power states supported by software and makes power management very flexible.

The Sleep power state puts the SM750 into a sleep mode. In this mode the DDR is put into self-refresh mode, and the crystal and PLL circuits are turned off.

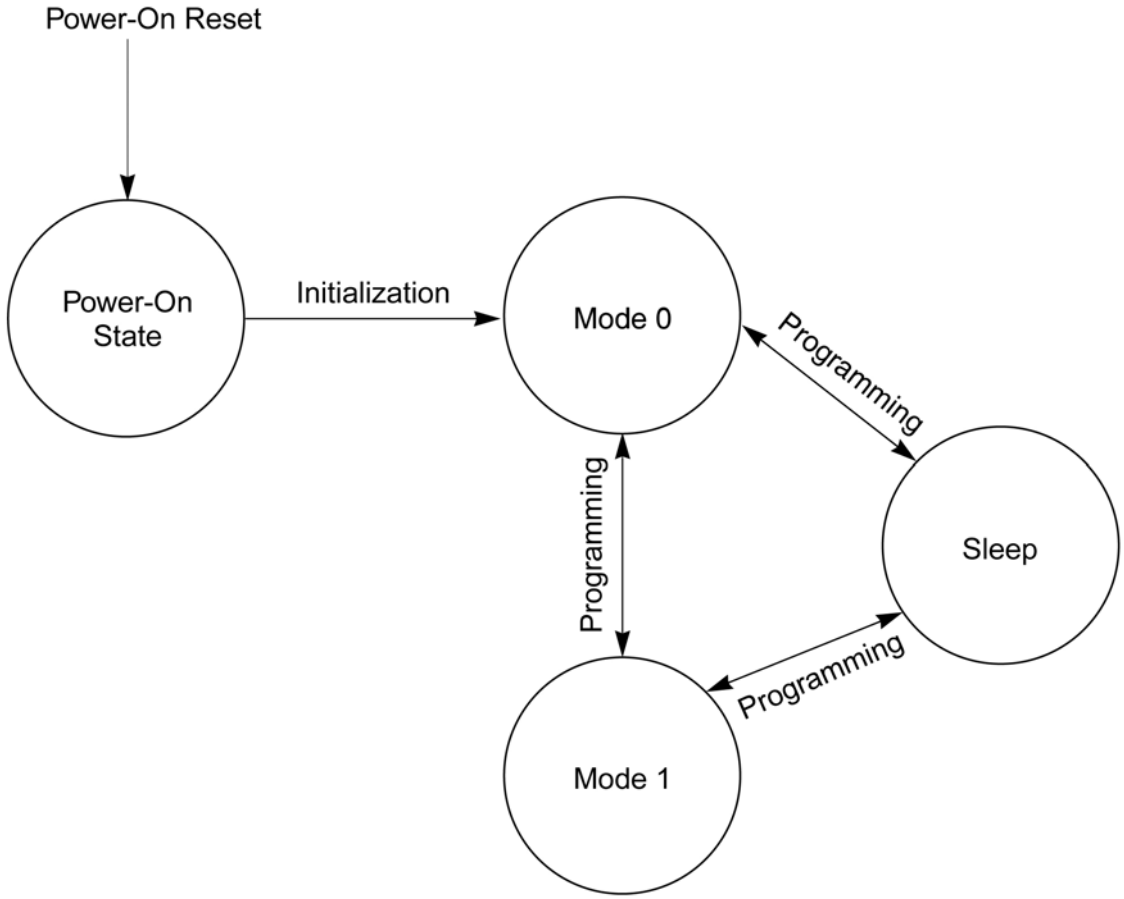


Figure 10: Power State Diagram

Notes: The System Control registers are clocked in the Host clock domain and even shutting off the crystal and PLL circuits does not keep the System Control registers and the host bus from functioning. This way the software is always able to wake up the SM750 from sleep mode.

1.3.14 MMIO Space

The MMIO space contains the SM750 register set and is divided into separate 64kB blocks that hold the registers for each individual functional block of the SM750. If a functional block requires a data port to fill its FIFO, a separate 64kB block is specified for the data port.

Figure 12 shows the MMIO space. Note that the addresses are offsets from the MMIO base address.

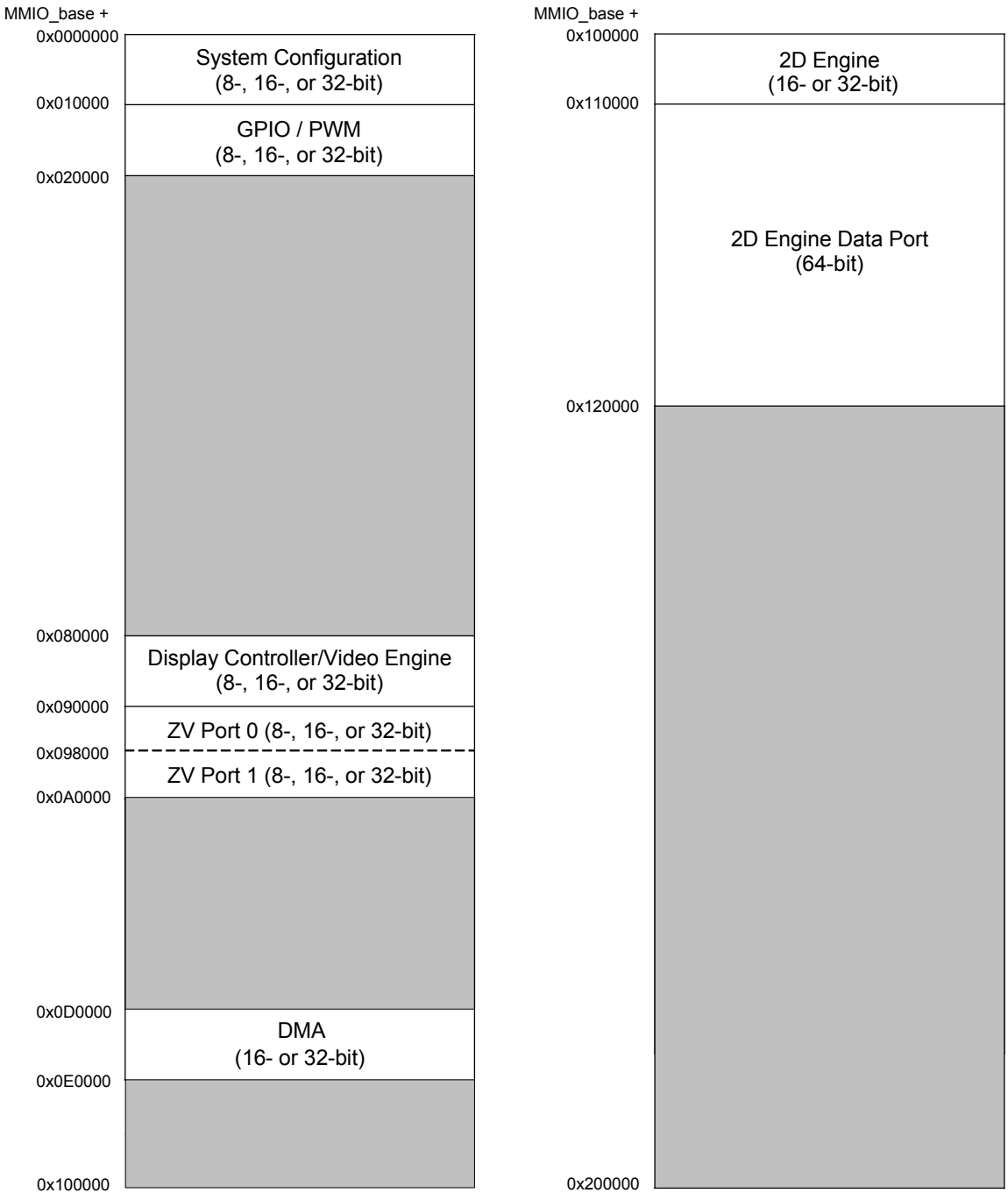


Figure 11: MMIO Space

1.4 Standard VGA

1.4.1 Video BIOS ROM Interface

The Video BIOS contains code for chip power-on initialization, graphics mode setup, and various read/write routines to the frame buffer. The Video BIOS can be burned into a separate video BIOS EPROM (this is the typical case for add-in board design) or be integrated into the system BIOS ROM (this is the typical case for embedded graphics implementation).

More information will be provided later.

1.4.2 Legacy VGA Support

TBA

2. VGA Register

2.1 Functional Overview

The SM750 has Standard VGA Registers and Extended VGA Registers.

2.2 VGA Registers

2.2.1 Register Descriptions

VGA Configuration Register

Read/Write MMIO_base + 0x000088

7	6	5	4	3	2	1	0
Res		BA		Res	VGA	Gra	Pre

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5:4	BA	User Configuration bits configured by BA[1:0]
3	Res	This bit is reserved.
2	VGA	VGA and 0xA0000 accessMode. (Power-on configuration through MA[12]) 0: Use VGA PLL and 0xA0000 access is in planar mode. 1: Use Panel PLL and 0xA0000 access is in linear mode.
1	Gra	Graphic Mode.
0	Pre	Prefetch Enable. (Power-on configuration through MA11) 0: Enable Prefetch. 1: Disable Prefetch.

2.3 Standard VGA Register

MISC: Miscellaneous Output Register

Write Only Address: 3C2

Read Only Address: 3CC

7	6	5	4	3	2	1	0
VSP	HSP	OEM	Res	VIDEO CLOCK		EVR	IO

Bit(s)	Name	Description
7	VSP	VSYNC Polarity Select. 0: Positive VSYNC polarity. 1: Negative VSYNC polarity.
6	HSP	HSYNC Polarity Select. 0: Positive HSYNC polarity. 1: Negative HSYNC polarity.
5	OEM	Odd/Even Memory Page Select. 0: Select lower 64K page of memory. 1: Select upper 64K page of memory.
4	Res	This bit is reserved.
3:2	VIDEO CLOCK	Video Clock Select. 00: 25.175MHz for 640 dots/line mode. 01: 28.322MHz for 720 dots/line mode. 10: Reserved. (enable external clock source) 11: Reserved. (enable external clock source)
1	EVR	Enable Video RAM Access from CPU. 0: Disable. 1: Enable.
0	IO	I/O Address Select. 0: Monochrome mode. Address based at 3Bxh. 1: Color mode. Address based at 3Dxh.

ISR0: Input Status Register 0

Read Only Address: 3C2

7	6	5	4	3	2	1	0
CRT	Res		MDS	Res			

Bit(s)	Name	Description
7	CRT	CRT Vertical Retrace Interrupt. 0: Interrupt is cleared. 1: Interrupt is pending.
6:5	Res	These bits are reserved.
4	MDS	Monitor Detect Status. 0: Monochrome display is detected. 1: Color display is detected.
3:0	Res	These bits are reserved.

ISR1: Input Status Register 1

Read Only Address: 3xA

7	6	5	4	3	2	1	0
Res		COLOR PLANE		VRS	Res		DISPLAY ENABLE

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5:4	COLOR PLANE	Color Plane Diagnostics. These bits return two of the 8 video output VID0-VID7, as selected by Color Plane Enable Register;[5:4]
3	VRS	Vertical Retrace Status. 0: In display mode. 1: In vertical retrace mode.
2:1	Res	These bits are reserved.
0	DISPLAY ENABLE	Display Enable. 0: In display mode. 1: Not in display mode. (it is either in horizontal or vertical retrace mode)

FCR: Feature Control Register

Write Only Address: 3xA

Read Only Address: 3CA

7	6	5	4	3	2	1	0
Res				VSC	Res		

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3	VSC	VYSNC Control. 0: VSYNC output is enabled. 1: VSYNC output is logical 'OR' of VYSNC and Vertical Display Enable.
2:0	Res	These bits are reserved.

SEQX: Sequencer Index Register

Read/Write Address: 3C4

7	6	5	4	3	2	1	0
Res				SEQ			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	SEQ	Sequencer Address/Index The Sequencer address register is written with the index value of the sequencer register to be accessed.

SEQ00: Reset Register

Read/Write Address: 3C5, Index: 00

7	6	5	4	3	2	1	0
Res						SR	AR

Bit(s)	Name	Description
7:2	Res	These bits are reserved.
1	SR	Synchronous Reset. 0: Sequencer is cleared and halted synchronously. 1: Normal operating mode.
0	AR	Asynchronous Reset. 0: Sequencer is cleared and halted asynchronously. 1: Normal operating mode.

SEQ01: Clocking Mode Register

Read/Write Address: 3C5, Index: 01

7	6	5	4	3	2	1	0
Res		SO	VS	DCS	SL	Res	DC

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5	SO	Screen Off. 0: Normal operating mode. 1: Screen is turned off buy SYNC signals remain active.
4	VS	Video Serial Shift Select. 0: Load video serializer every or every other character or clock, depending on Bit 2 of this register. 1: Load video serializer every 4th character clock.
3	DCS	Dot Clock Select. 0: Normal dot clock select by VCLK input frequency. 1: Dot clock is divided by 2 (320 / 360 pixel mode).
2	SL	Shift Load. 0: Load video serializer every character or clock. 1: Load video serializer every other character or clock.
1	Res	This bit is reserved.
0	DC	8/9 Dot Clock. 0: 9 dot wide character clock. 1: 8 dot wide character clock.

SEQ02: Enable Write Plane Register

Read/Write Address: 3C5, Index: 02

7	6	5	4	3	2	1	0
Res				ENW			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	ENW	Enable Writing to Memory Maps 3 through 0. (respectively) 0: Disable writing to corresponding plane. 1: Enable writing to corresponding plane.

SEQ03: Character Map Select Register

Read/Write Address: 3C5, Index: 03

7	6	5	4	3	2	1	0
Res		SCM	SCMB	SCMA	SCMA	SCMB	SCMB

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5, 3, 2	SCMA	Select Character Map A. This value set the portion of plane 2 used to generate text character when bit 3 of this register = 0, according to the following table:
4, 1, 0	SCMB	Select Character Map B. This value set the portion of plane 2 used to generate text character when bit 3 of this register = 1, according to the same table as character Map A.

Bit 5,3,2	Font Table Location
0 0 0	First 8K of plane 2
1 0 0	Second 8K of plane 2
0 0 1	Third 8K of plane 2
1 0 1	Fourth 8K of plane 2
0 1 0	Fifth 8K of plane 2
1 1 0	Sixth 8K of plane 2
0 1 1	Seventh 8K of plane 2
1 1 1	Eighth 8K of plane 2

SEQ04: Memory Mode Register

Read/Write Address: 3C5, Index: 04

7	6	5	4	3	2	1	0
Res				CM	SSA	EVM	Res

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3	CM	Chained 4 Map 0: Enable odd/even mode. 1: Enable Chain 4 mode. Use the two lower bits of CPU address to select plane in video memory as follows:
2	SSA	Select Sequential Addressing Mode. This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective. 0: Enable the odd/even addressing mode. Even addresses access plans 0 and 2, and odd addresses access planes 1 and 3. 1: Enable system to use a sequential addressing mode.
1	EVM	Extended Video Memory Enable. 0: Memory access restricted to 16/32K. 1: Enable extended video memory access. Allows complete memory access to 256K.
0	Res	This bit is reserved.

MA 1	MA 0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

CRTX: CRTC Controller Index Register

Read/Write Address: 3x4

This register is loaded with a binary value that indexes the CRTC controller register where data is to be accessed.

7	6	5	4	3	2	1	0
Res			CRTC				

Bit(s)	Name	Description
7:5	Res	These bits are reserved.
4:0	CRTC	CRTC Address Index. These bits specify the CRTC register to be addressed. Its value is programmed in hexadecimal.

CRT00: Horizontal Total Register

Read/Write Address: 3x5, Index: 00

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active.

7	6	5	4	3	2	1	0
HT							

Bit(s)	Name	Description
7:0	HT	Horizontal Total. This value = (Number of character clocks per scan line) – 5.

CRT01: Horizontal Total Register

Read/Write Address: 3x5, Index: 01

This register defines the number of character clocks for one horizontal line active display.

7	6	5	4	3	2	1	0
HE							

Bit(s)	Name	Description
7:0	HE	Horizontal Display End. This value = (Number of character clocks during active display) – 1.

CRT02: Horizontal Blank Start

Read/Write Address: 3x5, Index: 02

This register defines the number of character clocks at which horizontal ~Blank is asserted.

7	6	5	4	3	2	1	0
HB							

Bit(s)	Name	Description
7:0	HB	Horizontal Blank Start. This value = character value at which ~Blank signal becomes active.

CRT03: Horizontal Blank End

Read/Write Address: 3x5, Index: 03

This register defines the display enable skew and pulse width of ~Blank signal.

7	6	5	4	3	2	1	0
Res	DE		HBE				

Bit(s)	Name	Description
7	Res	This bit is reserved.
6:5	DE	Display Enable Skew. These 2 bits define the display enable skew timing in relation to HSYNC.
4:0	HBE	Horizontal Blank End. Horizontal Blank End has a 6-bit value. This register contains the least significant 5-bits of this value. Bit 6 of this value is at CRTC index 05 bit 7.

DESKW 1	DESKW 0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

CRT04: Horizontal Sync Pulse Start

Read/Write Address: 3x5, Index: 04

This register is used to adjust screen position horizontally and to specify the position at which HSYNC is active.

7	6	5	4	3	2	1	0
HSPS							

Bit(s)	Name	Description
7:0	HSPS	Horizontal Sync Pulse Start. This value = character clock count value at which HSYNC becomes active.

CRT05: End Horizontal Sync Pulse

Read/Write Address: 3x5, Index: 05

This register defines the horizontal sync skew and pulse width of HSYNC signal.

7	6	5	4	3	2	1	0
HBE	HSS		HSE				

Bit(s)	Name	Description
7	HBE	Horizontal Blank End Bit 5.
6:5	HSS	Horizontal Sync Skew. These 2 bits define the HSYNC signal skew timing in relation to HSYNC pulses.
4:0	HBE	Horizontal Sync End. Horizontal Sync End has a 5-bit value. This value defines the character clock counter value at which HSYNC becomes inactive.

HSSKW 1	HSSKW 0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

CRT06: Vertical Total

Read/Write Address: 3x5, Index: 06

This register defines the number of scan lines from VSYNC going active to the next VSYNC going active. Vertical total has a 11-bit value. Bit 8 of this value is located at CRT07 bit 0. Bit 9 of this value is located at CRT07 bit 5. Bit 10 of this value is located at CRT30 bit 3.

7	6	5	4	3	2	1	0
VT							

Bit(s)	Name	Description
7:0	VT	Vertical Total. Vertical Total has a 11-bit value. This register contains the least significant 8-bits of this value. This value = (number of scan lines from VSYNC going active to the next VSYNC) – 2.

CRT07: Overflow Vertical

Read/Write Address: 3x5, Index: 07

This register specifies the CRTC vertical overflow registers.

7	6	5	4	3	2	1	0
VSS	VDE	VT	LC	VBS	VSS	VDE	VT

Bit(s)	Name	Description
7	VSS	Vertical Sync Start Bit 9.
6	VDE	Vertical Display Enable End Bit 9.
5	VT	Vertical Total Bit 9.
4	LC	Line Compare Bit 8.
3	VBS	Vertical Blank Start Bit 8.
2	VSS	Vertical Sync Start Bit 8.
1	VDE	Vertical Display Enable End Bit 8.
0	VT	Vertical Total Bit 8.

CRT08: Preset Row Scan

Read/Write Address: 3x5, Index: 08

This register is used for panning and text scrolling.

7	6	5	4	3	2	1	0
Res	BP		PRSC				

Bit(s)	Name	Description
7	Res	This bit is reserved.
6:5	BP	Horizontal Sync Skew. These 2 bits define the HSYNC signal skew timing in relation to HSYNC pulses. **BPC 1** / **PBC 0** / **Operation** 0 / 0 / Normal 0 / 1 / 1Byte left shift 1 / 0 / 2Byte left shift 1 / 1 / 3Byte left shift
4:0	PRSC	Preset Row Scan Count These bits preset the vertical row scan counter once after each vertical retrace. This counter is automatically incremented by 1 after each horizontal sync period. Once the max row scan count is reached, this counter is cleared. This is useful for smoothing vertical text scrolling.

CRT09: Maximum Scan Line

Read/Write Address: 3x5, Index: 09

This register defines the max number of scan lines per character row and provides one scanning control and two overflow bits.

7	6	5	4	3	2	1	0
EDS	LC	VB	MSL				

Bit(s)	Name	Description
7	EDS	Enable Double Scan. 0: Normal. 1: Enable Double Scan. The row scan counter is clocked at half of the HSYNC rate.
6	LC	Line Compare Register Bit 9.
5	VB	Vertical Blank Start Register Bit 9.
4:0	MSL	Maximum Scan Line. This value equals to the total number of scan lines per character row – 1.

CRT0A: Cursor Start Scan Line

Read/Write Address: 3x5, Index: 0A

This register defines the row scan of a character line at which the cursor begins and enable/disable cursor.

7	6	5	4	3	2	1	0
Res		EC	CSSL				

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5	EC	Enable Cursor. 0: Cursor is ON. 1: Cursor is OFF.
4:0	CSSL	Cursor Start Scan Line. This value equals to the starting cursor row within the character box. If this value is programmed with a value greater than the Cursor End Scan Line Register, no cursor will be displayed.

CRT0B: Cursor End Scan Line

Read/Write Address: 3x5, Index: 0B

This register defines the row scan of a character line at which the cursor begins and enable/disable cursor.

7	6	5	4	3	2	1	0
Res	CS		CESL				

Bit(s)	Name	Description
7	Res	This bit is reserved.
6:5	CS	Cursor skew. These 2 bits define the cursor delay skew timing, which moves the cursor to the right, in character clock.

CSKW 1	CSKW 0	Character Clock Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit(s)	Name	Description
4:0	CESL	Cursor End Scan Line. This value equals to the ending cursor row within the character box. If this value is programmed with a value less than the Cursor Start Scan Line Register, no cursor will be displayed.

CRT0C: Display Start Address High

Read/Write Address: 3x5, Index: 0C

This register defines the high order first address after a vertical retrace at which the display on the screen begins on each screen refresh. This value is a 19-bit value. Bit [18:16] are located in CRT30 [6:4]. Bit [7:0] are located in CRT0D.

7	6	5	4	3	2	1	0
DSA							

Bit(s)	Name	Description
7:0	DSA	Display Start Address [15:8].

CRT0D: Display Start Address Low

Read/Write Address: 3x5, Index: 0D

This register defines the low order first address.

7	6	5	4	3	2	1	0
SA [7:0]							

Bit(s)	Name	Description
7:0	SA[7:0]	Start Address [7:0]. This register is the low order byte of the address [7:0].

CRT0E: Cursor Location High

Read/Write Address: 3x5, Index: 0E

This register defines the high order cursor location address. This value is a 19-bit value along with CRT30 [6:4] are the high order bits of the address.

7	6	5	4	3	2	1	0
CLH							

Bit(s)	Name	Description
7:0	CLH	Cursor Location High. This register is the high order byte of the cursor location address.

CRT0F: Cursor Location Low

Read/Write Address: 3x5, Index: 0F

This register defines the low order cursor location address.

7	6	5	4	3	2	1	0
CLL							

Bit(s)	Name	Description
7:0	CLL	Cursor Location Low. This register is the low order byte of the cursor location address.

CRT10: Vertical Sync Pulse Start

Read/Write Address: 3x5, Index: 10

This register is used to adjust screen position vertically and to specify the position at which VSYNC is active. Bit 10 of this value is in CRT30 [0]. Bit 9 is in CRT07 [7]. Bit 8 is in CRT07 [2].

7	6	5	4	3	2	1	0
VSPS							

Bit(s)	Name	Description
7:0	VSPS	Vertical Sync Pulse Start. Vertical Sync Start has a 11-bit value. This is the 8 LSB of this value. This value = number of scan lines at which VSYNC becomes active.

CRT11: Vertical Sync Pulse End

Read/Write Address: 3x5, Index: 11

This register is used to control vertical interrupt, vertical sync end CRT0-7 Write protect.

7	6	5	4	3	2	1	0
LW	RCS	DVI	CVI	VSPE			

Bit(s)	Name	Description
7	LW	Lock writing to CRTC register (CRT00-07). 0: Enable writing. 1: Disable writing, except CRT07 [4].
6	RCS	Refresh Cycle Select (3/5). 0: 3 DRAM refresh cycle per Horizontal scan line. 1: 5 DRAM refresh cycle per Horizontal scan line.
5	DVI	Disable Vertical Interrupt. 0: Enable. 1: Disable.
4	CVI	Clear Vertical Interrupt. 0: Clear. 1: Vertical Retrace Interrupt. This allows an interrupt to be generated at the end of active vertical display.
3:0	VSPE	Vertical Sync Pulse End. This value = number of scan lines at which VSYNC becomes inactive.

CRT12: Vertical Display End

Read/Write Address: 3x5, Index: 12

This register defines the number of scan line where the display on the screen ends. Bit 10 of this value is in CRT30 [2]. Bit 9 is in CRT07 [6]. Bit 8 is in CRT07 [1].

7	6	5	4	3	2	1	0
VDE							

Bit(s)	Name	Description
7:0	VDE	Vertical Display End. Vertical Display End has a 11-bit value. This register contains the 8 LSB of this value. This value = (number of scan lines during active display) -1.

CRT13: Offset

Read/Write Address: 3x5, Index: 13

This register defines the logical line width of the screen. The starting memory address for the next display row is larger than the current row by 2 (byte mode), 4 (word mode), or 8 (DWORD mode) times this offset.

7	6	5	4	3	2	1	0
LSW							

Bit(s)	Name	Description
7:0	LSW	Logical Screen Width. It has a 10-bit value. This register contains the 8 LSB of this value. The addressing mode is set by CRT14 [6] and CRT17 [3].

CRT14: Underline Location

Read/Write Address: 3x5, Index: 14

This register defines the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
Res	DWS	CS	ULL				

Bit(s)	Name	Description
7	Res	This bit is reserved.
6	DWS	DWORD Mode Select. 0: The memory address are byte or word addresses. 1: The memory address are DWORD addresses.
5	CS	Count by 4 Select. 0: The memory address counter depends on CRT17 [3]. 1: The memory address counter is incremented every four character clocks.
4:0	ULL	Under Line Location. It has a 5-bit value. This value = (scan line count of a character row on which an underline occurs) – 1.

CRT15: Vertical Blank Start

Read/Write Address: 3x5, Index: 15

This register defines the number of scan lines at which vertical blank is asserted. Bit 10 is in CRT30 [1], Bit 9 is in CRT09 [5], and Bit 8 is in CRT07 [3].

7	6	5	4	3	2	1	0
VBS							

Bit(s)	Name	Description
7:0	VBS	Vertical Blank Start (The 8 LSB of a 11-bit value). This value = (scan line count at which vertical blank signal becomes active) – 1.

CRT16: Vertical Blank End

Read/Write Address: 3x5, Index: 16

This register defines the number of scan lines at which vertical blank is de-asserted.

7	6	5	4	3	2	1	0
VBE							

Bit(s)	Name	Description
7:0	VBE	Vertical Blank End (This is a 8-bit value). This value = [(scan line count at which vertical blank signal becomes active) – 1] + (desired width of vertical blanking pulse in scan lines).

CRT17: CRT Mode Control

Read/Write Address: 3x5, Index: 17

This register defines the controls for CRT mode.

7	6	5	4	3	2	1	0
HR	BAS	AW	Res	WS	HCS	EGA	CGA

Bit(s)	Name	Description
7	HR	Hardware Reset for HSYNC and VSYNC. 0: HSYNC and VSYNC inactive. 1: HSYNC and VSYNC active.
6	BAS	Byte Address Mode Select. 0: Word address mode. All memory address counter bits shift down by one bit and the MSB of the address counter appears on the LSB. 1: Byte address mode.
5	AW	Address Wrap. 0: In word mode, memory address counter bit 13 appears on the memory address output of the CRT controller and the video memory address wraps around at 16KB. 1: In word mode, memory address counter bit 15 appears on the memory address bit 0 signal of the CRTC controller.
4	Res	This bit is reserved.
3	WS	Word Mode Select. 0: Byte mode addressing is selected and memory address counter is clocked by the character clock input. 1: Word mode addressing is selected and memory address counter is clocked by the character clock divided by 2.
2	HCS	Horizontal Retrace Clock Select. 0: Select horizontal retrace clock rate. 1: Select horizontal retrace clock rate divided by 2.
1	EGA	EGA Emulation. 0: Row scan counter bit 1 is replaced by memory address bit 14 during active display time. 1: Memory address bit 14 appears on the memory address output bit 14 signal of the CRT controller.
0	CGA	CGA Emulation. 0: Row scan counter bit 0 is replaced by memory address bit 13 during active display time. 1: Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller.

CRT18: Line Compare

Read/Write Address: 3x5, Index: 18

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0.

7	6	5	4	3	2	1	0
LC							

Bit(s)	Name	Description
7:0	LC	Line Compare. This value = Number of scan lines at which the screen is split into screen 1 and screen 2.

CRT22: Graphics Controller Data Latches Readback

Read/Write Address: 3x5, Index: 22

This register is used to read the CPU latches in the graphic controller.

7	6	5	4	3	2	1	0
DL							

Bit(s)	Name	Description
7:0	DL	Graphic Controller CPU Data Latches. Bits 1-0 of GR4 select the latch number N (3-0) of the CPU latch.

CRT24: Attribute Controller Toggle Latches Readback

Read/Write Address: 3x5, Index: 24

This register is used to provide access to the attribute controller toggle.

7	6	5	4	3	2	1	0
ACS	Res						

Bit(s)	Name	Description
7	ACS	Attribute Controller Index Select. 0: The attribute controller reads or writes and index value on the next access. 1: The attribute controller reads or writes a data value on the next access.
6:0	Res	These bits are reserved.

CRT26: Attribute Controller Toggle Latches Readback

Read/Write Address: 3x5, Index: 26

This register is used to provide access to the attribute controller index.

7	6	5	4	3	2	1	0
Res		VES	ACI				

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5	VES	Video Enable Status. This bit provides status of the video display enable bit in Attribute Controller (3C0h) index bit 5.
4:0	ACI	Attribute Controller Index. This value is the attribute controller index data at 3C0h.

GRXX: Graphics Controller Index

Read/Write Address: 3CE

This register is loaded with a binary value that indexes the graphics controller register where data is to be accessed.

7	6	5	4	3	2	1	0
Res				GC			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	GC	Graphics Controller Address Index. These bits specify the graphics controller register to be addressed. The value is in hexadecimal.

GRX00: Set/Reset

Read/Write Address: 3CF, Index: 00

This register represents the value written to all 8-bits of the corresponding memory planes when CPU executes a memory write in write mode 0.

7	6	5	4	3	2	1	0
Res				SRP			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	SRP	Set/Reset Plane [3:0] In write mode 0, the set/reset data can be enabled on the corresponding bit of the bit of Enable Set/Reset Data register. These bits become the color value for CPU memory write operations.

GRX01: Enable Set/Reset

Read/Write Address: 3CF, Index: 01

This register enables the set/reset register in write mode 0.

7	6	5	4	3	2	1	0
Res				ESRP			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	ESRP	Enable Set/Reset Plane [3:0] In write mode 0, the enable set/reset bits allow writing to the corresponding planes with the data in set/reset register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

GRX02: Color Compare

Read/Write Address: 3CF, Index: 02

This register is used to compare with the CPU memory read data. This register works in conjunction with the Color Don't Care Register.

7	6	5	4	3	2	1	0
Res				CCP			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	CCP	Color Compare Plane [3:0] These bits represent the reference color used to compare each pixel in corresponding plane. A logical 1 is returned in each plane bit position when color matches.

GRX03: Data Rotate/ROP

Read/Write Address: 3CF, Index: 03

This register is used to control rotation and raster operations.

7	6	5	4	3	2	1	0
Res			ROS		RC		

Bit(s)	Name	Description
7:5	Res	These bits are reserved.
4:3	ROS	Raster Operations Select: 00: No operation. 01: Logical AND with latched data. 10: Logical OR with latched data. 11: Logical XOR with latched data.
2:0	RC	Rotate Count. These bits specify the number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0. To write non-rotated data, the CPU must present a count with 0.

GRX04: Read Plane Select

Read/Write Address: 3CF, Index: 04

This register selects which memory plane the CPU data is reading from in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored.

7	6	5	4	3	2	1	0
Res						RP	

Bit(s)	Name	Description
7:2	Res	These bits are reserved.
1:0	RP	Read Plane Select: 00: Plane 0 01: Plane 1 10: Plane 2 11: Plane 3

GRX05: Graphics Mode

Read/Write Address: 3CF, Index: 05

7	6	5	4	3	2	1	0
Res	CS	CES	OEA	ERC	Res	WM	

Bit(s)	Name	Description
7	Res	This bit is reserved.
6	CS	256 Color Shift Mode Select. 0: Enable bit 5 of this register to control loading of the shift registers. 1: Shift registers are loaded that It supports the 256 color mode.
5	CES	Odd/Even Shift Mode Select. 0: Normal shift mode. 1: The video shift registers are directed to format the serial data stream with even numbered bits from both planes on the even numbered planes and odd numbered bits from both planes on the odd planes.
4	OEA	Odd/Even Addressing Select. 0: Normal addressing. 1: CGA odd/even addressing mode is selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3. Enable Read Compare. 0: System read data from memory planes selected by read map select register. This is called read mode 0. 1: System read the result of logical comparison between the data in 4 memory planes selected by the Color Don't Care Register and the Color Compare Register. The result is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1.
3	ERC	Enable Read Compare. 0: System read data from memory planes selected by read map select register. This is called read mode 0. 1: System read the result of logical comparison between the data in 4 memory planes selected by the Color Don't Care Register and the Color Compare Register. The result is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1.
2	Res	This bit is reserved.
1:0	WM	Write Mode Select. 00: Write mode 0. Each of four video planes is written with CPU data rotated by the number of counts in rotate register. If Set/Reset register is enabled for any of the four planes, the corresponding planes is written with the data stored in the Set/Reset register. 01: Write mode 1. Each of four video planes is written with CPU data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, Set/Reset data, enable Set/Reset data and bit mask registers are ignored. 10: Write mode 2. Video planes [3:0] are written with the value of CPU write data [3:0]. The 32-bit output from the four planes is then operated on by the Bit Mask register and the resulting data are written into the four planes. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored. 11: Write mode 3. Each of the four video planes is written with 8-bit of the color value in the Set/Reset register for the corresponding plane. The bit-position-enable field is formed with the logical AND of the Bit Mask register and rotated CPU data. The Enable Set/Reset register is ignored.

GRX06: Graphics Miscellaneous

Read/Write Address: 3CF, Index: 06

This register controls video memory addressing.

7	6	5	4	3	2	1	0
Res				MM		OES	GMS

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:2	MM	Memory Map Mode. 00: A0000h to BFFFFh (128KB). 01: A0000h to AFFFFh (64KB). 10: B0000h to B7FFFh (32KB). 11: B8000h to BFFFFh (32KB).
1	OES	Odd/Even Mode Select. 0: CPU address bit A0 is the memory address bit MA0. 1: CPU address A0 is replaced by a higher order address bit. A0 is then used to select odd or even maps. A0 = 0, select Map 2 or 0; A0 = 1, select Map 3 or 1.
0	GMS	Graphics Mode Select. 0: Select Text mode. 1: Select Graphics mode.

GRX07: Color Don't Care Plane

Read/Write Address: 3CF, Index: 07

This register controls whether the corresponding bit of the GRX02 is to be ignored or used for color comparison. It is used with GRX02 for Read Mode 1 accesses.

7	6	5	4	3	2	1	0
Res				CPS			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	CPS	Compare Plane Select. 0: The corresponding color plane becomes a not care plane when CPU read from the video memory is performed in read mode 1. 1: The corresponding color plane is used for color comparison with the data in GRX02.

GRX08: Bit Mask

Read/Write Address: 3CF, Index: 08

This register controls bit mask operations which applies simultaneously to all four maps. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BM							

Bit(s)	Name	Description
7:0	BM	Bit Mask 0: Corresponding bit of each plane in memory is set to the corresponding bit in the processor latches. 1: Corresponding bit of each plane in memory is set as specified by other conditions.

ATRX: Attribute Controller Index

Read/Write Address: 3C0

This register is loaded with a binary value that indexes the attribute controller register where data is to be accessed.

7	6	5	4	3	2	1	0
Res		PAS	ACA				

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5	PAS	Palette Address Source. 0: Disable internal color palette outputs and video outputs to allow CPU access to color palette registers. 1: Enable internal color palette and normal video translation.
4:0	ACA	Attribute Controller Address A binary value that points to the attribute controller register where data is to be written.

ATR00-0F: Palette

Read/Write Address: 3C1/3C0, Index: 00 - 0F

7	6	5	4	3	2	1	0
Res		PC					

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5:0	PC	Palette Colors. 0: Corresponding pixel color is de-selected. 1: Corresponding pixel color is enabled.

ATR10: Attribute Mode Control

Read/Write Address: 3C1/3C0, Index: 10

This register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
VID	CS	PPE	Res	BIS	LGC	MCE	TGM

Bit(s)	Name	Description
7	VID	VID5, VID4 Select 0: VID5 and VID4 palette register outputs are selected. 1: Color Select Register bit 1 and bit 0 are selected for outputs.
6	CS	256 Color Select 0: Disable 256 color mode pixel width. PCLK rate = internal dot clock rate. 1: Enable 256 color mode pixel width. PCLK rate = internal dot clock rate divided by 2.
5	PPE	Pixel Panning Enable. 0: Line compare will have no effect on the output of the pixel panning register. 1: Forces the output of the pixel panning register to 0 after matching line compare until VSYNC is active.
4	Res	This bit is reserved.
3	BIS	Blinking and Intensity Select 0: Select background intensity from the text attribute byte. 1: Select blink attribute in text modes.
2	LGC	Line Graphics Character Enable. 0: Forces the ninth dot to be the same color as the background in line graphics character codes. 1: Enable special line graphics character codes.
1	MCE	Mono/Color Emulation. 0: Select color display text attribute. 1: Select monochrome display text attribute.
0	TGM	Text/Graphics Mode Select. 0: Select text attribute control mode. 1: Select graphics control mode.

ATR11: Overscan Color

Read/Write Address: 3C1/3C0, Index: 11

This register controls the overscan or border color.

7	6	5	4	3	2	1	0
OC							

Bit(s)	Name	Description
7:0	OC	Overscan Color. The value determines the overscan or border color displayed on the CRT screen.

ATR12: Color Plane Enable

Read/Write Address: 3C1/3C0, Index: 12

This register enables the respective video memory color plane 0-3 and selects the video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
Res		VS		CPE			

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5:4	VS	Video Status Multiplexer. These bits select two out of the 8 color outputs which can read by the Input Status Register 1 bit 5 and bit 4.
3:0	CPE	Color Plane Enable. 0: Disable the corresponding color planes. 1: Enable the corresponding color planes.

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID7

ATR13: Horizontal Pixel Panning

Read/Write Address: 3C1/3C0, Index: 13

This register specifies the number of pixels to shift the display data horizontal to the left.

7	6	5	4	3	2	1	0
Res				HPP			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	HPP	Horizontal Pixel Panning. These 4 bits determine the horizontal left shift of the video data in number of pixels. In the 9 pixel/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixel/character text mode and all graphics modes, except for 256 color mode, a maximum shift of 7 pixels is allowed. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

Bit 3:0	9 pixel/char	8 pixel/char	256 color mode
0000	1	0	0
0001	2	1	-
0010	3	2	1
0011	4	3	-
0100	5	4	2
0101	6	5	-
0110	7	6	3
0111	8	7	-
1000	0	-	-

ATR14: Color Select

Read/Write Address: 3C1/3C0, Index: 14

This register specifies the high order bits of video output when pixel padding is enable/disabled for 256 color modes.

7	6	5	4	3	2	1	0
Res				SC7/6		SC5/4	

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:2	SC7/6	Select Color 7 and Color 6. These are the two most significant bits of the 8 bits color value for video DAC. These are normally used in all modes except 256 color modes.
1:0	SC5/4	Select Color 5 and Color 4. These bits can be substituted for VID5 and VID4 from the palette registers to form the 8-bit color value for video DAC.

3C6: DAC Mask

Read/Write Address: 3C6

This register is the pixel read mask register to select pixel video output.

7	6	5	4	3	2	1	0
DAM							

Bit(s)	Name	Description
7:0	DAM	DAC Address Mask This field is the pixel mask for palette DAC. When a bit in this field is programmed to 0, the corresponding bit in the pixel data is ignored in looking up an entry I the Color Lookup Table. This register is initialized to FFh by the BIOS during a video mode set.

3C7W: DAC Address Read

Read/Write Address: 3C7

This register contains the pointer to one of the 256 palette data registers and is used when reading the color palette. A write to this register causes 11b to be driven out to the RAMDAC output.

7	6	5	4	3	2	1	0
DRA							

Bit(s)	Name	Description
7:0	DRA	DAC Read Address After a color code is written into this register, the chip will identifies that a DAC read sequence will occur. A read sequence consists of three consecutive byte reads from the RAMDAC data register at 3C9h.

3C7R: DAC Status

Read/Write Address: 3C7

This register specifies the DAC status: read or write cycles.

7	6	5	4	3	2	1	0
Res						DS	

Bit(s)	Name	Description
7:2	Res	These bits are reserved.
1:0	DS	DAC Status. 00: DAC write operation in progress. 11: DAC read operation in progress.

3C8: DAC Address Write

Read/Write Address: 3C8

This register contains the pointer to one of the 256 palette data registers and is during a palette load. A write to this register causes 11b to be driven out to the RAMDAC output.

7	6	5	4	3	2	1	0
DWA							

Bit(s)	Name	Description
7:0	DWA	DAC Write Address. After a color code is written into this register, the chip identifies that a DAC write sequence will occur. A write sequence consists of three consecutive byte reads from the RAMDAC data register at 3C9h.

3C9: DAC Data

Read/Write Address: 3C9

This register is the data port to read or write the contents of the location in the Color Lookup Table pointed to by the DAC Read Address or the DAC Write Address registers. An access to this register will caused 01b to be driven to RAMDAC outputs.

7	6	5	4	3	2	1	0
DD							

Bit(s)	Name	Description
7:0	DD	DAC Read/Write Data. These read/write register bits store the pixel data for the palette DAC.

2.4 Extended VGA Registers

MMIO Address 0 Register

Read/Write Address: 3D4, Index: 80

7	6	5	4	3	2	1	0
Addr R/W							

Bit(s)	Name	Description
7:0	Addr	MMIO Address [7:0]

MMIO Address 1 Register

Read/Write Address: 3D4, Index: 81

7	6	5	4	3	2	1	0
Addr R/W							

Bit(s)	Name	Description
7:0	Addr	MMIO Address [15:8]

MMIO Address 2 Register

Read/Write Address: 3D4, Index: 82

7	6	5	4	3	2	1	0
Addr R/W							

Bit(s)	Name	Description
7:0	Addr	MMIO Address [23:16]

MMIO Data 0 Register

Read/Write Address: 3D4, Index: 84

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	MMIO Data [7:0]

MMIO Address 1 Register

Read/Write Address: 3D4, Index: 85

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	MMIO Data [15:8]

MMIO Address 2 Register

Read/Write Address: 3D4, Index: 86

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	MMIO Data [23:16]

MMIO Address 3 Register

Read/Write Address: 3D4, Index: 87

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	MMIO Data [31:24]

To write data into MMIO register via IO port, programs MMIO address into MMIO address registers, write high order data into data register 1-3 (index 85-87), write low order data into data register 0 will generate MMIO write cycle.

To read data from MMIO register via IO port, programs MMIO address into MMIO address registers, read the corresponding data register will generate MMIO read cycle.

VGA Configuration Register

Read/Write Address: 3D4, Index: 88

7	6	5	4	3	2	1	0
Res		BA		Res	VGA	Gra	Res

Bit(s)	Name	Description
7:6	Res	These bits are reserved.
5:4	BA	User Configuration bits configured by BA[1:0]
3	Res	This bit is reserved.
2	VGA	VGA and 0xA0000 access Mode. (Power-on configuration through MA[12]) 0: Use VGA PLL and 0xA0000 access is in planar mode. 1: Use Panel PLL and 0xA0000 access is in linear mode.
1	Gra	Graphic Mode. 0: VGA mode. 1: Graphic mode.
0	Res	This bit is reserved.

VGA Base Register

Read/Write Address: 3D4, Index: 89

7	6	5	4	3	2	1	0
VB R/W							

Bit(s)	Name	Description
7:0	VB	VGA Base Address [7:0]

VGA Base Register

Read/Write Address: 3D4, Index: 8A

7	6	5	4	3	2	1	0
VB R/W							

Bit(s)	Name	Description
7:2	Res	These bits are reserved.
1:0	VB	VGA Base Address [9:8]

In VGA mode, a 26-bits Local Memory address is generated by 10 bits (VGA Base Register) + 16 bits VGA Address. In other words, this is a page register to span 64M of frame buffer memory with a 64K address window.

VGA Scratch Data Register

Read/Write Address: 3D4, Index: 8B – 9F

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	Scratch Data

3. System Configuration

3.1 Functional Overview

The SM750 has only one interrupt to the host bus. All internal interrupts are shared without priority.

3.2 Register Descriptions

Table 7 shows the System Configuration Register offsets and general functions.

Address Offset from MMIO_base	Type	Width	Reset Value	Register Name
Configuration 1				
0x000000	R/W	32	0x00A00000	System Control
0x000004	R/W	32	0x01006066	Miscellaneous Control
0x000008	R/W	32	0x1F000000	$GPIO_{31:0}$ Control
0x00000C	R/W	32	0x01765324	Local Memory Arbitration Control
0x000010	R/W	32	0x01765324	PCI Express Bus Master Memory Arbitration Control
0x000014	R/W	32	0x00000000	Arbitration Control
0x000020	R	32	0x00000000	Raw Interrupt Status
0x000020	W	32	0x00000000	Raw Interrupt Clear
0x000024	R	32	0x00000000	Interrupt Status
0x000028	R/W	32	0x00000000	Interrupt Mask
0x00002C	R/W	32	0x00000000	Debug Control
Power Management				
0x000040	R	32	0x00005FC6	Current Clock Status
0x000044	R/W	32	0x00005FC6	Power Mode 0 Clock Control
0x000048	R/W	32	0x00005FC6	Power Mode 1 Clock Control
0x00004C	R/W	32	0x00000008	Power Mode Control
Configuration 2				
0x000050	R/W	32	0x00000000	PCI Master Base Address
0x000054	R	32	0x075000A0	Device Id
0x000058	R	32	0x00000000	PLL Clock Count
0x00005C	R/W	32	0x00020407	Primary Display PLL Control
0x000060	R/W	32	0x00020A1C	Secondary Display PLL Control
0x000064	R/W	32	0x00020407	VGA PLL 0 Control
0x000068	R/W	32	0x00020408	VGA PLL 1 Control
0x00006C	R/W	32	0x00000000	Scratch Data
0x000070	R/W	32	0x0002045C	MXCLK PLL Control

Table 8: SM750 System Configuration Register Summary

3.2.1 Configuration 1 Register Descriptions

System Control

Read/Write MMIO_base + 0x000000

Power-on Default 0x00A00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPMS R/W		Res						2DF	2D	2DMF	CSC	CRT	P	Buf	DMA
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res		Abort R/W	Res				BE	Res				CT R/W	EMT R/W	MT R/W	PT R/W

Bit(s)	Name	Description
31:30	DPMS	31:30 Vertical Sync Horizontal Sync 00 Pulsing Pulsing 01 Pulsing Not pulsing 10 Not pulsing Pulsing 11 Not pulsing Not pulsing
29:24	Res	These bits are reserved.
23	2DF	2D Engine FIFO Empty. (Read Only) 0: FIFO not empty. 1: FIFO empty.
22	2D	2D Engine Status. (Read Only) 0: Idle. 1: Busy.
21	2DMF	2D Engine Memory Interface FIFO Empty. (Read Only) 0: FIFO not empty. 1: FIFO empty.
20	CSC	Color Space Conversion Status. (Read Only) 0: Idle. 1: Busy.
19	CRT	CRT VSYNC. (Read Only) 0: Normal. 1: CRT VSYNC.
18	P	Panel VSYNC. (Read Only) 0: Normal. 1: Panel VSYNC.
17	Buf	Current Buffer. (Read Only) 0: Normal. 1: Flip pending.
16	DMA	DMA Status. (Read Only) 0: Idle. 1: Busy.
15:14	Res	These bits are reserved.
13	Abort	Drawing Engine Abort. 0: Normal. 1: Abort 2D engine.
12:9	Res	These bits are reserved.

Bit(s)	Name	Description
8	BE	BAR 2 to BAR 5 Enable. (The count starts with BAR0) 0: Disable BAR 2, 3, 4, and 5 of PCI Config Space. (Default) 1: Enable BAR 2, 3, 4, and 5 of PCI Config Space.
7:4	Res	These bits are reserved.
3	CT	CRT Interface 3-State. 0: Normal. 1: 3-state.
2	EMT	External Memory Interface 3-State. 0: Normal. 1: 3-state.
1	LMT	Local Memory Interface 3-State. 0: Normal. 1: 3-state.
0	PT	Panel Interface 3-State. 0: Normal. 1: 3-state.

Miscellaneous Control

Read/Write MMIO_base + 0x000004

Power-on Default 0x01006066

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				RC	RCtl		II R/W	PLL R/W	Res		DAC R/W	Res			Clk R
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ColSize R/W		Size R/W		tWTR	tWR	tRP	tRFC	tRAS	Rst R/W	RA R/W	CL R/W	DLL R/W	Low	Width R/W	E R/W

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	RC	Refresh Count. 0: Each refresh is 1 row. 1: Each refresh is 3 rows.
26:25	RCtl	Memory Refresh Control. 00: Refresh every 8x100xMemory Clock. 01: Refresh every 16x100xMemory Clock. 10: Refresh every 32x100xMemory Clock. 11: Refresh every 64x100xMemory Clock.
24	II	Interrupt Inverting. 0: Normal. 1: Inverted.
23	PLL	PLL Clock Count. (This bit is for testing purpose only) 0: Disable. 1: Enable.
22:21	Res	These bits are reserved.
20	DAC	DAC Power Control. 0: Enable. 1: Disable.
19:17	Res	These bits are reserved.
16	Clk	Clock Select. (Power-on configuration through strap pin MA9) 0: Crystal input. (default) 1: Test clock input.
15:14	ColSize	DRAM Column Size. (Power-on configuration through strap pins MA8 and MA7) 00: 256 words. 01: 512 words. 1x: 1024 words.
13:12	Size	DRAM Size. (Power-on configuration through strap pins MA6 and MA5) 00: 16MB 01: 32MB 10: 64MB 11: 8MB
11	tWTR	tWTR 0: 2 clocks. (default) 1: 1 clock.
10	tWR	tWR 0: 3 clocks. (default) 1: 2 clocks.
9	tRP	tRP 0: 3 clocks. (default) 1: 4 clocks.
8	tRFC	tRFC 0: 12 clocks. (default) 1: 14 clocks.
7	tRAS	tRAS 0: 7 clocks. (default) 1: 8 clocks.

Bit(s)	Name	Description
6	Rst	Local Memory Controller Reset. (Software can use this bit for debug when suspecting local memory problem) 0: Reset 1: Normal
5	RA	Local Memory Remain in Active State. (This bit can be used by software to tune performance for video memory) 0: Remain active. 1: Do not remain active.
4	CL	Memory CAS Latency. (Power-on configuration through strap pin MA4) 0: 2.5 clocks. 1: 3 clocks.
3	DLL	Delay Lock Loop Control. (Power-on configuration through strap pin MA3) 0: Enable. 1: Disable.
2	Low	DDR Low Driver Output. (Power-on configuration through strap pin MA2) 0: Enable 1: Disable
1	Width	Memory Bus Width. (Power-on configuration through strap pin MA1) 0: 32bit. 1: 64bit.
0	E	Embedded Memory Control. (Power-on configuration through strap pin MA0) (This bit is used to disable embedded local memory) 0: Enable. 1: Disable.

$GPIO_{31:0}$ Control

Read/Write MMIO_base + 0x000008

Power-on Default 0x01F00000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G_{31} R/W	G_{30} R/W	G_{29} R/W		G_{27} R/W		G_{25} R/W	G_{24} R/W		G_{22} R/W		G_{20} R/W	G_{19} R/W	G_{18} R/W	G_{17} R/W	G_{16} R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G_{15} R/W	G_{14} R/W	G_{13} R/W	G_{12} R/W	G_{11} R/W	G_{10} R/W	G_{9} R/W	G_{8} R/W	G_{7} R/W	G_{6} R/W	G_{5} R/W	G_{4} R/W	G_{3} R/W	G_{2} R/W	G_{1} R/W	G_{0} R/W

Bit(s)	Name	Description
31	G31	GPIO Pin 31 Control. 0: GPIO. 1: I^2C Data.
30	G30	GPIO Pin 30 Control. 0: GPIO. 1: I^2C Clock.
29	G29	GPIO Pin 29 Control. 0: GPIO. 1: SSP1 Clock Out.
28	G28	GPIO Pin 28 Control. 0: GPIO. 1: SSP1 Input. (Default)
27	G27	GPIO Pin 27 Control. 0: GPIO. 1: SSP1 Frame Out.
26	G26	GPIO Pin 26 Control. 0: GPIO. 1: SSP1 Input. (Default)
25	G25	GPIO Pin 25 Control. 0: GPIO. 1: SSP1 Transmit.
24	G24	GPIO Pin 24 Control. 0: GPIO. 1: SSP0 Clock Out.
23	G23	GPIO Pin 23 Control. 0: GPIO. 1: SSP0 Input. (Default)
22	G22	GPIO Pin 22 Control. 0: GPIO. 1: SSP0 Frame Out.
21	G21	GPIO Pin 21 Control. 0: GPIO. 1: SSP0 Input. (Default)
20	G20	GPIO Pin 20 Control. 0: GPIO. 1: SSP0 Transmit.
19	G19	GPIO Pin 19 Control. 0: GPIO. 1: PWM2.
18	G18	GPIO Pin 18 Control. 0: GPIO. 1: PWM1.

Bit(s)	Name	Description
17	G17	GPIO Pin 17 Control. 0: GPIO. 1: PWM0.
16	G16	GPIO Pin 16 Control. 0: GPIO or ZV-Port 1 Clock. 1: Test Data[xx].
15	G15	GPIO Pin 15 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
14	G14	GPIO Pin 14 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
13	G13	GPIO Pin 13 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
12	G12	GPIO Pin 12 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
11	G11	GPIO Pin 11 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
10	G10	GPIO Pin 10 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
9	G9	GPIO Pin 9 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
8	G8	GPIO Pin 8 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
7	G7	GPIO Pin 7 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
6	G6	GPIO Pin 6 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
5	G5	GPIO Pin 5 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
4	G4	GPIO Pin 4 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
3	G3	GPIO Pin 3 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
2	G2	GPIO Pin 2 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
1	G1	GPIO Pin 1 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].
0	G0	GPIO Pin 0 Control. 0: GPIO or ZV-Port[xx]. 1: Test Data[xx].

Local Memory Arbitration Control

Read/Write MMIO_base + 0x00000C

Power-on Default 0x01765324

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Int R/W	Res	VGA R/W			Res	DMA R/W			Res	ZVPort1 R/W		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	ZVPort0 R/W			Res	Video R/W			Res	Panel R/W			Res	CRT R/W		

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28	Int	Internal Memory Priority Scheme. 0: Fixed priority. 1: Revolving priority.
27	Res	This bit is reserved.
26:24	VGA	VGA FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
23	Res	This bit is reserved.
22:20	DMA	DMA FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
19	Res	This bit is reserved.
18:16	ZVPort1	ZV Port 1 FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
15	Res	This bit is reserved.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>14:12</td><td>ZVPort0</td><td>ZV Port 0 FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
<tr><td>11</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>10:8</td><td>Video</td><td>Video FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
<tr><td>7</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>6:4</td><td>Panel</td><td>Panel FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
<tr><td>3</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>2:0</td><td>CRT</td><td>CRT FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
</table>

PCI Bus Master Memory Arbitration Control

Read/Write MMIO_base + 0x000010

Power-on Default 0x01765324

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Ext R/W	Res	VGA R/W			Res	DMA R/W			Res	ZVPort1 R/W		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	ZVPort0 R/W			Res	Video R/W			Res	Panel R/W			Res	CRT R/W		

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28	Ext	External Memory Priority Scheme. 0: Fixed priority. 1: Revolving priority.
27	Res	This bit is reserved.
26:24	VGA	VGA FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
23	Res	This bit is reserved.
22:20	DMA	DMA FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
19	Res	This bit is reserved.
18:16	ZVPort1	ZV Port1 FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
15	Res	This bit is reserved.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>14:12</td><td>ZVPort0</td><td>ZV Port0 FIFO Priority.<table><tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr><tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr><tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr><tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr></table></td></tr>
<tr><td>11</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>10:8</td><td>Video</td><td>Video FIFO Priority.<table><tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr><tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr><tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr><tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr></table></td></tr>
<tr><td>7</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>6:4</td><td>Panel</td><td>Panel FIFO Priority.<table><tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr><tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr><tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr><tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr></table></td></tr>
<tr><td>3</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>2:0</td><td>CRT</td><td>CRT FIFO Priority.<table><tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr><tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr><tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr><tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr></table></td></tr>
</table>

Arbitration Control

Read/Write MMIO_base + 0x000014

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Int R/W	Res					Panel R/W			Res	ZVPort R/W		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	Command R/W			Res	DMA R/W			Res	Video R/W			Res	CRT R/W		

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28	Int	Internal Memory Priority Scheme. 0: Fixed priority. 1: Revolving priority.
27:23	Res	These bits are reserved.
22:20	Panel	Panel FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
19	Res	This bit is reserved.
18:16	ZVPort	ZV Port FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
15	Res	This bit is reserved.
14:12	Command	Command List Interpreter FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
11	Res	This bit is reserved.
10:8	DMA	DMA FIFO Priority. 000 Off; 001 Priority 1 (highest).; 010 Priority 2.; 011 Priority 3.; 100 Priority 4.; 101 Priority 5.; 110 Priority 6.; 111 Priority 7 (lowest).
7	Res	This bit is reserved.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>6:4</td><td>Video</td><td>Video FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
<tr><td>3</td><td>Res</td><td>This bit is reserved.</td></tr>
<tr><td>2:0</td><td>CRT</td><td>CRT FIFO Priority.
<table>
<tr><td>000</td><td>Off</td><td>100</td><td>Priority 4.</td></tr>
<tr><td>001</td><td>Priority 1 (highest).</td><td>101</td><td>Priority 5.</td></tr>
<tr><td>010</td><td>Priority 2.</td><td>110</td><td>Priority 6.</td></tr>
<tr><td>011</td><td>Priority 3.</td><td>111</td><td>Priority 7 (lowest).</td></tr>
</table></td></tr>
</table>

Raw Interrupt Status

Read MMIO_base + 0x000020

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											ZV1 R	ZV0 R	CV R	PV R	VV R

Bit(s)	Name	Description
31:5	Res	These bits are reserved.
4	ZV1	ZV Port 1 VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
3	ZV0	ZV Port 0 VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
2	CV	CRT VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
1	PV	Panel VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
0	VV	VGA VSYNC Interrupt Status. 0: Interrupt not active. 1: Interrupt active.

Raw Interrupt Clear

Write MMIO_base + 0x000020

Power-on Default 0x0000000

Interrupt bit should be clear by software when the interrupt has been serviced. Writing a zero has no effect. This register can be used to clear interrupts from VGA, Panel, CRT, ZV0, and ZV1. Other features (DMA, for example) have interrupt clear bits in their own functional registers sets.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											ZV1 W	ZV0 W	CV W	PV W	VV W

Bit(s)	Name	Description
31:5	Res	These bits are reserved.
4	ZV1	ZV Port 1 VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.
3	ZV0	ZV Port 0 VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.
2	CV	CRT VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.
1	PV	Panel VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.
0	VV	VGA VSYNC Interrupt Status. 0: No action. 1: Clear interrupt.

Interrupt Status

Read MMIO_base + 0x000024

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G_{31} R	G_{30} R	G_{29} R	G_{28} R	G_{27} R	G_{26} R	G_{25} R	Res								
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res			I^2C R	PW R	Res	DMA1 R	Res R	S1 R	S0 R	2D R	ZV1 R	ZV0 R	CV R	PV R	VV R

Bit(s)	Name	Description
31	G31	GPIO Pin 31 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
30	G30	GPIO Pin 30 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
29	G29	GPIO Pin 29 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
28	G28	GPIO Pin 28 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
27	G27	GPIO Pin 27 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
26	G26	GPIO Pin 26 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
25	G25	GPIO Pin 25 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
24:13	Res	These bits are reserved.
12	I^2C	I^2C Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
11	PW	PWM Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
10	Res	This bit is reserved.
9	DMA1	DMA 1 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
8	Res	This bit is reserved.
7	S1	SSP1 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
6	S0	SSP0 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
5	2D	2D Engine Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
4	ZV1	ZV-Port 1 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
3	ZV0	ZV-Port 0 Interrupt Status. 0: Interrupt not active. 1: Interrupt active.

Bit(s)	Name	Description
2	CV	CRT Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
1	PV	Panel Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.
0	VV	VGA Vertical Sync Interrupt Status. 0: Interrupt not active. 1: Interrupt active.

Interrupt Mask

Read MMIO_base + 0x000028

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
G31 R/W	G30 R/W	G29 R/W	G28 R/W	G27 R/W	G26 R/W	G25 R/W	Res								
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res			I^2C R/W	PW R/W	Res	DMA1 R/W	PCI R/W	S1 R/W	S0 R/W	2D R/W	ZV1 R/W	ZV0 R/W	CV R/W	PV R/W	VV R/W

Bit(s)	Name	Description
31	G^{31}	GPIO Pin 31 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
30	G30	GPIO Pin 30 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
29	G29	GPIO Pin 29 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
28	G28	GPIO Pin 28 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
27	G27	GPIO Pin 27 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
26	G26	GPIO Pin 26 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
25	G25	GPIO Pin 25 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
24:13	Res	These bits are reserved.
12	I^2C	I^2C Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
11	PW	PWM Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
10	Res	This bit is reserved.
9	DMA1	DMA 1 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
8	PCI	PCI Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
7	S1	SSP1 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
6	S0	SSP0 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
5	2D	2D Engine Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
4	ZV1	ZV-Port 1 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.

Bit(s)	Name	Description
3	ZV0	ZV-Port 0 Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
2	CV	CRT Vertical Sync Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
1	PV	Panel Vertical Sync Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.
0	VV	VGA Vertical Sync Interrupt Mask. 0: Interrupt disabled. 1: Interrupt enabled.

Debug Control

Read/Write MMIO_base + 0x00002C

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								Module R/W			Partition R/W				

Bit(s)	Name	Description
31:8	Res	These bits are reserved.
7:5	Module	Module Select for Partition.
4:0	Partition	Partition select for Debugging Test Mode. 00000: PCI controller 00001: External memory controller 00010: HIF controller 00100: Display controller 00101: ZV-Port 0 00110: 2D Engine 01000: Internal memory interface 01011: ZV-Port 1 01100: SSP0 01101: SSP1 10101: I^2C 11010: Internal memory controller 11011: DMA 11100: Simulation test mode 11110: VGA 0 11111: VGA 1

3.2.2 Power Management Register Descriptions

Current Clock Status

Read MMIO_base + 0x000040

Power-on Default 0x00005FC6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MR		M2R		Res	VR	PR	I^2CR	SR	GR	ZR	CR	2DR	DR	MR	DMAR

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:14	M	MCLK Select. (Master clock select, the frequencies are derived from input crystal value of 14.31818 MHz) 00: Divided by 3. 01: Divided by 4. (default) 10: Divided by 6. 11: Divided by 8.
13:12	M2	M2XCLK Select. (Memory clock select, the frequencies are derived from input crystal value of 14.3181 MHz) 00: Divided by 1. 01: Divided by 2. (default) 10: Divided by 3. 11: Divided by 4.
11	Res	This bit is reserved.
10	V	VGA Clock Control. 0: Disable. 1: Enable.
9	P	PWM Clock Control. 0: Disable. 1: Enable.
8	I^2C	I^2C Clock Control. 0: Disable. 1: Enable.
7	S	SSP Clock Control. 0: Disable. 1: Enable.
6	G	GPIO Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Local Memory Controller Clock Control. 0: Disable. 1: Enable.
0	DMA	DMA Clock Control. 0: Disable. 1: Enable.

Power Mode 0 Clock Control

Read/Write MMIO_base + 0x000044

Power-on Default 0x00005FC6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M R/W		M2 R/W		Res	V R/W	P R/W	I^2C R/W	S R/W	G R/W	Z R/W	C R/W	2D R/W	D R/W	M R/W	DMA R/W

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:14	M	MCLK Select. 00: Divided by 3. 01: Divided by 4. (default) 10: Divided by 6. 11: Divided by 8.
13:12	M2	M2XCLK Select. 00: Divided by 1. 01: Divided by 2. (default) 10: Divided by 3. 11: Divided by 4.
11	Res	This bit is reserved.
10	V	VGA Clock Control. 0: Disable. 1: Enable.
9	P	PWM Clock Control. 0: Disable. 1: Enable.
8	I^2C	I^2C Clock Control. 0: Disable. 1: Enable.
7	S	SSP Clock Control. 0: Disable. 1: Enable.
6	G	GPIO Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Local Memory Controller Clock Control. 0: Disable. 1: Enable.
0	DMA	DMA Clock Control. 0: Disable. 1: Enable.

Power Mode 1 Clock Control

Read/Write MMIO_base + 0x000048

Power-on Default 0x00005FC6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M R/W		M2 R/W		Res	V R/W	P R/W	I^2C R/W	S R/W	G R/W	Z R/W	C R/W	2D R/W	D R/W	M R/W	DMA R/W

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:14	M	MCLK Select. 00: Divided by 3. 01: Divided by 4. (default) 10: Divided by 6. 11: Divided by 8.
13:12	M2	M2XCLK Select. 00: Divided by 1. 01: Divided by 2. (default) 10: Divided by 3. 11: Divided by 4.
11	Res	This bit is reserved.
10	V	VGA Clock Control. 0: Disable. 1: Enable.
9	P	PWM Clock Control. 0: Disable. 1: Enable.
8	I^2C	I^2C Clock Control. 0: Disable. 1: Enable.
7	S	SSP Clock Control. 0: Disable. 1: Enable.
6	G	GPIO Clock Control. 0: Disable. 1: Enable.
5	Z	ZV Port Clock Control. 0: Disable. 1: Enable.
4	C	Color Space Conversion Clock Control. 0: Disable. 1: Enable.
3	2D	2D Engine Clock Control. 0: Disable. 1: Enable.
2	D	Display Controller Clock Control. 0: Disable. 1: Enable.
1	M	Local Memory Controller Clock Control. 0: Disable. 1: Enable.
0	DMA	DMA Clock Control. 0: Disable. 1: Enable.

Power Mode Control

Read/Write MMIO_base + 0x00004C

Power-on Default 0x00000008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res												O R/W	A R/W	Mode R/W	

Bit(s)	Name	Description
31:4	Res	These bits are reserved.
3	O	Oscillator Input Control. (Enable or disable crystal input) 0: Disable. 1: Enable. (default)
2	A	ACPI Select. 0: Disable. (Power management according to SMI power mode) 1: Enable.
1:0	Mode	Power Mode Select. 00: Power Mode 0. 01: Power Mode 1. 1x: Sleep Mode.

3.2.3 Configuration 2 Register Descriptions

PCI Master Base Address

Read/Write MMIO_base + 0x000050

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Base55:32 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Base55:32 R/W								Base30:23 R/W							

Bit(s)	Name	Description
31:8	Base55:32	Base Address Bits [55:32] for 64-bit addressing.
7:0	Base30:23	Base Address Bits [30:23] for 32-bit addressing. This is added to bit 23 to 25 of bus master address to generate bit 23 to 31 for system address.

Device Id

Read MMIO_base + 0x000054

Power-on Default 0x075000A0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DeviceId R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								RevisionId R							

Bit(s)	Name	Description
31:16	DeviceId	Device Identification: 0x0750.
15:8	Res	These bits are reserved.
7:0	RevisionId	Revision Identification: 0xA0.

PLL Clock Count

Read MMIO_base + 0x000058

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ClockCount R															

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:0	ClockCount	Number of clocks since enabling. These clock counts verify if there is a PLL function. (This is for testing purpose only)

Primary Display Control

Read/Write MMIO_base + 0x00005C

Power-on Default 0x00020407

Controlled by Configuration Register (0x3D4, index 88) bit 2 exclusively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													By R/W	PD R/W	CS R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POD R/W		OD R/W		N R				M R							

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	POD	PLL Post Divider. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

Secondary Display Control

Read/Write MMIO_base + 0x000060

Power-on Default 0x00020A1C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													By R/W	PD R/W	CS R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POD R/W		OD R/W		N R				M R							

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	POD	PLL Post Divider. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

VGA PLL 0 Control

Read/Write MMIO_base + 0x000064

Power-on Default 0x00020407

Controlled by Standard VGA Register 3C2[2] exclusively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													By R/W	PD R/W	CS R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POD R/W		OD R/W		N R				M R							

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	POD	PLL Post Divider. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

VGA PLL 1 Control

Read/Write MMIO_base + 0x000068

Power-on Default 0x00020408

Controlled by Standard VGA Register 3C2[2] exclusively.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													By R/W	PD R/W	CS R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
POD R/W		OD R/W		N R				M R							

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	POD	PLL Post Divider. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

PLL Notes:

- All PLLs are defaulted to power on after RESET. Software can turn off any PLL not in use for power saving purpose.
- PLL output frequency = 14.31818 MHz x M / N (2^OD)

MXCLK PLL Control

Read/Write MMIO_base + 0x000070

Power-on Default 0x0002045C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													By R/W	PD R/W	OD R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res		OD R/W		N R				M R							

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	By	PLL Bypass. 0: No bypass. (default) 1: Bypass.
17	PD	PLL Power Down. 0: Power Down. 1: Power On.
16	CS	PLL Clock Select. 0: Crystal input. (default) 1: Test clock input.
15:14	Res	These bits are reserved.
13:12	OD	PLL OD. 00: Divided by 1. 01: Divided by 2. 10: Divided by 4. 11: Divided by 8.
11:8	N	PLL N Value.
7:0	M	PLL M Value.

Scratch Data

Read/Write MMIO_base + 0x00006C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data R/W															

Bit(s)	Name	Description
31:0	Data	Scratch Data.

4. PCI Configuration Space

4.1 Register Descriptions

The PCI specification defines the configuration space for auto-configuration (plug-and-play), and device and memory relocation.

Table 8 summarizes the PCI Configuration Space Registers.

Address	Type	Width	Reset Value	Register Name
0x00	R	32	0x0750126F	CSR00: Vendor ID and Device ID
0x04	R/W	32	0x02300000	CSR04: Command and Status
0x08	R	32	0x380000C0	CSR08: Revision ID and Class Code
0x0D	R	8	0x00	CSR0C: Latency Timer
0x10	R/W	32	0x00000000	CSR10: Linear Frame Buffer Base Address Register
0x14	R/W	32	0x00000000	CSR14: Base Address Register for Memory Map Address
0x18	R/W	32	0x00000000	CSR18: 64K VGA 0xA0000/0xB0000 Base Address
0x1C	R/W	32	0x00000000	CSR1C: 32K VGA 0xB8000 Base Address
0x20	R/W	32	0x00000000	CSR20: VGA I/O Ports 0x3Cx Base Address
0x24	R/W	32	0x00000000	CSR24: VGA I/O Ports 0x3Dx/0x3Bx Base Address
0x2C	R	32	0x00000000	CSR2C: Subsystem ID and Subsystem Vendor ID
0x30	R/W	32	0x00000000	CSR30: Expansion ROM Base Address
0x34	R	32	0x00000040	CSR34: Power Down Capability Pointer
0x3C	R/W	32	0x00000000	CSR3C: Interrupt Pin and Interrupt Line
0x40	R	32	0x06010001	CSR40: Power Down Capability Register
0x44	R/W	32	0x00000000	CSR44: Power Down Capability Data

Table 9: PCI Configuration Space Register Summary

Figure 13 lists the registers available in the PCI Configuration register space.

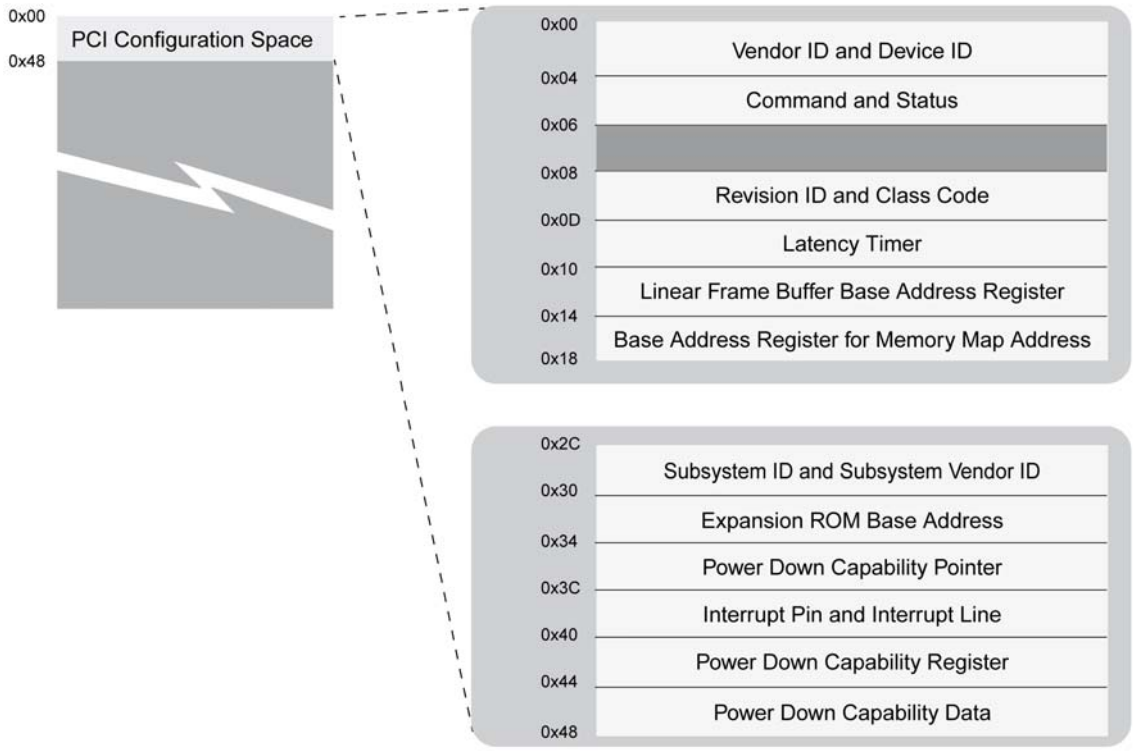


Figure 12: PCI Configuration Register Space

CSR00: Vendor ID and Device ID

Read Address 0x00

Power-on Default 0x0750126F

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device ID R															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Vendor ID R															

This register specifies the device and vendor IDs.

Bit(s)	Name	Description
31:16	Device ID	These bits are hardwired to 0x0750 to identify the SM750 device.
15:0	Vendor ID	These bits are hardwired to 0x126F to identify the vendor as Silicon Motion®, Inc.

CSR04: Command and Status

Read/Write Address 0x04

Power-on Default 0x02300000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DPE R	SSE R	RMA R	RTA R	STA R	DEVSEL R		MDPE R	FBB R	Res	66C R	NCD R	INT R	Res		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res					IAD R	FBBC R	SERR R	IDSEL R	PER R	VPS R/W	MWR R/W	SCE R	PBM R/W	MS R/W	IO R

This register controls which types of PCI command cycles are supported by the SM750.

Notes: Reserved bits are read only.

Bit(s)	Name	Description
31	DPE	Detected Parity Error. 0: Normal. 1: Error detected.
30	SSE	Signaled System Error. 0: Normal. 1: Error detected.
29	RMA	Received Master Abort. 0: Normal. 1: Aborted.
28	RTA	Received Target Abort. 0: Normal. 1: Aborted.
27	STA	Signaled Target Abort. 0: Normal. 1: Aborted.
26:25	DEVSEL	DEVSEL Timing. Not applicable for PCI Express. Hardwired to 0.
24	MDPE	Master Data Parity Error. 0: Normal. 1: Error detected.
23	FBB	Fast Back-to-Back Capable. Not applicable for PCI Express. Hardwired to 0.
22	Res	This bit is reserved.
21	66C	66 MHz Capable.
20	NCD	New Capability Definition.
19	INT	INTx Status.
18:11	Res	These bits are reserved.
10	IAD	INTx Assertion Disable.
9	FBBC	Fast Back-to-Back Enable. Not applicable for PCI Express. Hardwired to 0.
8	SERR	SERR# Enable.
7	IDSEL	IDSEL Stepping/Wait Cycle Control. Not applicable for PCI Express. Hardwired to 0.
6	PER	Parity Error Response.

Bit(s)	Name	Description
5	VPS	VGA Palette Snoop. Not applicable for PCI Express. Hardwired to 0.
4	MWR	Memory Write and Invalidate. Not applicable for PCI Express. Hardwired to 0.
3	SCE	Special Cycle Enable. Not applicable for PCI Express. Hardwired to 0.
2	PBM	PCI Bus Master Enable.
1	MS	Memory Space Access Enable. 0: Disable. 1: Enable.
0	IO	I/O Space Access Enable. 0: Disable.

CSR08: Revision ID and Class Code

Read Address 0x08

Power-on Default 0x038000A0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Base Class Code R								Subclass Code R							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Level Programming Interface R								Revision ID R							

This register specifies the silicon revision ID and the Class Code that the silicon supports.

Bit(s)	Name	Description
31:24	Base	Class Code 0x03 = For Video Controller
23:16	Subclass	Code 0x00 = Bootable Device
15:8	Register	Level Programming Interface 0x00 = Hardwired setting
7:0	Revision ID	0xA0 = Hardware Revision

CSR0C: Latency Timer

Read Address 0x0D

Power-on Default 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LT R								Res							

This register specifies the latency timer that the SM750 supports for burst master mode.

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:8	LT	Latency Timer. The default for this field is 0x00.
7:0	Res	These bits are reserved.

CSR10: Linear Frame Buffer Base Address Register

Read/Write Address 0x10

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Linear Address Memory Base R/W/R											Linear Frame Buffer Base Address R				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Linear Frame Buffer Base Address R															MB R

This register specifies the PCI configuration space for address relocation.

Notes: Reserved bits are read only.

Bit(s)	Name	Description
31:21	Linear Address Memory Base Address	Memory segment allocated within 64 MB boundary. • If 2 MB: **Bits 26:21** = FBA (Read/Write) • If 4 MB: **Bits 26:22** = FBA (Read/Write) **Bit 21** = 0b • If 8 MB: **Bits 26:23** = FBA (Read/Write) **Bits 22:21** = 00b (Read Only) • If 16 MB: **Bits 26:24** = FBA (Read/Write) **Bits 23:21** = 000b (Read Only) • If 32 MB: **Bit 26** = FBA (Read/Write) **Bits 24:21** = 0000b (Read Only) • If 64 MB: **Bit 26** = FBA (Read/Write) **Bits 25:21** = 00000b (Read Only)
20:1	Linear Frame Buffer Base Address	The default for this read-only field is 0x000000.
0	MB	Memory Base Read. The default for this bit is 0.

CSR14: Base Address Register for Memory Map Address

Read/Write Address 0x14

Power-on Default 0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FBA R/W											ABA R				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ABA R															MB R

This register specifies the PCI configuration space for address relocation.

Notes: Reserved bits are read only.

Bit(s)	Name	Description
31:21	FBA	Memory Map Address Base Address. • If One Endian: **Bits [31:21]** = FBA (Read/Write) • If Big and Small Endian: **Bit [31:22]** = FBA (Read/Write) **Bit [21]** = 0b (Read Only)
20:1	ABA	Memory Map Address Base Address. The default for this read-only field is 0x000000.
0	MB	Memory Base. The default for this read-only bit is 0.

CSR18: 64K VGA 0xA0000/0xB0000 Base Address

Read/Write Address 0x18

Power-on Default0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
64K VGA BAR R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
64K VGA BAR R/W															

Bit(s)	Name	Description
31:0	64K VGA BAR	Memory segment allocated for 64K access of legacy VGA 0xA0000 or 0xB0000 memory area.

CSR1C: 32K VGA 0xB8000 Base Address

Read/Write Address 0x1C

Power-on Default0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
32K VGA BAR R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
32K VGA BAR R/W															

Bit(s)	Name	Description
31:0	32K VGA BAR	Memory segment allocated for 32K access of legacy VGA 0xB8000 memory area.

CSR20: VGA I/O Ports 0x3Cx Base Address

Read/Write Address 0x20

Power-on Default0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VGA 3Cx BAR R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VGA 3Cx BAR R/W															

Bit(s)	Name	Description
31:0	VGA 3Cx BAR	Memory segment allocated for 16 bytes access of legacy VGA I/O ports 0x3Cx memory area.

CSR24: VGA I/O Ports 0x3Dx/0x3Bx Base Address

Read/Write Address 0x24

Power-on Default0x0000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VGA 3D/Bx BAR R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VGA 3D/Bx BAR R/W															

Bit(s)	Name	Description
31:0	VGA 3D/Bx BAR	Memory segment allocated for 16 bytes access of legacy VGA I/O ports 0x3Dx or 0x3Bx memory area.

CSR2C: Subsystem ID and Subsystem Vendor ID

Read Address 0x2C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Subsystem ID R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Subsystem Vendor ID R/W															

This register specifies both the Subsystem device ID and the Subsystem Vendor ID.

Bit(s)	Name	Description
31:16	Subsystem ID	This System ID is written by the system BIOS during POST.
15:0	Subsystem Vendor ID	This field contains the Subsystem Vendor ID.

CSR30: Expansion ROM Base Address

Read/Write Address 0x30

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROM Base Address R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res															BIOS R/W

This register specifies the expansion ROM base address.

Notes: Reserved bits are read only.

Bit(s)	Name	Description
31:16	ROM Base Address	Memory segment allocated for BIOS ROM in 64KB boundary [15:0].
15:1	Res	These bits are reserved.
0	BIOS Address Decode Enable	This bit is valid only if memory space access is enabled (CSR04 bit 1 = 1). 0: Disable. 1: Enable.

CSR34: Power Down Capability Pointer

Read Address 0x34

Power-on Default 0x00000040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Power Down Capability Pointer															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Power Down Capability Pointer															

This register contains the address where PCI power down management registers are located.

Bit(s)	Name	Description
31:0	Power Down Capability Pointer	The Capability pointer contains the address where the PCI Power Down Management Register is located.

CSR3C: Interrupt Pin and Interrupt Line

Read/Write Address 0x3C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Interrupt Pin R								Interrupt Line R/W							

This register specifies the PCI interrupt pin and interrupt line.

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:8	Interrupt Pin	
7:0	Interrupt Line	

CSR40: Power Down Capability Register

Read Address 0x40

Power-on Default 0x06010001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCI Power Down Management Capability (0x0601)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
No More Extra Capability Pointer (0x00) R								PCI Power Down Management Capability (0x01) R							

This register contains the address for PCI power-down management capabilities.

Bit(s)	Name	Description
31:16	PCI Power Down Management Capability	Offset 2. This field is hardwired to 0x0601.
15:8	No More Extra Capability Pointer	This field is hardwired to 0x00.
7:0	PCI Power Down Management Capability ID	Offset 0. This field is hardwired to 0x01.

CSR44: Power Down Capability Data

Read/Write Address 0x44

Power-on Default 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Data R								Res							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCI Power Down Management Control/Status R/W														PDS R/W	

This register contains the address for PCI power-down management Control, Status and Data.

Bit(s)	Name	Description
31:24	Data	Offset 7. This data field is read-only.
23:16	Res	These bits are reserved.
15:2	PCI Power Down Management Control/Status	Offset 4.
1:0	PDS	Power Down Management Control and Status. 00: Power Down Management State D0. 01: Power Down Management State D1. 10: Power Down Management State D2. 11: Power Down Management State D3.

5. Drawing Engine

5.1 Functional Overview

The SM750's Drawing Engine is designed to accelerate Microsoft's DirectDraw and Direct3D applications. The engine contains a 3-operand ALU with 256 raster operations, source and destination FIFOs, as well as a host data FIFO. The drawing engine pipeline allows single cycle operations and runs at the memory clock speed.

The Drawing Engine includes several key functions to achieve the high GUI performance. The device supports color expansion with packed mono font, color pattern fill, host BLT, stretch BLT, short stroke, line draw, and others. Dedicated pathways are designed to transfer data between the host interface (HIF) bus and the Drawing Engine, and memory interface (MIF) bus and the Drawing Engine. In addition, the Drawing Engine supports rotation BIBLT for any block size, and automatic self activate rotation BLIT. This feature allows conversion between landscape and portrait display without the need for special software drivers.

5.2 Programmer's Model

The Drawing Engine supports various drawing functions, including Bresenham line draw, short stroke line draw, BITBLT, rectangle fill, HOSTBLT, Rotation Blit, and others. Hardware clipping is supported by 4 registers, DPR2C-DPR32, which define a rectangular clipping area.

The drawing engine supports two types of addressing formats for its source and destination locations. In XY addressing mode, the location is specified in X-Y coordinates, where the upper left corner of the screen is defined to be (0,0). In linear addressing mode, the location is specified based on its position in the display memory sequentially from the first pixel of the visible data. The addressing mode is set by the Addressing field of the 2D Stretch & Format register. The Command field of the 2D Control register selects other drawing functions, for example, Bresenham line draw, host write and short stroke.

5.3 Register Descriptions

All Drawing Engine control registers can be accessed via memory mapping. The address is at DP_Base + XXXh, where DP_Base is at PCI graphics base address + 4MB + 32K. Figure 14 shows how this 64kB region in the MMIO space is laid out. It controls the Drawing Engine registers.

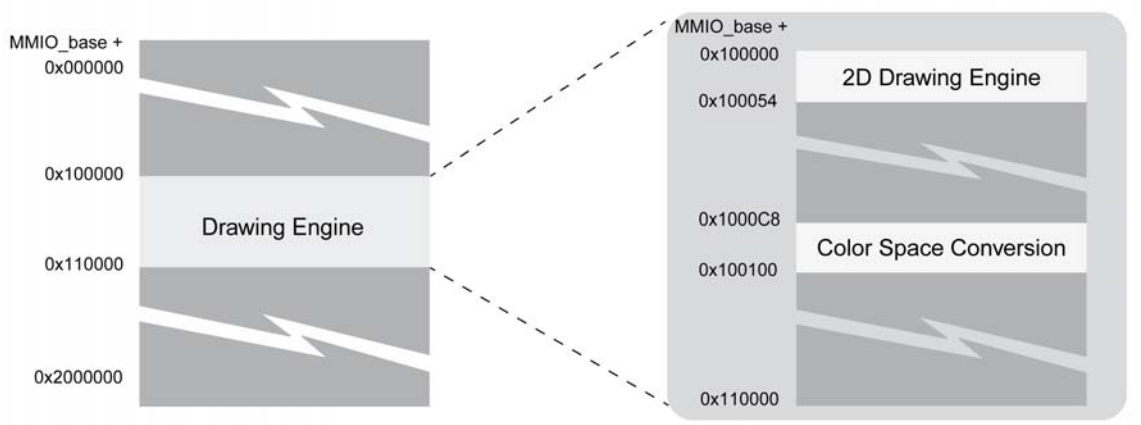


Figure 13: Bus Signal Level

Table 9 summarizes the Drawing Engine registers.

Offset from MMIO_base	Type	Width	Reset Value	Register Name
0x100000	R/W	32	0x00000000	2D Source
0x100004	R/W	32	0x00000000	2D Destination
0x100008	R/W	32	0x00000000	2D Dimension
0x10000C	R/W	32	0x00000000	2D Control
0x100010	R/W	32	0x00000000	2D Pitch
0x100014	R/W	32	0x00000000	2D Foreground
0x100018	R/W	32	0x00000000	2D Background
0x10001C	R/W	32	0x00000000	2D Stretch & Format
0x100020	R/W	32	0x00000000	2D Color Compare
0x100024	R/W	32	0x00000000	2D Color Compare Mask
0x100028	R/W	32	0x00000000	2D Mask
0x10002C	R/W	32	0x00000000	2D Clip TL
0x100030	R/W	32	0x00000000	2D Clip BR
0x100034	R/W	32	0x00000000	2D Mono Pattern Low
0x100038	R/W	32	0x00000000	2D Mono Pattern High
0x10003C	R/W	32	0x00000000	2D Window Width

Offset from MMIO_base	Type	Width	Reset Value	Register Name
0x100040	R/W	32	0x00000000	2D Source Base
0x100044	R/W	32	0x00000000	2D Destination Base
0x100048	R/W	32	0x00000000	2D Alpha
0x10004C	R/W	32	0x00000000	2D Wrap
0x100050	R/W	32	0x00000000	2D Status
0x1000C8	R/W	32	0x00000000	CSC Source Base
0x1000CC	R/W	32	0x00000000	CSC Constants
0x1000D0	R/W	32	0x00000000	CSC Source X
0x1000D4	R/W	32	0x00000000	CSC Source Y
0x1000D8	R/W	32	0x00000000	CSC U Source Base in YUV420
0x1000DC	R/W	32	0x00000000	CSC V Source Base in YUV420
0x1000E0	R/W	32	0x00000000	CSC Source Dimension
0x1000E4	R/W	32	0x00000000	CSC Source Pitch
0x1000E8	R/W	32	0x00000000	CSC Destination
0x1000EC	R/W	32	0x00000000	CSC Destination Dimension
0x1000F0	R/W	32	0x00000000	CSC Destination Pitch
0x1000F4	R/W	32	0x00000000	CSC Scale Factor
0x1000F8	R/W	32	0x00000000	CSC Destination Base
0x1000FC	R/W	32	0x00000000	CSC Control

Table 10: Drawing Engine Register Summary

5.3.1 2D Drawing Engine Registers

The 2D Drawing Engine register space is shown in Figure 15.

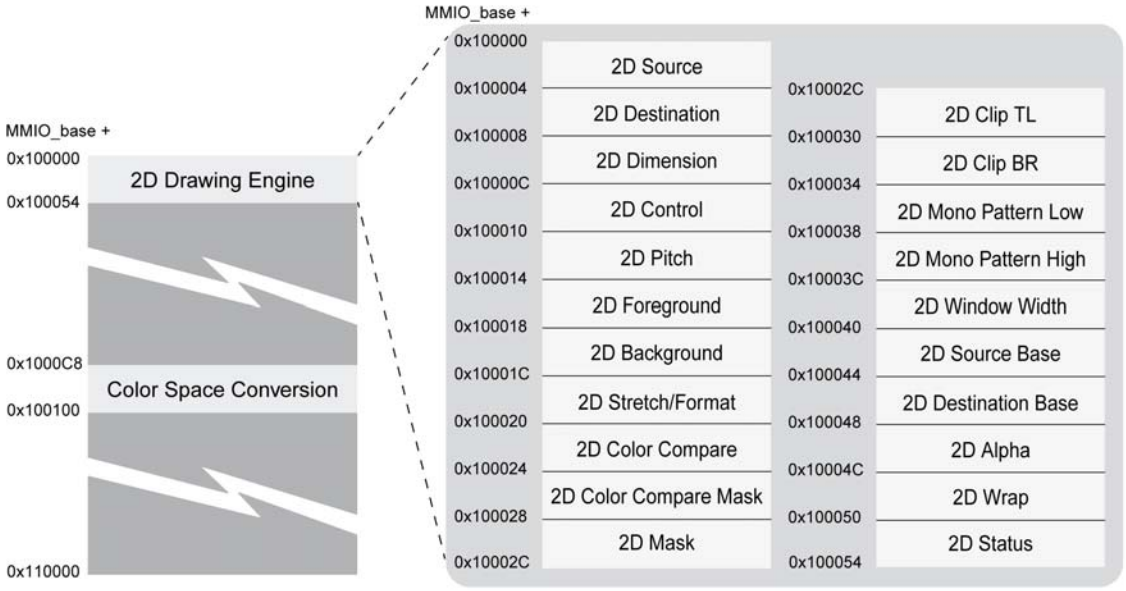


Figure 14: 2D Drawing Register Space

2D Source

Read/Write MMIO_base + 0x100000

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W R/W	Res	X_K1 R/W													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y_K2 R/W															

Bit(s)	Name	Description
31	W	Wrap Control. 0: Disable. 1: Enable.
30	Res	This bit is reserved.
29:16	X_K1	In XY addressing mode, the 12-bit X-coordinate of source (bits 27:16). In linear addressing mode, the lower 12-bits of the source address (bits 27:16). In host write mode, the 5-bit mono source for alignment (bits 20:16) In Bresenham line drawing mode, the 14-bit K1 constant for line drawing (bits 29:16): K1 = 2 * min(|dx|, |dy|).
15:0	Y_K2	In XY addressing mode, the 12-bit Y-coordinate of source (bits 11:0). In linear addressing mode, the higher 12-bits of the source address (bits 11:0). In host write mode, this field is not used. In Bresenham line drawing mode, the 14-bit K2 constant for line drawing (bits 13:0): K2 = 2 * (min(|dx|, |dy|) – max(|dx|, |dy|).

2D Destination

Read/Write MMIO_base + 0x100004

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W R/W	Res		X R/W												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y R/W															

Bit(s)	Name	Description
31	W	Wrap Control. 0: Disable. 1: Enable.
30:29	Res	These bits are reserved.
28:16	X	In XY addressing mode, the 12-bit X-coordinate of source (bits 27:16). In linear addressing mode, the lower 12-bits of the source address (bits 27:16). In Bresenham mode, the vector X start address (bits 27:16).
15:0	Y	In XY addressing mode, the 12-bit Y-coordinate of source (bits 11:0). In linear addressing mode, the higher 12-bits of the source address (bits 11:0). In Bresenham mode, the vector Y start address (bits 11:0)

2D Dimension

Read/Write MMIO_base + 0x100008

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			X_VL R/W												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y_ET R/W															

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28:16	X_VL	In XY addressing mode, the X dimension in pixels. In Bresenham mode, the vector length. In short stroke mode, horizontal length
15:0	Y_ET	In XY addressing mode, the Y dimension in pixels. In Bresenham mode, the vector error term given by: ET = 2 * min(|dx|, |dy|) – max(|dx|, |dy|) if start X > end X, or ET = 2 * min(|dx|, |dy|) – max(|dx|, |dy|) – 1 if start X <= end X. In short stroke mode, the non-horizontal length.

2D Control

Read/Write MMIO_base + 0x10000C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	P R/W	U R/W	Q R/W	D R/W	M R/W	X R/W	Y R/W	St R/W	H R/W	LP R/W	Command R/W				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R R/W	R2 R/W	Mono R/W		RR R/W	TM R/W	TS R/W	T R/W	ROP R/W							

Bit(s)	Name	Description
31	S	Drawing Engine Status. 0: Stop. 1: Start.
30	P	Pattern Select. 0: Monochrome. 1: Color.
29	U	Update Destination X after Operation Control. 0: Disable. 1: Enable.
28	Q	Quick Start Control. Quick start will start the drawing engine after the X field in the 2D Dimension register has been written to. 0: Disable. 1: Enable.
27	D	Direction Control for Operation. 0: Left to right. 1: Right to left.
26	M	Major Axis for Line Drawing. 0: X axis. 1: Y axis.
25	X	X Step Control for Line Drawing. 0: Positive. 1: Negative.
24	Y	Y Step Control for Line Drawing. 0: Positive. 1: Negative.
23	St	Stretch in Y Direction Control. 0: Disable. 1: Enable.
22	H	Host BitBlt Select. 0: Color. 1: Monochrome.
21	LP	Draw Last Pixel Control for Line Drawing. 0: Don't draw last pixel. 1: Draw last pixel.
20:16	Command	Command Code.

00000	BitBit	00111	Line Draw
00001	Rectangle Fill	01000	Host Write
00010	De-Tile	01001	Host Read
00011	Trapezoid Fill	01010	Host Write bottom-to-top
00100	Alpha Blend	01011	Rotate
00101	RLE Strip	01100	Font
00110	Short Stroke	01111	Texture Load

Bit(s)	Name	Description
15	R	ROP Control. 0: ROP3. 1: ROP2.
14	R2	ROP2 Control. 0: ROP2 source is bitmap. 1: ROP2 source is pattern.
13:12	Mono	Monochrome Data Pack Control. 00: Not packed. 01: Packed at 8-bit. 10: Packed at 16-bit.
11	RR	Repeat Rotation Control. Only valid when Command is 01011 (Rotate). When enabled, the drawing engine is started again at every vertical sync. 0: Disable. 1: Enable.
10	TM	Transparency Match Select. 0: Matching pixel is opaque. 1: Matching pixel is transparent.
9	TS	Transparency Select. 0: Transparency is controlled by source. 1: Transparency is controlled by destination.
8	T	Transparency Control. 0: Disabled. 1: Enabled.
7:0	ROP	ROP2 or ROP3 code (see tables below).

Binary Raster Operations (ROP2)

Each raster-operation code represents a Boolean operation in which the values of the pixels in the selected pen and the destination bitmap are combined. The operands used in these operations are:

- P = selected pen
- D = destination bitmap

		Bit[2:0]							
		0	1	2	3	4	5	6	7
Bit 3	0	0	~(D+S)	D*~S	~S	~D*S	~D	D^S	(~D*S)
	1	D*S	(~D^S)	D	D+~S	S	~D+S	D+S	1

Ternary Raster Operations (ROP3)

Each raster-operation code represents a Boolean operation in which the values of the pixels in the source, the selected brush, and the destination are combined.
The operands and operands are:

- D = destination bitmap
- P = selected brush (pattern)
- S = source bitmap
- a = bitwise AND
- n = bitwise NOT (inverse)
- o = bitwise OR
- x = bitwise XOR (exclusive OR)

All Boolean operations are presented in reverse Polish notation. For example, the following operation replaces the pixel values in the destination bitmap with a combination of the pixel values of the source and brush:

PSo = (P+S)

The following operation combines the values of the pixels in the source and brush with the pixel values of the destination bitmap (there are alternative spellings of the same function, so although a particular spelling may not be in the list, an equivalent form would be):

DPSoo = (P+S) + D

The SM750 supports all the 256 operations. However, the pattern must be monochrome.

Table 10 lists all the possible ROP3 operations.

bit [3:0]	Bits [7:4] 0	1	2	3	4	5	6	7
0	0	PDSona	DPSnaa	PSna	PSDnaa	PDna	PDSxa	PDSana
1	DPSoon	DSon	SDPxon	SDPnaon	DPSxon	DSPnaon	DSPDSaoxxn	SSDxPDxaxn
2	DPSona	SDPxnon	DSna	SDPSoox	SDxPDxa	DPSDaox	DSPDoax	SDPSxox
3	PSon	SDPaon	SPDnaon	Sn	SPDSanaxn	SPDSxaxn	SDPnox	SDPnoan
4	SDPona	DPSxnon	SPxDSxa	SPDSaox	SDna	DPSonon	SDPSoax	DSPDxox
5	DPon	DPSaon	PDSPanaxn	SPDSxnox	DPSnaon	Dn	DSPnox	DSPnoan
6	PDSxnon	PSDPSanaxx	SDPSaox	SDPox	DSPDaox	DPSox	DSx	SDPSnaox
7	PDSaon	SSPxDSxaxn	SDPSxnox	SDPoan	PSDPxaxn	DPSoan	SDPSonox	DSan
8	SDPnaa	SPxPDxa	DPSxa	PSDPoax	SDPxa	PDSPoax	DSPDSonoxxn	PDSax
9	PDSxon	SDPSanaxn	PSDPSaoxxn	SPDnox	PDSPDaoxxn	DPSnox	PDSxxn	DSPDSoaxxn
A	DPna	PDSPaox	DPSana	SPDSxox	DPSDoax	DPx	DPSax	DPSDnoax
B	PSDnaon	SDPSxaxn	SSPxPDxaxn	SPDnoan	PDSnox	DPSDonox	PSDPSoaxxn	SDPxnan
C	SPna	PSDPaox	SPDSoax	PSx	SDPana	DPSDxox	SDPax	SPDSnoax
D	PDSnaon	DSPDxaxn	PSDnox	SPDSonox	SSPxDSxoxn	DPSnoan	PDSPDoaxxn	DPSxnan
E	PDSonon	PDSox	PSDPxox	SPDSnaox	PDSPxox	DPSDnaox	SDPSnoax	SPxDSxo
F	Pn	PDSoan	PSDnoan	PSan	PDSnoan	DPan	PDSxnan	DPSaan

bit [3:0]	Bits [7:4] 8	9	A	B	C	D	E	F
0	DPSaa	PDSxna	DPa	PDSnoa	PSa	PSDnoa	PDSoa	P
1	SPxDSxon	SDPSnoaxn	PDSPnaoxn	PDSPxoxn	SPDSnaoxn	PSDPxoxn	PDSoxn	PDSono
2	DPSxna	DPSDPoaxx	DPSnoa	SSPxDSxox	SPDSonoxn	PDSnax	DSPDxax	PDSnao
3	SPDSnoaxn	SPDaxn	DPSDxoxn	SDPanan	PSxn	SPDSoaxn	PSDPaoxn	PSno
4	SDPxna	PSDPSoaxx	PDSPonoxn	PSDnax	SPDnoa	SSPxPDxax	SDPSxax	PSDnao
5	PDSPnoaxn	DPSaxn	PDxn	DPSDoaxn	SPDSxoxn	DPSanan	PDSPaoxn	PDno
6	DSPDSoaxx	DPSxx	DSPnax	DPSDPaoxx	SDPnax	PSDPSaoxx	SDPSanax	PDSxo
7	PDSaxn	PSDPSonoxx	PDSPoaxn	SDPxan	PSDPoaxn	DPSxan	SPxPDxan	PDSano
8	DSa	SDPSonoxn	DPSoa	PSDPxax	SDPoa	PDSPxax	SSPxDSxax	PDSao
9	SDPSnaoxn	DSxn	DPSoxn	DSPDaoxn	SPDoxn	SDPSaoxn	DSPDSanaxn	PDSxno
A	DSPnoa	DPSnax	D	DPSnao	DPSDxax	DPSDanax	DPSao	DPo
B	DSPDxoxn	SDPSoaxn	DPSono	DSno	SPDSaoxn	SPxDSxan	DPSxno	DPSnoo
C	SDPnoa	SPDnax	SPDSxax	SPDSanax	S	SPDnao	SDPao	PSo
D	SDPSxoxn	DSPDoaxn	DPSDaoxn	SDxPDxan	SDPono	SDno	SDPxno	PSDnoo
E	SSDxPDxax	DSPDSaoxx	DSPnao	DPSxo	SDPnao	SDPxo	DSo	DPSoo
F	PDSanan	PDSxan	DPno	DPSano	SPno	SDPano	SDPnoo	1

Table 11: ROP3 Operations

Rotate Command

For the Rotate command, the X and Y bits determine the rotation angle. For the Short Stroke command, the D, M, X, and Y bits determine the direction of the vector.

X	Y	Rotation Direction
0	0	0 degrees
0	1	270 degrees
1	0	90 degrees
1	1	180 degrees

D	M	X	Y	Vector Direction
0	0	0	0	225 degrees
0	0	0	1	135 degrees
0	0	1	0	315 degrees
0	0	1	1	45 degrees
0	1	0	0	270 degrees
0	1	0	1	90 degrees
1	0	0	0	180 degrees
1	0	1	0	0 degrees

2D Pitch

Read/Write MMIO_base + 0x100010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Destination R/W												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			Source R/W												

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28:16	Destination	Pitch of destination specified in pixels.
15:13	Res	These bits are reserved.
12:0	Source	Pitch of source specified in pixels.

2D Foreground

Read/Write MMIO_base + 0x100014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Foreground R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Foreground R/W															

Bit(s)	Name	Description	
31:0	Foreground	Bits Per Pixel	Foreground Color
		8	Index color.
		16	RGB565 color
		32	RGBx888 color.

2D Background

Read/Write MMIO_base + 0x100018

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Background R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Background R/W															

Bit(s)	Name	Description	
31:0	Background	Bits Per Pixel	Background Color
		8	Index color.
		16	RGB565 color
		32	RGBx888 color.

In monochrome transparency, the Background must be programmed with the invert of the Foreground pixels in the 2D Foreground register.

2D Stretch & Format

Read/Write MMIO_base + 0x10001C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	XY R/W	Y R/W			Res	X R/W			Res	Format R/W		Addressing R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res				Height R/W											

Bit(s)	Name	Description
31	Res	This bit is reserved.
30	XY	Pattern XY Select. 0: Only use X and Y fields in linear mode. 1: Use X and Y fields in XY mode.
29:27	Y	Pattern Y Origin. This field is only valid in linear mode (Addressing = 1111) or when XY is enabled.
26	Res	This bit is reserved.
25:23	X	Pattern X Origin. This field is only valid in linear mode (Addressing = 1111) or when XY is enabled.
22	Res	This bit is reserved.
21:20	Format	Pixel Format. 00: 8-bits per pixel. 01: 16-bits per pixel. 10: 32-bits per pixel.
19:16	Addressing	Addressing Mode. 0000: XY mode. 1111: Linear mode.
15:12	Res	These bits are reserved.
11:0	Height	Source height when stretch is enabled.

2D Color Compare

Read/Write MMIO_base + 0x100020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								Color R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color R/W															

Bit(s)	Name	Description
31:24	Res	These bits are reserved.
23:0	Color	Bits Per Pixel: Color Compare 8: Index color. 16: RGB565 color 32: RGB888 color.

In monochrome transparency, the Color must be programmed with the same value as the Foreground pixels in the 2D Foreground register.

2D Color Compare Mask

Read/Write MMIO_base + 0x100024

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								Mask R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mask R/W															

Bit(s)	Name	Description
31:24	Res	These bits are reserved.
23:0	Mask	Mask Bits for Color Compare. 0: Color compare always matches. 1: Color compare only matches when bits are equal.

2D Mask

Read/Write MMIO_base + 0x100028

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit R/W															

Bit(s)	Name	Description
31:16	Byte	Byte mask for each of the 16 bytes on the 128-bit memory bus. 0: Disable write. 1: Enable write.
15:0	Bit	Bit mask for 8- and 16-bits per pixel modes. 0: Disable write. 1: Enable write.

2D Clip TL

Read/Write MMIO_base + 0x10002C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Top R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		E R/W	S R/W	Left R/W											

Bit(s)	Name	Description
31:16	Top	Top Coordinate of Clipping Rectangle.
15:14	Res	These bits are reserved.
13	E	Clipping Control. 0: Disable. 1: Enable.
12	S	Clipping Select Control. 0: Write outside clipping rectangle disabled. 1: Write inside clipping rectangle disabled.
11:0	Left	Left Coordinate of Clipping Rectangle.

2D Clip BR

Read/Write MMIO_base + 0x100030

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bottom R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			Right R/W												

Bit(s)	Name	Description
31:16	Bottom	Bottom Coordinate of Clipping Rectangle.
15:13	Res	These bits are reserved.
12:0	Right	Right Coordinate of Clipping Rectangle.

2D Mono Pattern Low

Read/Write MMIO_base + 0x100034

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Pattern R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern R/W															

Bit(s)	Name	Description
31:0	Pattern	Bits [31:0] of monochrome pattern.

2D Mono Pattern High

Read/Write MMIO_base + 0x100038

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Pattern R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern R/W															

Bit(s)	Name	Description
31:0	Pattern	Bits [63:32] of monochrome pattern.

2D Window Width

Read/Write MMIO_base + 0x10003C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Destination R/W												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			Source R/W												

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28:16	Destination	Width of destination window specified in pixels.
15:13	Res	These bits are reserved.
12:0	Source	Width of source window specified in pixels.

2D Source Base

Read/Write MMIO_base + 0x100040

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of source window with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

2D Destination Base

Read/Write MMIO_base + 0x100044

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory address of destination window with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

2D Alpha

Read/Write MMIO_base + 0x100048

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res								Alpha R/W							

Bit(s)	Name	Description
31:8	Res	These bits are reserved.
7:0	Alpha	Alpha Value for Alpha Blend.

2D Wrap – Width and Height

Read/Write MMIO_base + 0x10004C

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Width R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Height R/W															

Bit(s)	Name	Description
31:16	Width	Horizontal pitch (H_Pitch) in pixels.
15:0	Height	Vertical pitch (V_Pitch) in lines.

2D Status

Read/Write MMIO_base + 0x100050

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res														CSC R/W	2D R/W

Bit(s)	Name	Description
31:2	Res	These bits are reserved.
1	CSC	Color Space Conversion Interrupt Status. Write a 0 into this field to clear the interrupt status. 0: CSC not active or job not done. 1: CSC interrupt.
0	2D	2D Engine Interrupt Status. Write a 0 into this field to clear the interrupt status. 0: 2D not active or job not done. 1: 2D interrupt.

5.3.2 Color Space Conversion Registers

The Color Space Conversion register space is shown in Figure 16.

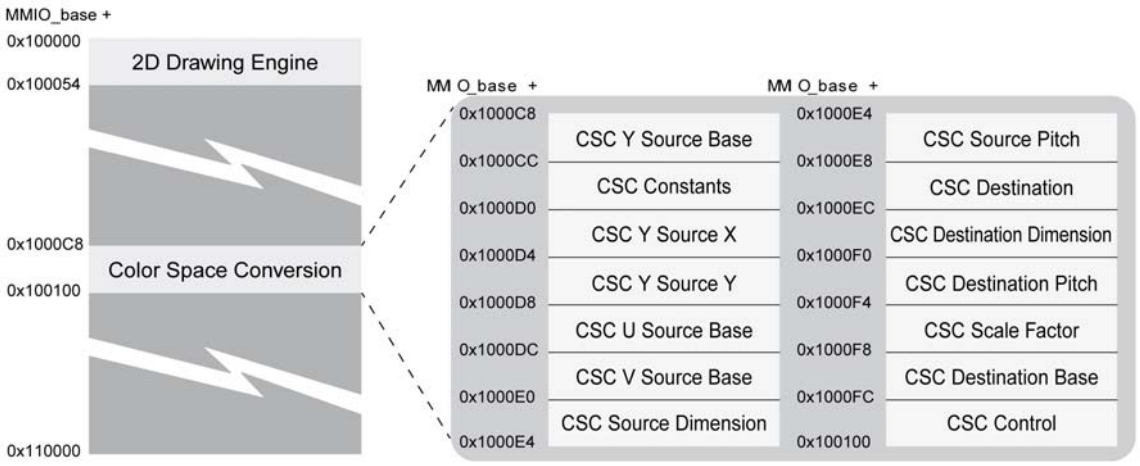


Figure 15: Color Space Conversion Register Space

CSC Source Base (Y Source Base in YUV420)

Read/Write MMIO_base + 0x1000C8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of Source Base with 128-bit Alignment. Memory Address of Y Source Base in YUV420 with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Constants

Read/Write MMIO_base + 0x1000CC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Conversion Constant (luminosity).
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	B Blue Conversion Constant.

CSC Source X

Read/Write MMIO_base + 0x1000D0

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				X_I R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X_F R/W												Res			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	X_I	Integer Part of Starting X-coordinate of Source.
15:3	X_F	Fractional Part of Starting X-coordinate of Source.
2:0	Res	These bits are reserved.

CSC Source Y

Read/Write MMIO_base + 0x1000D4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Y_I R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y_F R/W												Res			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	Y_I	Integer Part of Starting Y-coordinate of Source.
15:3	Y_F	Fractional Part of Starting Y-coordinate of Source.
2:0	Res	These bits are reserved.

CSC U Source Base in YUV420

Read/Write MMIO_base + 0x1000D8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of U Source Base in YUV420 with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC V Source Base in YUV420

Read/Write MMIO_base + 0x1000DC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	CS R/W	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Ext Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of V Source Base in YUV420 with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Source Dimension

Read/Write MMIO_base + 0x1000E0

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Width R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Height R/W															

Bit(s)	Name	Description
31:16	Width	Width of Source in Pixels.
15:0	Height	Height of Source in Lines.

CSC Source Pitch

Read/Write MMIO_base + 0x1000E4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UV R/W															

Bit(s)	Name	Description
31:16	Y	Pitch of Source specified in bytes ÷ 16. Pitch of Y Source in YUV420 specified in bytes ÷ 16.
15:0	UV	Pitch of U or V Source in YUV420 specified in bytes ÷ 16.

CSC Destination

Read/Write MMIO_base + 0x1000E8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W R/W	Res			X R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				Y R/W											

Bit(s)	Name	Description
31	W	Wrap Control. 0: Disable. 1: Enable.
30:28	Res	These bits are reserved.
27:16	X	X-coordinate of Destination.
15:12	Res	These bits are reserved.
11:0	Y	Y-coordinate of Destination.

CSC Destination Dimension

Read/Write MMIO_base + 0x1000EC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Width R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Height R/W															

Bit(s)	Name	Description
31:16	Width	Width of Destination in Pixels.
15:0	Height	Height of Destination in Lines.

CSC Destination Pitch

Read/Write MMIO_base + 0x1000F0

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
X R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y R/W															

Bit(s)	Name	Description
31:16	X	Horizontal Pitch of Destination specified in Bytes ÷ 16.
15:0	Y	Vertical Pitch of Destination specified in Lines.

CSC Scale Factor

Read/Write MMIO_base + 0x1000F4

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
X R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y R/W															

Bit(s)	Name	Description
31:16	X	Horizontal scale factor specified in 3.13 format. Scale factor = 2^{13} * ($Width_S$ – 1) / ($Width_D$ – 1).
15:0	Y	Vertical scale factor specified in 3.13 format. Scale factor = 2^{13} * ($Height_S$ – 1) / ($Height_D$ – 1).

CSC Destination Base

Read/Write MMIO_base + 0x1000F8

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	CS R/W	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:4	Address	Memory Address of Destination Window with 128-bit Alignment.
3:0	0000	These bits are hardwired to zeros.

CSC Control

Read/Write MMIO_base + 0x1000FC

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	$Format_S$ R/W			$Format_D$ R/W		H R/W	V R/W	B R/W	Res						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res															

Bit(s)	Name	Description
31	S	Color Space Conversion Control. 0: Stop. 1: Start.
30:28	$Format_S$	Source Pixel Format. 000 YUV422 / 100 Reserved 001 Reserved / 101 Reserved 010 YUV420 / 110 RGB565 011 Reserved / 111 RGB888
27:26	$Format_D$	Destination Pixel Format. 00: RGB565. 01: RGBx888.
25	H	Horizontal Linear Filter Control. 0: Disable. 1: Enable.
24	V	Vertical Linear Filter Control. 0: Disable. 1: Enable.
23	B	Byte Order for YUV422. 0 YUYV 1 UYVY
22:0	Res	These bits are reserved.

6. Display Controller

6.1 Programmer's Model

The SM750 integrates a concurrent video processor to control LCD display. Some of the features are:

- Background graphic supports from 4-bit index color, 8-bit index color, 16-bit direct color, and 32-bit direct color.
  Background graphic can be programmed to pan to the left/right and to up/down automatically according to number of VSYNC.
- Support 1 independent video surface using hardware scaling for any size of video windows at any location of the screen display and using hardware YUV to RGB color space conversion.
- Support 1 Alpha blend surface at any location of the screen display. It can use as hardware cursor or popup icon or sub picture for the video. Data format is 4-bit alpha and 4-bit color.
- The LCD module manages data flow and generate timing to select LCD display. It provides support for 18-bit, 24-bit, 36-bit panels up to 1920x1440.

The Video Processor Control Registers specify the control registers for Video Processor. The Video Processor Control Registers can only be accessed through memory-mapping.

6.2 Register Descriptions

Table 11 summarizes the Display Controller registers.

Offset from MMIO_base	Type	Width	Reset Value[1]	Register Name
Primary Graphics Control				
0x080000	R/W	32	0x00010000	Primary Display Control
0x080004	R/W	32	Undefined	Primary Display Panning Control
0x080008	R/W	32	Undefined	Primary Display Color Key
0x08000C	R/W	32	Undefined	Primary Display FB Address
0x080010	R/W	32	Undefined	Primary Display FB Offset/Window Width
0x080014	R/W	32	Undefined	Primary Display FB Width
0x080018	R/W	32	Undefined	Primary Display FB Height
0x08001C	R/W	32	Undefined	Primary Display Plane TL Location
0x080020	R/W	32	Undefined	Primary Display Plane BR Location
0x080024	R/W	32	Undefined	Primary Display Horizontal Total
0x080028	R/W	32	Undefined	Primary Display Horizontal Sync
0x08002C	R/W	32	Undefined	Primary Display Vertical Total
0x080030	R/W	32	Undefined	Primary Display Vertical Sync
0x080034	R	32	0b0000.0000.0000.0000. 0000.0XXX.XXXX.XXXX	Primary Display Current Line
Video Control				
0x080040	R/W	32	0b0000.0000.0000.0001. X000.0000.0000.0000	Video Display Control
0x080044	R/W	32	Undefined	Video FB 0 Address
0x080048	R/W	32	Undefined	Video FB Width
0x08004C	R/W	32	Undefined	Video FB 0 Last Address
0x080050	R/W	32	Undefined	Video Plane TL Location
0x080054	R/W	32	Undefined	Video Plane BR Location
0x080058	R/W	32	0x00000000	Video Scale
0x08005C	R/W	32	0x00000000	Video Initial Scale
0x080060	R/W	32	0x00EDEDED	Video YUV Constants
0x080064	R/W	32	Undefined	Video FB 1 Address
0x080068	R/W	32	Undefined	Video FB 1 Last Address

Offset from MMIO_base	Type	Width	Reset Value[1]	Register Name
Video Alpha Control				
0x080080	R/W	32	0x00000000	Video Alpha Display Control
0x080084	R/W	32	Undefined	Video Alpha FB Address
0x080088	R/W	32	Undefined	Video Alpha FB Offset/Window Width
0x08008C	R/W	32	Undefined	Video Alpha FB Last Address
0x080090	R/W	32	Undefined	Video Alpha Plane TL Location
0x080094	R/W	32	Undefined	Video Alpha Plane BR Location
0x080098	R/W	32	0x00000000	Video Alpha Scale
0x08009C	R/W	32	0x00000000	Video Alpha Initial Scale
0x0800A0	R/W	32	Undefined	Video Alpha Chroma Key
0x0800A4 – 0x0800C0	R/W	32	Undefined	Video Alpha Color Lookup
Primary Display Cursor Control				
0x0800F0	R/W	32	Undefined	Primary Display HWC Address
0x0800F4	R/W	32	Undefined	Primary Display HWC Location
0x0800F8	R/W	32	Undefined	Primary Display HWC Color 1 & 2
0x0800FC	R/W	32	Undefined	Primary Display HWC Color 3
0x080100	R/W	32	0x00010000	Alpha Display Control
0x080104	R/W	32	Undefined	Alpha FB Address
0x080108	R/W	32	Undefined	Alpha FB Offset/Window Width
0x08010C	R/W	32	Undefined	Alpha Plane TL Location
0x080110	R/W	32	Undefined	Alpha Plane BR Location
0x080114	R/W	32	Undefined	Alpha Chroma Key
0x080118 – 0x080134	R/W	32	Undefined	Alpha Color Lookup
Secondary Graphics Control				
0x080200	R/W	32	0x00010000	Secondary Display Control
0x080204	R/W	32	Undefined	Secondary Display FB Address
0x080208	R/W	32	Undefined	Secondary Display FB Offset/Window Width
0x08020C	R/W	32	Undefined	Secondary Display Horizontal Total
0x080210	R/W	32	Undefined	Secondary Display Horizontal Sync
0x080214	R/W	32	Undefined	Secondary Display Vertical Total

Offset from MMIO_base	Type	Width	Reset Value[1]	Register Name
0x080218	R/W	32	Undefined	Secondary Display Vertical Sync
0x08021C	R/W	32	Undefined	Secondary Display Signature Analyzer
0x080220	R	32	0b0000.0000.0000.0000.0000.0XXX.XXXX.XXXX	Secondary Display Current Line
0x080224	R/W	32	0b0000.0000.XXXX.XXXX.XXXX.XXXX.XXXX.XXXX	Secondary Display Monitor Detect
Secondary Display Cursor Control				
0x080230	R/W	32	Undefined	Secondary Display HWC Address
0x080234	R/W	32	Undefined	Secondary Display HWC Location
0x080238	R/W	32	Undefined	Secondary Display HWC Color 1 & 2
0x08023C	R/W	32	Undefined	Secondary Display HWC Color 3
Palette RAM				
0x080400 – 0x0807FC	R/W	32	Undefined	Primary Display Palette RAM
0x080C00 – 0x080FFC	R/W	32	Undefined	Secondary Display Palette RAM

Table 12: Display Controller Register Summary

1.In the reset values, “X” indicates don’t care.

Figure 17 shows how this 64kB region in the MMIO space is laid out. It controls the backend of the display controller as shown in Figure 18.

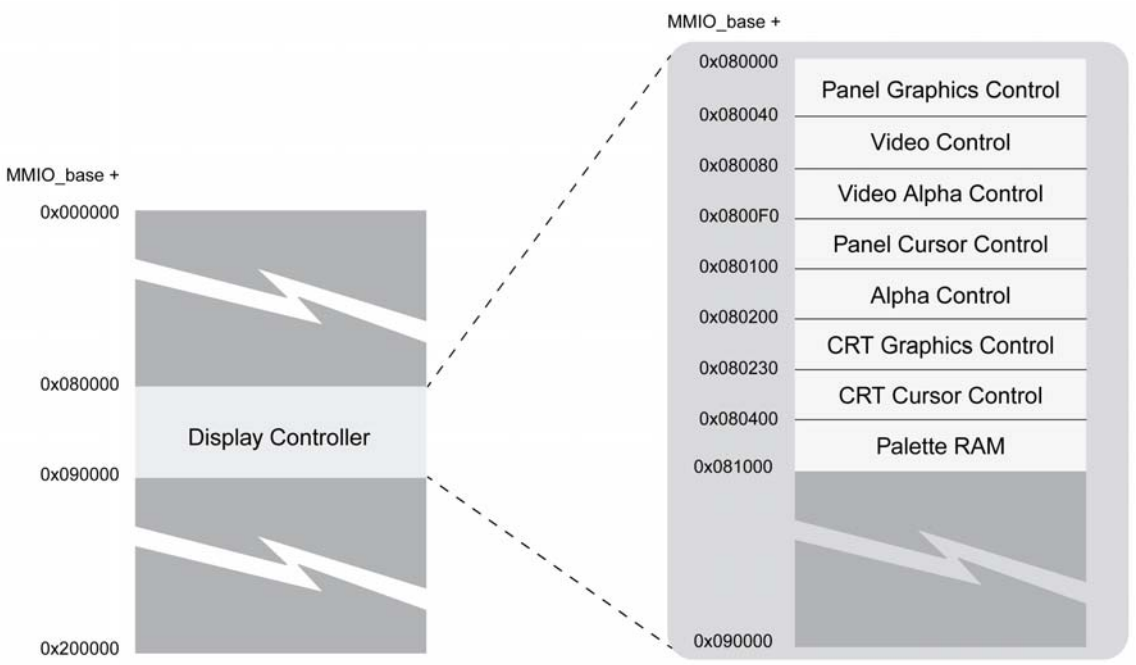


Figure 16: Display Controller Register Space

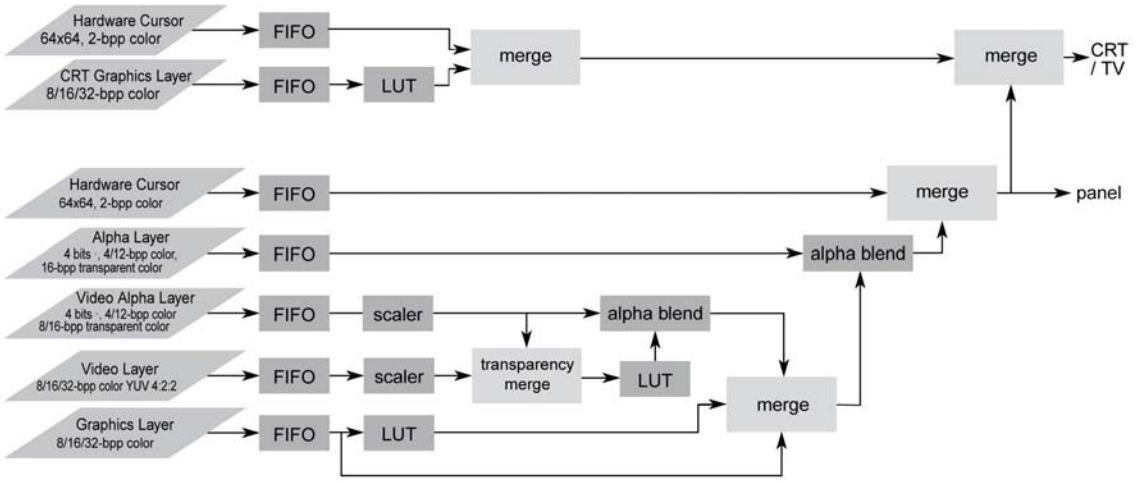


Figure 17: Video Layers

6.2.1 Primary Graphics Control Registers

Figure 19 shows the layout of the Primary Graphics Control registers.

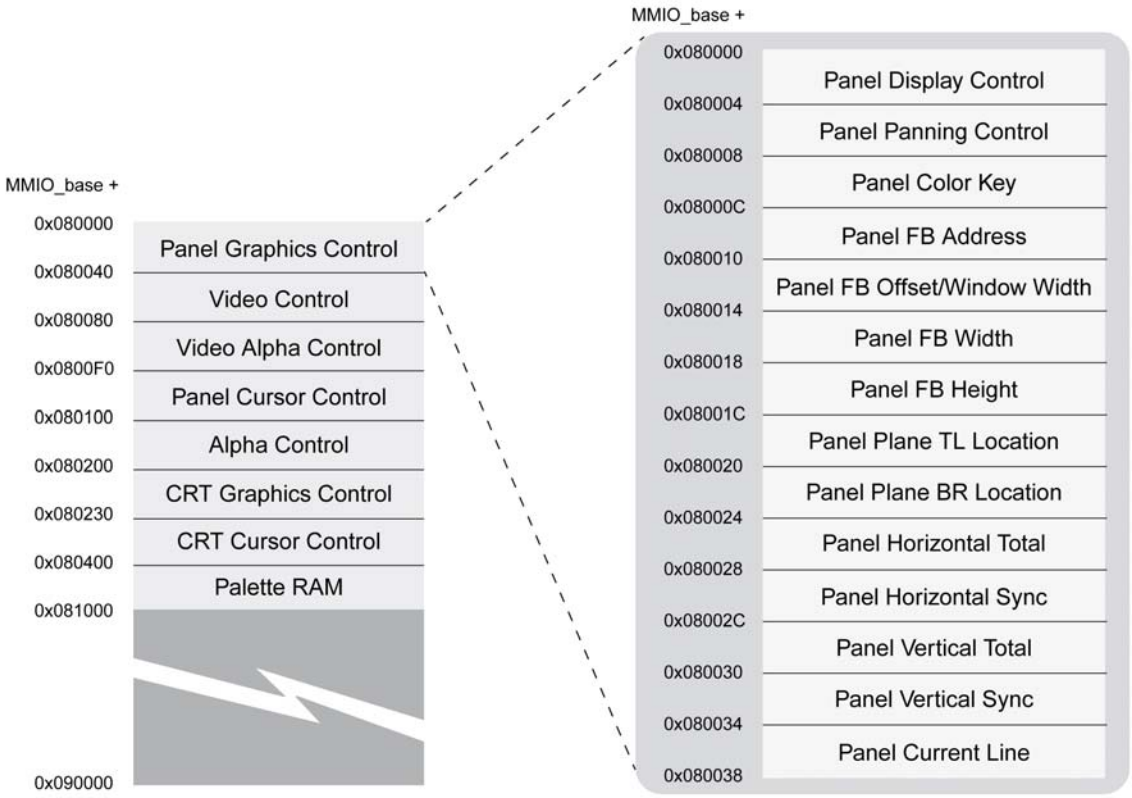


Figure 18: Primary Graphics Control Register Space

To understand video windowing, please refer to Figure 20. Here a window is created inside a much large frame buffer. That window is then being displayed on the panel as the Primary Graphics Plane.

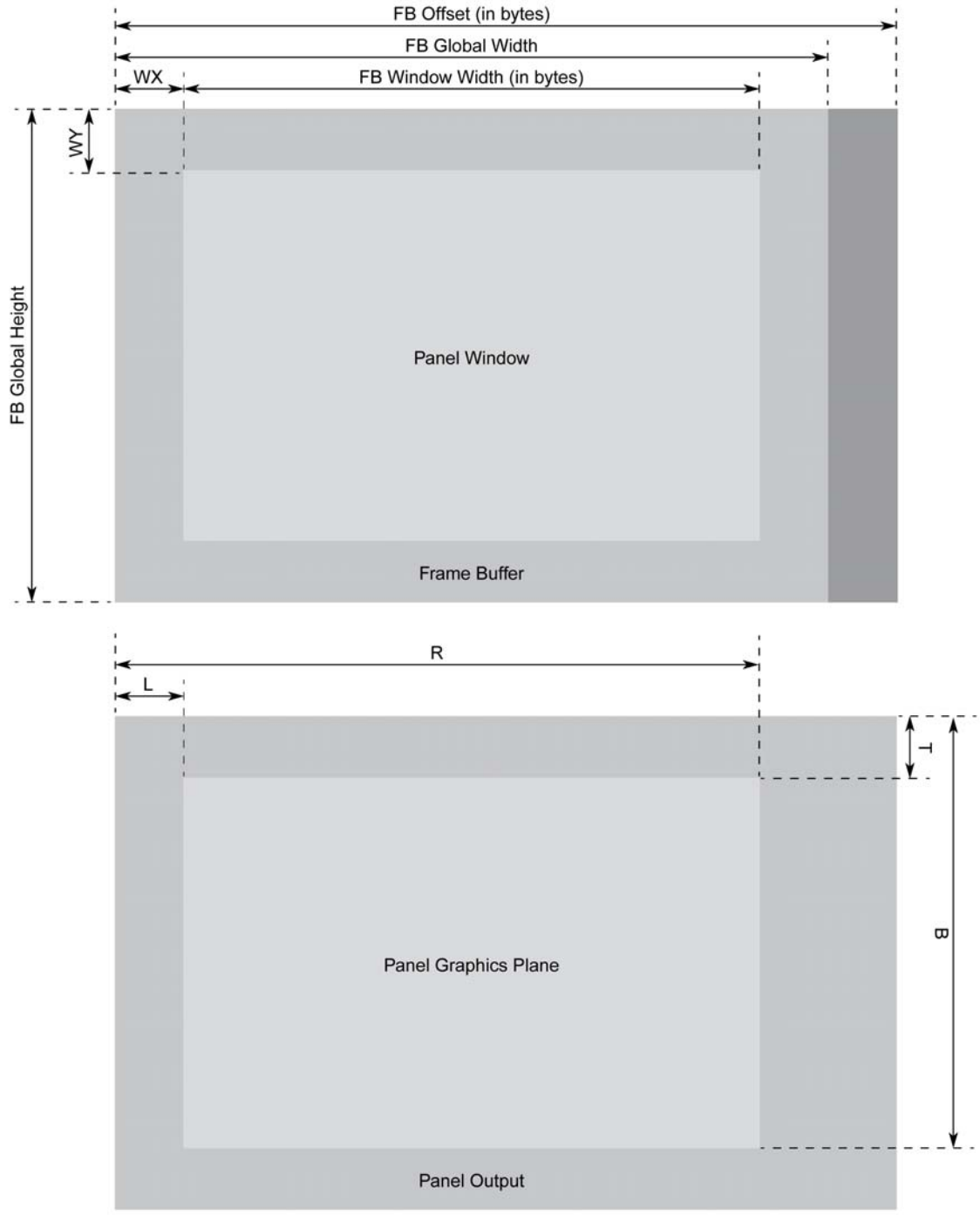


Figure 19: Video Windowing

Primary Display Control

Read/Write MMIO_base + 0x080000

Power-on Default 0x00010000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res		Sel R/W		En R/W	Bias R/W	Data R/W	VDD R/W	Res				DD R/W	DP R/w	FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	CP R/W	VSP R/W	HSP R/W	V R/W	CAPT R/W	CK R/W	TE R/W	VPD R/W	VP R/W	HPD R/W	HP R/W	γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:30	Res	These bits are reserved.
29:28	Sel	Panel Data Select. 00: Panel Data. 01: VGA Data. 10: Secondary Display Data. 11: Reserved.
27	En	FPEN Control. 0: Drive low. 1: Drive high.
26	Bias	Control VBIASEN Output Pin. 0: Driven low. 1: Driven high.
25	Data	Panel Control Signals and Data Lines Enable. 0: Disable panel control signals and data lines. 1: Enable panel control signals and data lines.
24	VDD	Control FPVDDEN Output Pin. 0: Driven low. 1: Driven high.
23:20	Res	These bits are reserved.
19	DD	Dual Digital Display Output. 0: Disable. 1: Enable.
18	DP	Double Pixel Output. 0: Disable. 1: Enable.
17:16	FIFO	Panel Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15	Res	This bit is reserved.
14	CP	Clock Phase Select. 0: Clock active high. 1: Clock active low.
13	VSP	Vertical Sync Pulse Phase Select. 0: Vertical sync pulse active high. 1: Vertical sync pulse active low.
12	HSP	Horizontal Sync Pulse Phase Select. 0: Horizontal sync pulse active high. 1: Horizontal sync pulse active low.

Bit(s)	Name	Description
11	V	VSYNC
10	CAPT	Enabel Capture Timing (Frame Lock). 0: Disable capture timing. 1: Lock panel timing to ZV Port 0 timing.
9	CK	Enable Color Key. 0: Disable color key. 1: Enable color key.
8	TE	Enable Panel Timing. 0: Disable panel timing. 1: Enable panel timing.
7	VPD	Vertical Panning Direction. 0: Panning down. 1: Panning up.
6	VP	Enable Automatic Vertical Panning. 0: Disable. 1: Enable.
5	HPD	Horizontal Panning Direction. 0: Pan to the right. 1: Pan to the left.
4	HP	Enable Automatic Horizontal Panning. 0: Disable. 1: Enable.
3	γ	Enable Gamma Control. Gamma control can only be enabled in RGB 5:6:5 and RGB 8:8:8 modes. 0: Disable. 1: Enable.
2	E	Primary Graphics Plane Enable. 0: Disable Primary graphics plane. 1: Enable Primary graphics plane. Note: This bit has delayed update until the next VSYNC after change of value, and bit 8 of this register must be set to 1 for a VSYNC to happen.
1:0	Format	Primary Graphics Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 32-bit RGB 8:8:8 mode. 11: Reserved.

Primary Display Panning Control

Read/Write MMIO_base + 0x080004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VPan R/W								Res		VWait R/W					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HPan R/W								Res		HWait R/W					

Bit(s)	Name	Description
31:24	VPan	Number of lines to pan vertically.
23:22	Res	These bits are reserved.
21:16	VWait	Number of vertical sync pulses for each vertical pan.
15:8	HPan	Number of pixels to pan horizontally.
7:6	Res	These bits are reserved.
5:0	HWait	Number of horizontal sync pulses for each horizontal pan.

Primary Display Color Key

Read/Write MMIO_base + 0x080008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Color key mask for video window plane.
15:0	Value	Color key value for video window plane.

Primary Display FB Address

Read/Write MMIO_base + 0x08000C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer for the Primary graphics plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Primary Display FB Offset/Window Width

Read/Write MMIO_base + 0x080010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res		FB Window Width R/W										0000			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res		FB Offset R/W										0000			

Bit(s)	Name	Description
31:30	Res	These bits are reserved.
29:20	FB Window Width	Number of bytes per line of the frame buffer window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Res	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the FB graphics plane.
3:0	0000	These bits are hardwired to zeros.

Primary Display FB Width

Read/Write MMIO_base + 0x080014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				FB Global Width R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				WX R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	FB Global Width	Width of FB graphics window specified in pixels (see Figure 5-4).
15:12	Res	These bits are reserved.
11:0	WX	Starting x-coordinate of Primary graphics window specified in pixels.

Primary Display FB Height

Read/Write MMIO_base + 0x080018

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				FB Global Height R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				WY R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	FB GLobal Height	Height of FB graphics window specified in lines.
15:12	Res	These bits are reserved.
11:0	WY	Starting y-coordinate of Primary graphics window specified in lines.

Primary Display Plane TL Location

Read/Write MMIO_base + 0x08001C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					T R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					L R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	T	Top location of the Primary Display graphics plane specified in lines.
15:11	Res	These bits are reserved.
10:0	L	Left location of the Primary Display graphics plane specified in pixels.

Primary Display Plane BR Location

Read/Write MMIO_base + 0x080020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					B R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					R R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	B	Bottom location of the Primary Display graphics plane specified in lines.
15:11	Res	These bits are reserved.
10:0	R	Right location of the Primary Display graphics plane specified in pixels.

Primary Display Horizontal Total

Read/Write MMIO_base + 0x080024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				HT R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				HDE R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	HT	Primary Display horizontal total specified as number of pixels - 1.
15:12	Res	These bits are reserved.
11:0	HDE	Primary Display horizontal display end specified as number of pixels - 1.

Primary Display Horizontal Sync

Read/Write MMIO_base + 0x080028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								HSW R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				HS R/W											

Bit(s)	Name	Description
31:24	Res	These bits are reserved.
23:16	HSW	Primary Display horizontal sync width specified in pixels.
15:12	Res	These bits are reserved.
11:0	HS	Primary Display horizontal sync start specified as pixel number - 1.

Primary Display Vertical Total

Read/Write MMIO_base + 0x08002C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					VT R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res					VDE R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	VT	Primary Display vertical total specified as number of lines - 1.
15:11	Res	These bits are reserved.
10:0	VDE	Primary Display vertical display end specified as number of lines - 1.

Primary Display Vertical Sync

Read/Write MMIO_base + 0x080030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res										VSH R/W					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res					VS R/W										

Bit(s)	Name	Description
31:22	Res	These bits are reserved.
21:16	VSH	Primary Display vertical sync height specified in lines.
15:11	Res	These bits are reserved.
10:0	VS	Primary Display vertical sync start specified as line number - 1.

Primary Display Current Line

Read MMIO_base + 0x080034

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					Line R										

Bit(s)	Name	Description
31:11	Res	These bits are reserved.
10:0	Line	Primary Display current line being fetched.

6.2.2 *Video Control Registers*

Figure 21 shows the layout of the Video Control registers.

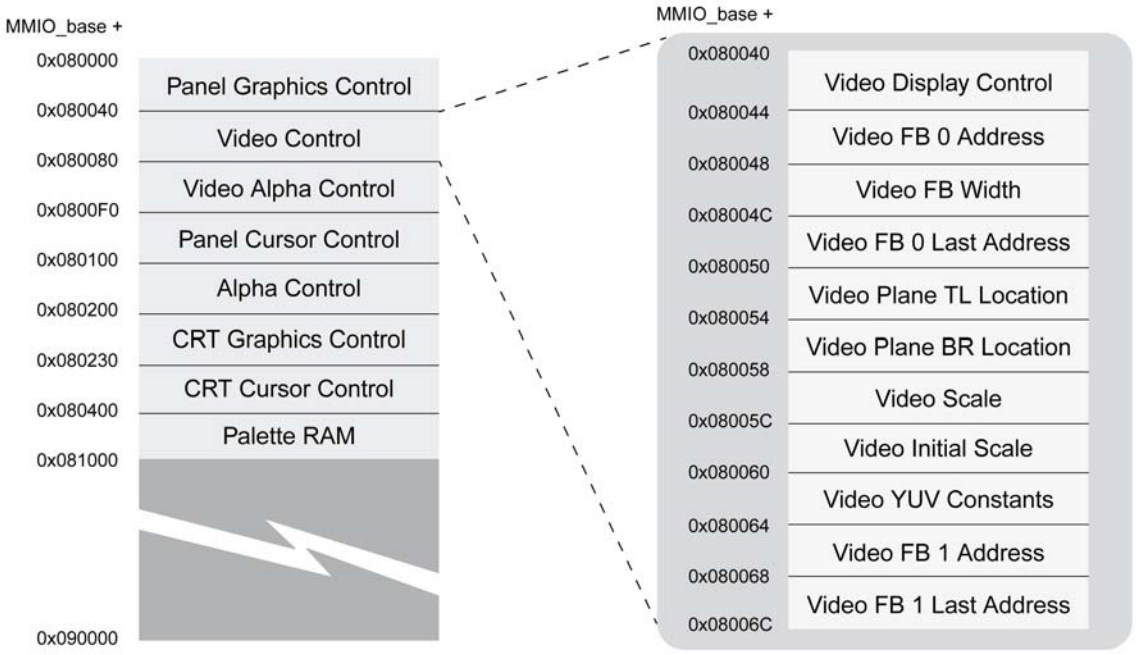


Figure 20: Video Control Register Space

Video Display Control

Read/Write MMIO_base + 0x080040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res													LineBuf R/W	FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Buf R	CB R/W	DB R/W	BS R/W	VS R/W	HS R/W	VI R/W	HI R/W	Pixel R/W				γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:19	Res	These bits are reserved.
18	LineBuf	Line Buffer. 0: Disable. 1: Enable.
17:16	FIFO	Video Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15	Buf	Current Video Frame Buffer Used. This bit is read-only. 0: Buffer 0. 1: Buffer 1.
14	CB	Use Capture Frame Buffer as Video Frame Buffer. 0: Disable. 1: Enable.
13	DB	Enable Double Buffering. 0: Disable. 1: Enable.

Bit(s)	Name	Description
12	BS	Enable Byte Swapping for YUV Data. 0: Disable (YUYV). 1: Enable (UYVY).
11	VS	Force Vertical Scale Factor to ½. 0: Disable. 1: Enable.
10	HS	Force Horizontal Scale Factor to ½. 0: Disable. 1: Enable.
9	VI	Enable Vertical Interpolation. 0: Disable. 1: Enable.
8	HI	Enable Horizontal Interpolation. 0: Disable. 1: Enable.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	Res	This bit is reserved.
2	E	Video Plane Enable. 0: Disable video plane. 1: Enable video plane.
1:0	Format	Video Plane Format. 00: reserved. 01: 16-bit RGB 5:6:5 mode. 10: reserved. 11: 16-bit YUYV mode.

1.All display devices have an inherent non-linearity so that the intensity of the output is not linearly proportional to the input signal over the full range of input values. The gamma control helps to correct this nonlinearity.

Video FB 0 Address

Read/Write MMIO_base + 0x080044

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer 0 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video FB Width

Read/Write MMIO_base + 0x080048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res		Width R/W										0000			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		Offset R/W										0000			

Bit(s)	Name	Description
31:30	Res	These bits are reserved.
29:20	Width	Number of bytes per line of the video plane specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Res	These bits are reserved.
13:4	Offset	Number of 128-bit aligned bytes per line of the video plane.
3:0	0000	These bits are hardwired to zeros.

Video FB 0 Last Address

Read/Write MMIO_base + 0x08004C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	Res	Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Internal memory. 1: External memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of last byte of frame buffer 0 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Plane TL Location

Read/Write MMIO_base + 0x080050

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					T R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					L R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	T	Top location of the video plane specified in lines.
15:11	Res	These bits are reserved.
10:0	L	Left location of the video plane specified in pixels.

Video Plane BR Location

Read/Write MMIO_base + 0x080054

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					B R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					R R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	B	Bottom location of the video plane specified in lines.
15:11	Res	These bits are reserved.
10:0	R	Right location of the video plane specified in pixels.

Video Scale

Read/Write MMIO_base + 0x080058

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VS R/W	Res			VScale R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS R/W	Res			HScale R/W											

Bit(s)	Name	Description
31	VS	Select Vertical Video Scaling. 0: Video expands vertically. 1: Video shrinks vertically.
30:28	Res	These bits are reserved.
27:16	VScale	Vertical Video Scale Factor. For expansion: VScale = ($height_{src}$ / $height_{dest}$) * 2^{12}. For shrinking: VScale = ($height_{dest}$ / $height_{src}$) * 2^{12}.
15	HS	Select Horizontal Video Scaling. 0: Video expands horizontally. 1: Video shrinks horizontally.
14:12	Res	These bits are reserved.
11:0	HScale	Horizontal Video Scale Factor. For expansion: HScale = ($width_{src}$ / $width_{dest}$) * 2^{12}. For shrinking: HScale = ($width_{dest}$ / $width_{src}$) *2^{12}.

Scaling example: To expand (magnify) the horizontal scale by a factor of 3:

1 Set HS = 0.

2 Calculate the scaling factor: (widthsrc / widthdest) * 212 = (1/3) * 212

3 Set HScale. In this example, HScale = 0101 0101 0101 b or 555h.

To shrink the horizontal scale by a factor of 3:

1 Set HS = 1.

2 Calculate the scaling factor: (widthdest / widthsrc) * 212 = ((1/3/)1) * 212 = 1/3 * 212

3. Set HScale. Note that the HScale setting is the same for shrinking by 1/3 as it is for magnifying by a factor of 3, only the setting of HS differs

Video Initial Scale

Read/Write MMIO_base + 0x08005C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				VS R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res				HS R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	VS	Initial vertical scale factor for video buffer.
15:12	Res	These bits are reserved.
11:0	HS	Initial horizontal scale factor for video buffer.

Video YUV Constants

Read/Write MMIO_base + 0x080060

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	Blue Conversion Constant.

Video FB 1 Address

Read/Write MMIO_base + 0x080064

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer 1 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video FB 1 Last Address

Read/Write MMIO_base + 0x080068

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of last byte of frame buffer 1 for the video plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

6.2.3 *Video Alpha Control Registers*

Figure 22 shows the layout of the Video Alpha Control registers.

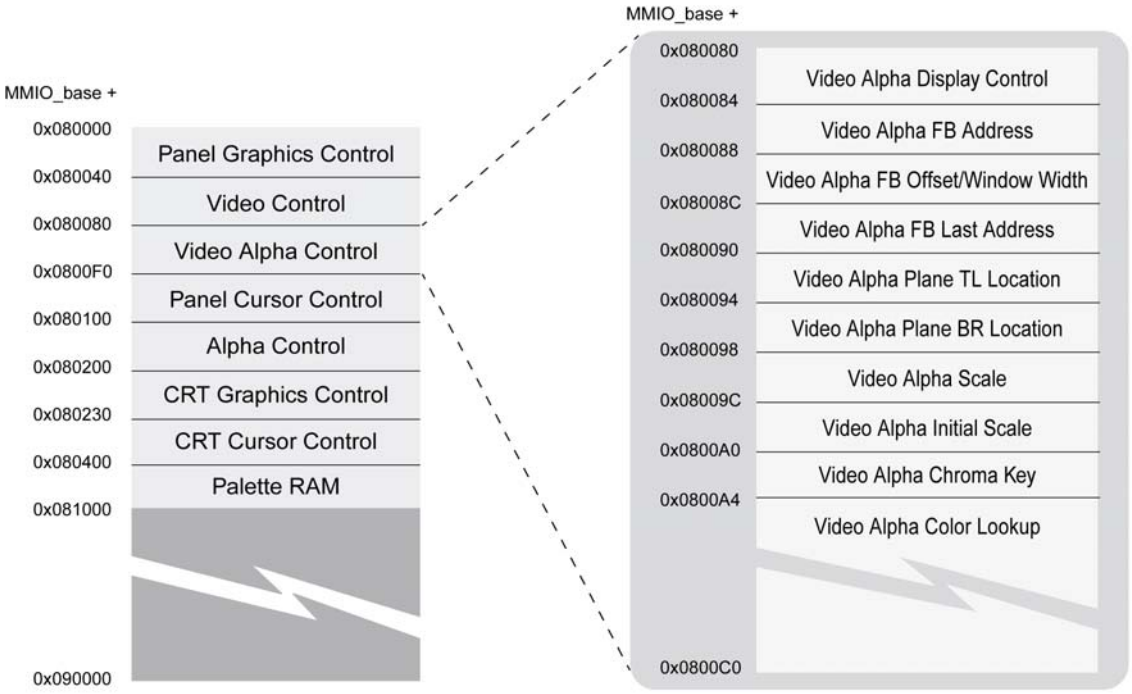


Figure 21: Video Alpha Control Register Space

Video Alpha Display Control

Read/Write MMIO_base + 0x080080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Sel R/W	Alpha R/W				Res						FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res				VS R/W	HS R/W	VI R/W	HI R/W	Pixel R/W				CK R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28	Sel	Alpha Select. 0: Use per-pixel alpha values. 1: Use alpha value specified in *Alpha*.
27:24	Alpha	Video Alpha Plane Alpha Value. This field is only valid when the *Sel* bit is 1.
23:18	Res	These bits are reserved.
17:16	FIFO	Video Alpha Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15:12	Res	These bits are reserved.
11	VS	Force Vertical Scale Factor to ½. 0: Disable. 1: Enable.
10	HS	Force Horizontal Scale Factor to ½. 0: Disable. 1: Enable.
9	VI	Enable Vertical Interpolation. 0: Disable. 1: Enable.
8	HI	Enable Horizontal Interpolation. 0: Disable. 1: Enable.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	CK	Enable Chroma Key. 0: Disable. 1: Enable.
2	E	Video Alpha Plane Enable. 0: Disable video plane. 1: Enable video plane.
1:0	Format	Video Alpha Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 8-bit indexed αI 4:4 mode. 11: 16-bit αRGB 4:4:4:4 mode.

Video Alpha FB Address

Read/Write MMIO_base + 0x080084

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer for the video alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Alpha FB Offset/Window Width

Read/Write MMIO_base + 0x080088

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res		Window Width R/W										0000			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res		FB Offset R/W										0000			

Bit(s)	Name	Description
31:30	Res	These bits are reserved.
29:20	Window Width	Number of bytes per line of the video alpha window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Res	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the video alpha FB.
3:0	0000	These bits are hardwired to zeros.

Video Alpha FB Last Address

Read/Write MMIO_base + 0x08008C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of last byte of frame buffer for the video alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Video Alpha Plane TL Location

Read/Write MMIO_base + 0x080090

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					Top R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res					Left R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	Top	Top location of the video alpha plane specified in lines.
15:11	Res	These bits are reserved.
10:0	Left	Left location of the video alpha plane specified in pixels.

Video Alpha Plane BR Location

Read/Write MMIO_base + 0x080094

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					Bottom R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res					Right R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	Bottom	Bottom location of the video alpha plane specified in lines.
15:11	Res	These bits are reserved.
10:0	Right	Right location of the video alpha plane specified in pixels.

Video Alpha Scale

Read/Write MMIO_base + 0x080098

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VS R/W	Res			VScale R/W											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HS R/W	Res			HScale R/W											

Bit(s)	Name	Description
31	VS	Select Vertical Video Scaling. 0: Video expands vertically. 1: Video shrinks vertically.
30:28	Res	These bits are reserved.
27:16	VScale	Vertical Video Scale Factor. For expansion: VScale = $height_{src}$ / $height_{dest}$ * 2_{12}. For shrinking: VScale = $height_{dest}$ / $height_{src}$ * 2_{12}.
15	HS	Select Horizontal Video Scaling. 0: Video expands horizontally. 1: Video shrinks horizontally.
14:12	Res	These bits are reserved.
11:0	HScale	Horizontal Video Scale Factor. For expansion: HScale = $width_{src}$ / $width_{dest}$ * 2_{12}. For shrinking: HScale = $width_{dest}$ / $width_{src}$ * 2_{12}.

Video Alpha Initial Scale

Read/Write MMIO_base + 0x08009C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				VS R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				HS R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	VS	Initial Vertical Scale Factor.
15:12	Res	These bits are reserved.
11:0	HS	Initial Horizontal Scale Factor.

Video Alpha Chroma Key

Read/Write MMIO_base + 0x0800A0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Chroma Key Mask for Video Alpha Plane. 0: Compare respective bit. 1: Do not compare respective bit.
15:0	Value	Chroma Key Value for Video Alpha Plane.

Video Alpha Color Lookup

Read/Write MMIO_base + 0x0800A4-0x0800C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Lookup1 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lookup0 R/W															

Bit(s)	Name	Description
31:16	$Lookup_1$	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 1.
15:0	$Lookup_0$	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 0.

There are 8 Video Alpha Color Lookup registers, each containing two RGB 5:6:5 color lookup values for each of the 16 4-bit indexed colors.

6.2.4 *Primary Display Cursor Control Registers*

Figure 23 shows the layout of the Primary Display Cursor Control registers.

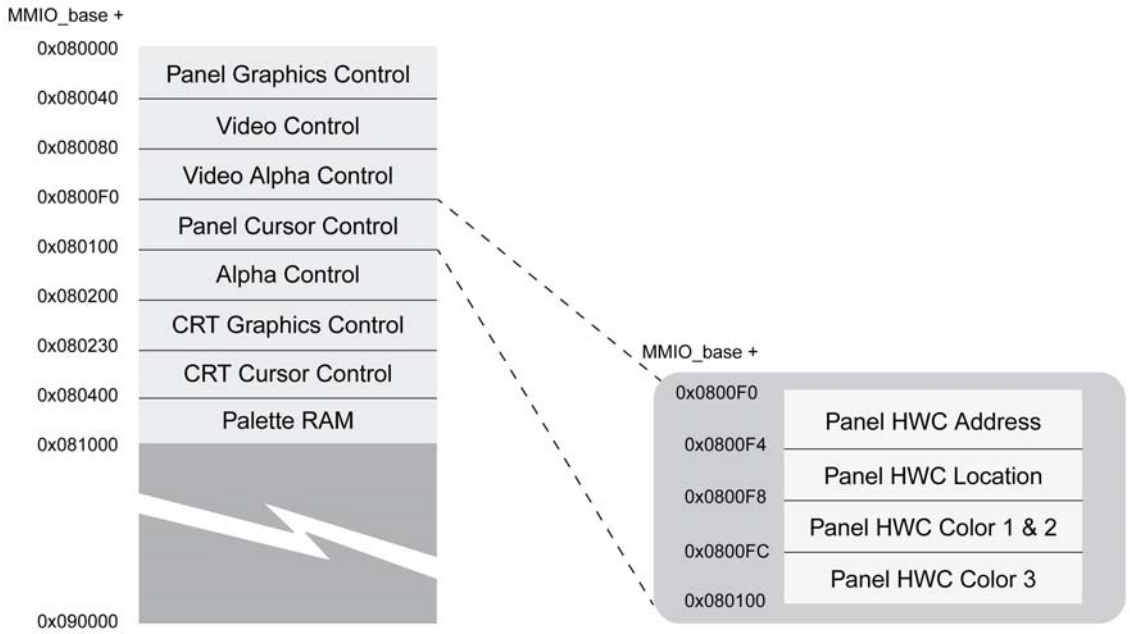


Figure 22: Primary Display Cursor Control Register Space

Primary Display HWC Address

Read/Write MMIO_base + 0x0800F0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E R/W	Res			Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31	E	Enable Primary Display Hardware Cursor. 0: Disable. 1: Enable.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of Primary Display hardware cursor with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Primary Display HWC Location

Read/Write MMIO_base + 0x0800F4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				T R/W	Y R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res				L R/W	X R/W										

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	T	Top Boundary Select. 0: Primary Display hardware cursor is within screen top boundary. 1: Primary Display hardware cursor is partially outside screen top boundary.
26:16	Y	Primary Display Hardware Cursor Y Position.
15:12	Res	These bits are reserved.
11	L	Left Boundary Select. 0: Primary Display hardware cursor is within screen left boundary. 1: Primary Display hardware cursor is partially outside screen left boundary.
10:0	X	Primary Display Hardware Cursor X Position.

Primary Display HWC Color 1 & 2

Read/Write MMIO_base + 0x0800F8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Color2 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color1 R/W															

Bit(s)	Name	Description
31:16	Color2	Primary Display hardware cursor color 2 in RGB 5:6:5.
15:0	Color1	Primary Display hardware cursor color 1 in RGB 5:6:5.

Primary Display HWC Color 3

Read/Write MMIO_base + 0x0800FC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color3 R/W															

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:0	Color3	Primary Display hardware cursor color 3 in RGB 5:6:5.

6.2.5 *Alpha Control Registers*

Figure 24 shows the layout of the Alpha Control registers.

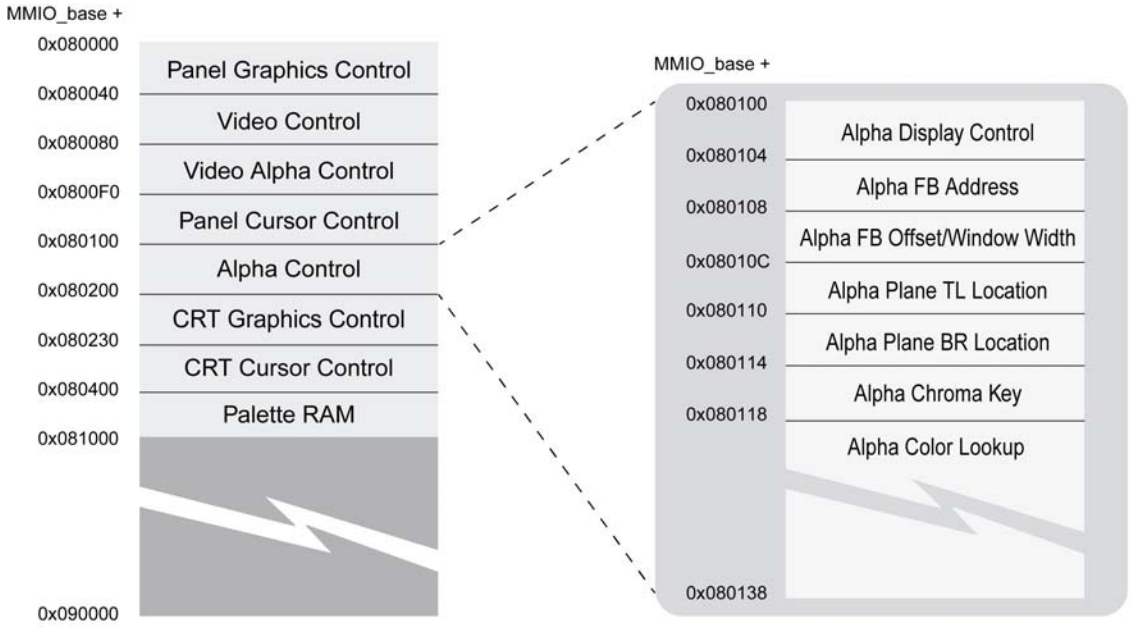


Figure 23: Alpha Control Register Space

Alpha Display Control

Read/Write MMIO_base + 0x080100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res			Sel R/W	Alpha R/W				Res						FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res								Pixel R/W				CK R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:29	Res	These bits are reserved.
28	Sel	Alpha Select. 0: Use per-pixel alpha values. 1: Use alpha value specified in *Alpha*.
27:24	Alpha	Alpha Plane Alpha Value. This field is only valid when the *Sel* bit is 1.
23:18	Res	These bits are reserved.
17:16	FIFO	Video Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15:8	Res	These bits are reserved.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	CK	Enable Chroma Key. 0: Disable chroma key. 1: Enable chroma key.
2	E	Alpha Plane Enable. 0: Disable alpha plane. 1: Enable alpha plane.
1:0	Format	Alpha Plane Format. 00: reserved. 01: 16-bit RGB 5:6:5 mode. 10: 8-bit indexed αI 4:4 mode. 11: 16-bit αRGB 4:4:4:4 mode.

Alpha FB Address

Read/Write MMIO_base + 0x080104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of frame buffer for the alpha plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Alpha FB Offset/Window Width

Read/Write MMIO_base + 0x080108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res		Window Width R/W										0000			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res		FB Offset R/W										0000			

Bit(s)	Name	Description
31:30	Res	These bits are reserved.
29:20	Window Width	Number of bytes per line of the alpha window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Res	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the alpha FB.
3:0	0000	These bits are hardwired to zeros.

Alpha Plane TL Location

Read/Write MMIO_base + 0x08010C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					Top R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					Left R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	Top	Top location of the alpha plane specified in lines.
15:11	Res	These bits are reserved.
10:0	Left	Left location of the alpha plane specified in pixels.

Alpha Plane BR Location

Read/Write MMIO_base + 0x080110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					Bottom R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					Right R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	Bottom	Bottom location of the alpha plane specified in lines.
15:11	Res	These bits are reserved.
10:0	Right	Right location of the alpha plane specified in pixels.

Alpha Chroma Key

Read/Write MMIO_base + 0x080114

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mask R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value R/W															

Bit(s)	Name	Description
31:16	Mask	Chroma Key Mask for Alpha Plane. 0: Compare respective bit. 1: Do not compare respective bit.
15:0	Value	Chroma Key Value for Alpha Plane.

Alpha Color Lookup

Read/Write MMIO_base + 0x080118-0x080134

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Lookup1 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lookup0 R/W															

Bit(s)	Name	Description
31:16	Lookup1	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 1.
15:0	Lookup0	Alpha RGB 5:6:5 color lookup value for 4-bit indexed color 0.

There are 8 Alpha Color Lookup registers, each containing two RGB 5:6:5 color lookup values for each of the 16 4-bit indexed colors.

6.2.6 *Secondary Display Graphics Control Registers*

Figure 25 shows the layout of the Secondary Display Graphics Control registers.

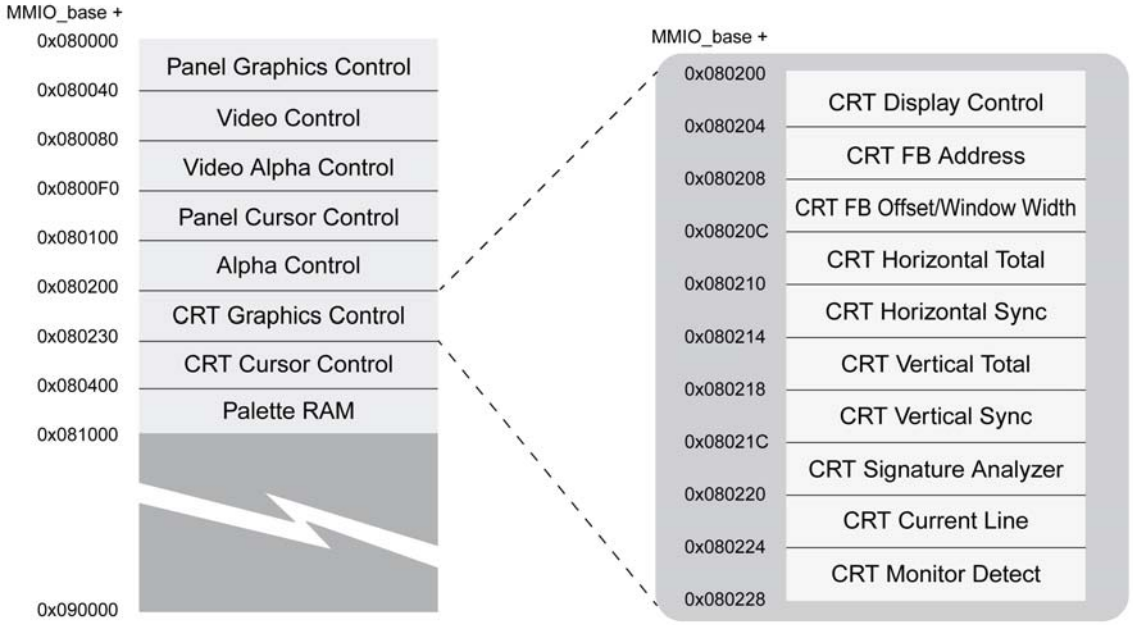


Figure 24: Secondary Display Graphics Control Register Space

Secondary Display Control

Read/Write MMIO_base + 0x080200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					VDS	Res	HAC	Lock	Exp	VI	HI	Sel		FIFO R/W	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res	CP R/W	VSP R/W	HSP R/W	VS R	B R/W	Res	TE R/W	Pixel R/W				γ R/W	E R/W	Format R/W	

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26	VDS	VGA Data Shift. (Color data shift from lower 6-bit to 8-bit) 0: Enable. 1: Disable.
25	Res	This bit is reserved.
24	HAC	Enable Horizontal Auto-Centering. 0: Disable. 1: Enable.
23	Lock	Enable Capture Timing (Frame Lock). 0: Disable capture timing. 1: Lock panel timing to CRT timing.
22	Exp	Enable Auto Expansion. 0 Disable. 1: Enable.
21	VI	Enable Vertical Interpolation. 0: Disable. 1: Enable.
20	HI	Enable Horizontal Interpolation. 0: Disable. 1: Enable.
19:18	Sel	Secondary Display Data Select. 00: Panel Data. 01: VGA Data. 10: CRT Data. 11: reserved.
17:16	FIFO	Secondary Display Data FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 00: 1 or more entries empty. 01: 3 or more entries empty. 10: 7 or more entries empty. 11: 11 or more entries empty.
15	Res	This bit is reserved.
14	CP	CRT Clock Phase Select. 0: CRT clock active high. 1: CRT clock active low.
13	VSP	Vertical Sync Pulse Phase Select. 0: Vertical sync pulse active high. 1: Vertical sync pulse active low.
12	HSP	Horizontal Sync Pulse Phase Select. 0: Horizontal sync pulse active high. 1: Horizontal sync pulse active low.
11	VS	Vertical Sync. This bit is read only.
10	B	CRT Data Blanking. 0: CRT will show pixels. 1: CRT will be blank.
9	Res	This bit is reserved.

Bit(s)	Name	Description
8	TE	Enable CRT Timing. 0: Disable CRT timing. 1: Enable CRT timing.
7:4	Pixel	Starting Pixel Number for Smooth Pixel Panning.
3	γ	Enable Gamma Control. Gamma control can be enabled only in RGB 5:6:5 and RGB 8:8:8 modes. 0: Disable gamma control. 1: Enable gamma control.
2	E	Secondary Display Graphics Plane Enable. 0: Disable Secondary Display Graphics plane. 1: Enable Secondary Display Graphics plane. Note: This bit has delayed update until the next VSYNC after change of value, and bit 8 of this register must be set to 1 for a VSYNC to happen.
1:0	Format	Secondary Display Graphics Plane Format. 00: 8-bit indexed mode. 01: 16-bit RGB 5:6:5 mode. 10: 32-bit RGB 8:8:8 mode. 11: reserved.

Secondary Display FB Address

Read/Write MMIO_base + 0x080204

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: No flip pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of the frame buffer for the Secondary Display graphics plane with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Secondary Display FB Offset/Window Width

Read/Write MMIO_base + 0x080208

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res		Window Width R/W										0000			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		FB Offset R/W										0000			

Bit(s)	Name	Description
31:30	Res	These bits are reserved.
29:20	Window Width	Number of bytes per line of the Secondary Display graphics window specified in 128-bit aligned bytes.
19:16	0000	These bits are hardwired to zeros.
15:14	Res	These bits are reserved.
13:4	FB Offset	Number of 128-bit aligned bytes per line of the Secondary Display graphics FB.
3:0	0000	These bits are hardwired to zeros.

Secondary Display Horizontal Total

Read/Write MMIO_base + 0x08020C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				HT R/W											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				HDE R/W											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	HT	Secondary Display horizontal total specified as number of pixels – 1.
15:12	Res	These bits are reserved.
11:0	HDE	Secondary Display horizontal display end specified as number of pixels – 1.

Secondary Display Horizontal Sync

Read/Write MMIO_base + 0x080210

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								HSW R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res				HS R/W											

Bit(s)	Name	Description
31:24	Res	These bits are reserved.
23:16	HSW	Secondary Display horizontal sync width specified in pixels.
15:12	Res	These bits are reserved.
11:0	HS	Secondary Display horizontal sync start specified as pixel number - 1.

Secondary Display Vertical Total

Read/Write MMIO_base + 0x080214

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					VT R/W										
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res					VDE R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	VT	Secondary Display vertical total specified as number of lines – 1.
15:11	Res	These bits are reserved.
10:0	VDE	Secondary Display vertical display end specified as number of lines – 1.

Secondary Display Vertical Sync

Read/Write MMIO_base + 0x080218

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res										VSH R/W					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res					VS R/W										

Bit(s)	Name	Description
31:22	Res	These bits are reserved.
21:16	VSH	Secondary Display vertical sync height specified in lines.
15:11	Res	These bits are reserved.
10:0	VS	Secondary Display vertical sync start specified as line number - 1.

Secondary Display Signature Analyzer

Read/Write MMIO_base + 0x08021C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Status R															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res												E R/W	R R/W	Sel R/W	

Bit(s)	Name	Description
31:16	Status	Analyzer Signature. This field is read-only.
15:4	Res	These bits are reserved.
3	E	Enable Signature Analyzer. 0: Disable. 1: Enable.
2	R	Reset Signature Analyzer. 0: Normal. 1: Reset.
1:0	Sel	Source Select for Signature Analyzer. 00: Red color. 01: Green color. 10: Blue color. 11: reserved.

Secondary Display Current Line

Read MMIO_base + 0x080220

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					Line R										

Bit(s)	Name	Description
31:11	Res	These bits are reserved.
10:0	Line	Secondary Display Current Line Being Fetched.

CRT Monitor Detect

Read/Write MMIO_base + 0x080224

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				R1/G1/B1 MDET R	R1/G1/B1 E R/W	R0/G0/B0 MDET R	R0/G0/B0 E R/W	Data R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data R/W															

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	R1/G1/B1 MDET	R1/G1/B1 Monitor Detect Read Back. 0: Monitor Absent. R1, G1, and B1 voltage are greater than 0.325 V. 1: Monitor Present. R1, G1, or B1 voltage is less than or equal to 0.325 V.
26	R1/G1/B1 E	R1/G1/B1 Monitor Detect Enable. 0: Disable. 1: Enable.
25	R0/G0/B0 MDET	R0/G0/B0 Monitor Detect Read Back. 0: Monitor Absent. R0, G0, and B0 voltage are greater than 0.325 V. 1: Monitor Present. R0, G0, or B0 voltage is less than or equal to 0.325 V.
24	R0/G0/B0 E	R0/G0/B0 Monitor Detect Enable. 0: Disable. 1: Enable.
23:0	Data	Monitor Detect Data in RGB 8:8:8 and is used by both R0/G0/B0 and R1/G1/B1 channels. Bit [23:16], [15:8], and [7:0] are corresponding to R, G, and B outputs respectively.

Secondary Display Scaler Register

Read/Write MMIO_base + 0x080228

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				VSF											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				HSF											

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27:16	VSF	Vertical Scale Factor.
15:12	Res	These bits are reserved.
11:0	HSF	Horizontal Scale Factor.

6.2.7 Secondary Display Cursor Control Registers

Figure 26 shows the layout of the Secondary Display Cursor Control registers.

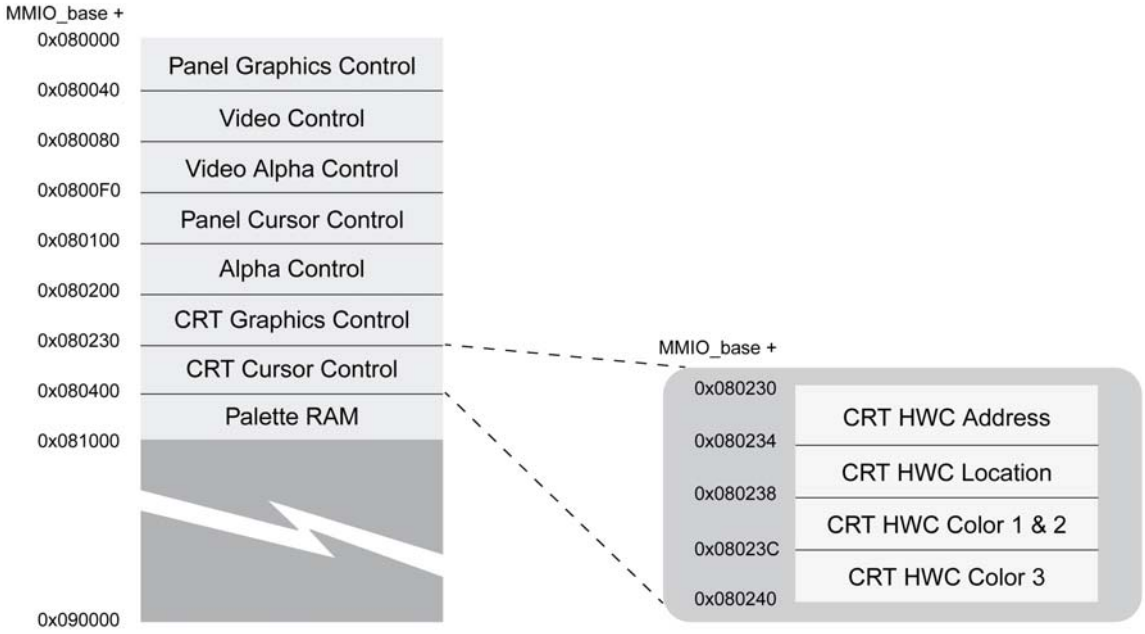


Figure 25: Secondary Display Cursor Control Register Space

Secondary Display HWC Address

Read/Write MMIO_base + 0x080230

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
E R/W	Res			Ext R/W	Res	Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Address R/W												0000			

Bit(s)	Name	Description
31	E	Enable Secondary Display Hardware Cursor. 0: Disable. 1: Enable.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: PCI Bus Master memory.
26	Res	This bit is reserved.
25:4	Address	Memory address of Secondary Display hardware cursor with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Secondary Display HWC Location

Read/Write MMIO_base + 0x080234

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				T R/W	Y R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				L R/W	X R/W										

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	T	Top Boundary Select. 0: Secondary Display hardware cursor is within screen top boundary. 1: Secondary Display hardware cursor is partially outside screen top boundary.
26:16	Y	Secondary Display Hardware Cursor Y Position.
15:12	Res	These bits are reserved.
11	L	Left Boundary Select. 0: Secondary Display hardware cursor is within screen left boundary. 1: Secondary Display hardware cursor is partially outside screen left boundary.
10:0	X	Secondary Display Hardware Cursor X Position.

Secondary Display HWC Color 1 & 2

Read/Write MMIO_base + 0x080238

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Color2 R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color1 R/W															

Bit(s)	Name	Description
31:16	Color2	Secondary Display Hardware Cursor Color 2 in RGB 5:6:5.
15:0	Color1	Secondary Display Hardware Cursor Color 1 in RGB 5:6:5.

Secondary Display HWC Color 3

Read/Write MMIO_base + 0x08023C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color3 R/W															

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:0	Color3	Secondary Display Hardware Cursor Color 3 in RGB 5:6:5.

6.2.8 *Palette RAM Registers*

Figure 27 shows the layout of the Palette RAM registers.

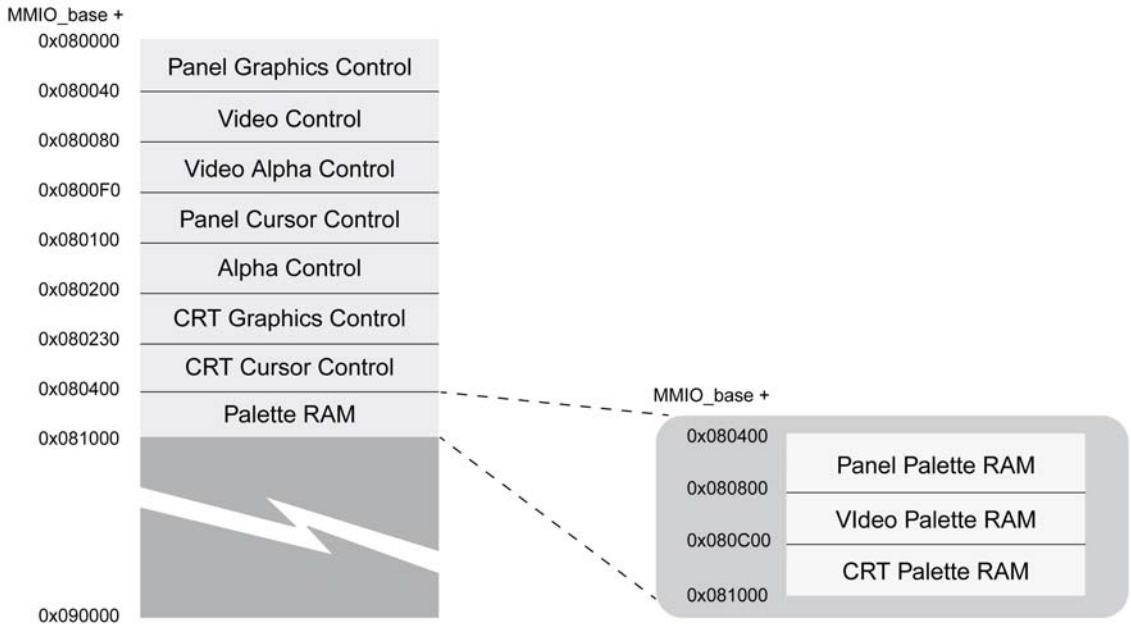


Figure 26: Palette RAM Register Space

Vertical Auto Expansion

Read/Write MMIO_base + 0x080240-0x080267

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								Comp							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Line				VS											

Bit(s)	Name	Description
31:24	Res	These bits are reserved. (must be 0)
23:16	Comp	Line Compare with Vertical Display End VGA mode: 3D4_01[7:0] Non-VGA mode: 0x8002C[10:3]
15:12	Line	Number of Line Before Secondary Display Horizontal Total to Start Panel Display. This will lock panel timing to Secondary Display timing. This also allows enough data in the line buffer to start graphic display from the line buffer.
11:0	VS	Vertical Scale Factor.

Horizontal Auto Expansion

Read/Write MMIO_base + 0x080268-0x08027F

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ACH								Comp							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				HS											

Bit(s)	Name	Description
31:24	ACH	Auto-Centering Horizontal Centering. (0x080268 to 0x08027C)
23:16	Comp	Line Compare with Horizontal Display End VGA mode: 3D4_12[7:0] Non-VGA mode: 0x80024[10:3]
15:12	Res	These bits are reserved.
11:0	HS	Horizontal Scale Factor.

Centering TL Location

Read/Write MMIO_base + 0x080280-0x080282

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					T R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					L R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	T	Top location of the centering specified in lines.
15:11	Res	These bits are reserved.
10:0	L	Left location of the centering specified in pixels.

Centering BR Location

Read/Write MMIO_base + 0x080284-0x080286

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					B R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					R R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	B	Bottom location of the centering specified in lines.
15:11	Res	These bits are reserved.
10:0	R	Right location of the centering specified in pixels.

Primary Display Palette RAM

Read/Write MMIO_base + 0x080400-0x0807FC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								Red R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Green R/W								Blue R/W							

Bit(s)	Name	Description
31:24	Res	These bits are reserved.
23:16	Red	For indexed color modes: 8-bit red color value. For 16- and 32-bit color modes: 8-bit red alpha value.
15:8	Green	For indexed color modes: 8-bit green color value. For 16- and 32-bit color modes: 8-bit green alpha value.
7:0	Blue	For indexed color modes: 8-bit blue color value. For 16- and 32-bit color modes: 8-bit blue alpha value.

There are 256 Primary Display Palette RAM registers, each containing a 24-bit RGB 8:8:8 color value.

Secondary Display Palette RAM

Read/Write MMIO_base + 0x080C00-0x080FFC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res								Red R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Green R/W								Blue R/W							

Bit(s)	Name	Description
31:24	Res	These bits are reserved.
23:16	Red	For indexed color modes: 8-bit red color value. For 16- and 32-bit color modes: 8-bit red alpha value.
15:8	Green	For indexed color modes: 8-bit green color value. For 16- and 32-bit color modes: 8-bit green alpha value.
7:0	Blue	For indexed color modes: 8-bit blue color value. For 16- and 32-bit color modes: 8-bit blue alpha value.

There are 256 Video Palette RAM registers, each containing a 24-bit RGB 8:8:8 color value.

7. GPIO

7.1 Functional Overview

7.1.1 GPIO Interface

The GPIO peripheral includes the following registers:

- Data register
- Data Direction register
- Interrupt Setup register
- Interrupt Status register
- Interrupt Reset register

7.2 Programmer's Model

The base address of the GPIO is not fixed, and can be different for any particular system implementation.

However, the offset of any particular register from the base address is fixed.

The following locations are reserved and must not be used during normal operation:

- Locations at offsets 0x424 to 0xFCC are reserved for possible future extensions and test purposes
- Locations at offsets +0xFDO to +0xFDC are reserved for future ID expansion.

Figure 28 shows how this 64kB region in the MMIO space is laid out. It controls the GPIO registers.

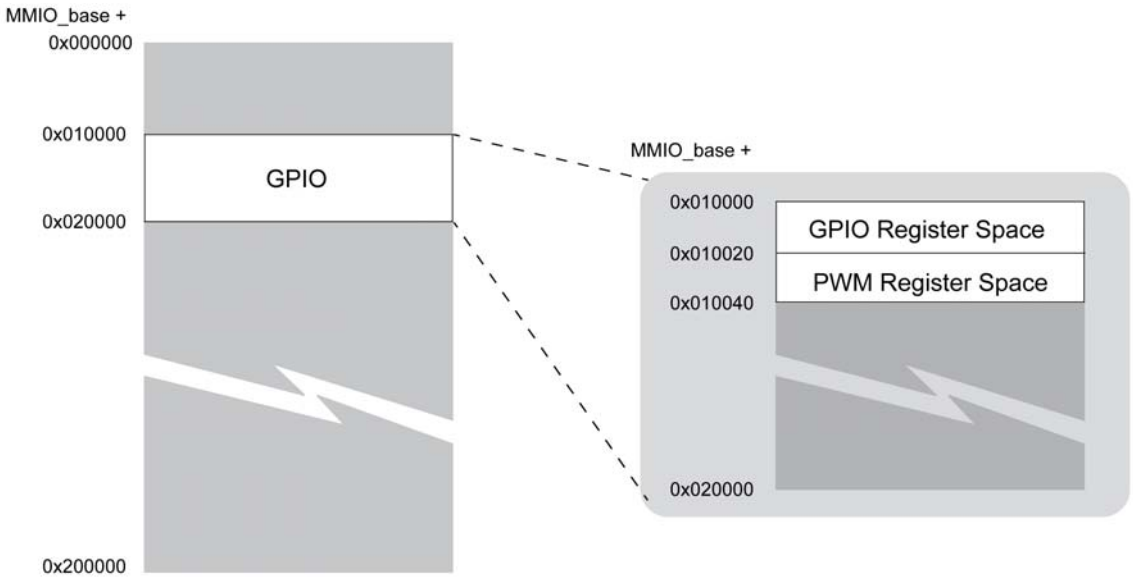


Figure 27: GPIO Register Space

The following sections define each region in more detail.

7.3 Register Descriptions

The GPIO registers are shown in Table 12.

Address	Type	Width	Reset Value	Register Name
0x010000	R/W	32	0x00000000	GPIO Data
0x010008	R/W	32	0x00000000	GPIO Data Direction
0x010010	R/W	32	0x00000000	GPIO Interrupt Setup
0x010014	R	32	0x00000000	GPIO Interrupt Status
0x010014	W	32	0x00000000	GPIO Interrupt Reset

Table 13: GPIO Register Summary

7.3.1 GPIO Register Descriptions

The GPIO registers are described in this section.

The GPIO registers control the GPIO pins. There are seven GPIO registers, two of which share the same address for interrupt status/reset. Figure 29 defines the register layout for the GPIO registers.

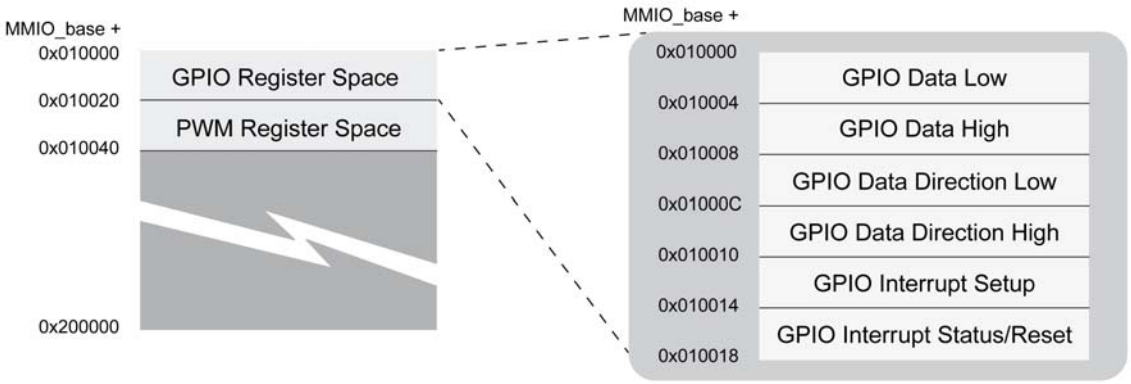


Figure 28: GPIO Register Space

GPIO Data

Read/Write Address 0x010000

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Data_{31:16}$ R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$Data_{15:0}$ R/W															

Bit(s)	Name	Description
31:0	$Data_{31:0}$	The values in the $Data_{31:0}$ bits reflect the value on the $GPIO_{31:0}$ pins.

This register reflects the value on a GPIO pin. If it is programmed as an input, the value of the GPIO pin is transferred to the corresponding bit in this register. If it is programmed as an output, the value of the bit is transferred to the corresponding GPIO pin.

GPIO Data Direction

Read/Write Address 0x010008

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
$Data_{31:16}$ R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$Data_{15:0}$ R/W															

Bit(s)	Name	Description
31:0	$Direction_{31:0}$	This register defines whether a GPIO pin is programmed as in input or as an output. 0: Input. 1: Output.

GPIO Interrupt Setup

Read/Write Address 0x010010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res									$Trigger_{31:25}$ R/W						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$Active_{31:25}$ R/W								Res	$Enable_{31:25}$ R/W						

Bit(s)	Name	Description
31:23	Res	These bits are reserved.
22:16	$Trigger_{31:25}$	Triggering Type. 0: Edge triggered. 1: Level triggered.
15	Res	This bit is reserved.
14:8	$Active_{31:25}$	Active State. 0: Active low or falling edge. 1: Active high or rising edge.
7	Res	This bit is reserved.
6:0	$Enable_{31:25}$	This register defines whether GPIO31:25 pins are programmed as regular input/output pins or as interrupt input pins. It also defines the interrupt type. 0: Regular GPIO Input/Output. 1: GPIO Interrupt.

GPIO Interrupt Status

Read Address 0x010014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res									$Status_{31:25}$ R/W						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															

Bit(s)	Name	Description
31:23	Res	These bits are reserved.
22:16	$Status_{31:25}$	This read/only register reflects the status of the interrupt pins. When an external interrupt happens on a GPIO interrupt pin, the status bit will be set to “1” until the software resets the interrupt by writing to the GPIO Interrupt Status. 0: Interrupt inactive. 1: Interrupt active.
15:0	Res	These bits are reserved.

GPIO Interrupt Reset

Write Address 0x010014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res									$Reset_{31:25}$ R/W						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															

Bit(s)	Name	Description
31:23	Res	These bits are reserved.
22:16	$Reset_{31:25}$	This field resets the GPIO interrupt. 0: No action. 1: Reset interrupt.
15:0	Res	These bits are reserved.

SPI 0 Control 0

Read/Write MMIO_base + 0x020n00 Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR R/W								Ph R/W	Pol R/W	Format R/W		DataSize R/W			

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:8	SCR	Serial Clock Rate. The clock rate is calculated as follows: where CPSDVSR is an even value from 2 to 254, programmed via the Clock Prescale register. FSSPCLK CPSDVSR 1 + SCR( )×
7	Ph	SCLKOUT Phase for Motorola SPI Frame.
6	Pol	SCLKOUT Polarity for Motorola SPI Frame. 0: Rising edge. 1: Falling edge.
5:4	Format	Frame Format. 00: Motorola SPI frame format. 01: Texas Instruments serial frame format. 10: National Microwire frame format. 11: Reserved
3:0	DataSize	Data Size Select. 0000: Reserved 0001: Reserved 0010: Reserved 0011: 4-bit 0100: 5-bit 0101: 6-bit 0110: 7-bit 0111: 8-bit 1000: 9-bit 1001: 10-bit 1010: 11-bit 1011: 12-bit 1100: 13-bit 1011: 14-bit 1110: 15-bit 1111: 16-bit

SPI 0 Control 1

Read/Write MMIO_base + 0x020n04

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res									O R/W	M R/W	E R/W	L R/W	OI R/W	TI R/W	RI R/W

Bit(s)	Name	Description
31:7	Res	These bits are reserved.
6	O	Slave-Mode Output Select. 0: Enable. 1: Disable.
5	M	Mode Select. 0: Master mode. 1: Slave mode.
4	E	SSP Enable. 0: Enable. 1: Disable.
3	L	Loopback Mode. 0: Normal. 1: Internal Loopback.
2	OI	Overflow Interrupt Enable. 0: Disable. 1: Enable.
1	TI	Transmit Interrupt Enable. 0: Disable. 1: Enable.
0	RI	Receive Interrupt Enable. 0: Disable. 1: Enable.

SPI 0 Data

Read/Write MMIO_base + 0x020n08

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data R/W															

When the SSP is programmed for National Microwire frame format, the default transmit data size is eight bits (the most significant byte is ignored).

Bit(s)	Name	Description
31:16	Res	These bits are reserved.
15:0	Data	Data read from receive FIFO or written to transmit FIFO.

SPI 0 Status

Read/Write MMIO_base + 0x020n0C

Power-on Default 0x00000003

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											B R	R R		T R	

Bit(s)	Name	Description
31:5	Res	These bits are reserved.
4	B	SSP Busy Flag. 0: Idle. 1: Busy.
3:2	R	Receive FIFO Status. 00: Empty. 01: Not empty. 11: Full.
1: 0	T	Transmit FIFO Status. 00: Full. 10: Not full. 11: Empty.

SPI 0 Clock Prescale

Read/Write MMIO_base + 0x020n10

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								Prescale R/W							

Bit(s)	Name	Description
31:8	Res	These bits are reserved.
7:0	Prescale	Clock Prescale Value. This must be an even number, so bit 0 is always “0”

SPI 0 Interrupt Status

Read/Write MMIO_base + 0x020n14

Power-on Default 0b0000.0000.0000.0000.0000.0000.0000.00XX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res													O R/W	T R	R R

Bit(s)	Name	Description
31:3	Res	These bits are reserved.
2	O	Receive FIFO Overflow Interrupt Status. Writing any value to this bit clears the interrupt. 0: Inactive. 1: Active.
1	T	Transmit FIFO Interrupt Status. This bit is read-only. 0: Inactive. 1: Acitve.
0	R	Receive FIFO Interrupt Status. This bit is read-only. 0: Inactive. 1: Active.

8. I²C Interface

8.1 Functional Overview

The SM750 supports one I²C interface. The interface is in Master mode with 7-bit addressing. It supports speeds up to 400 kbps (Fast mode).

Figure 30 shows a simplified block diagram of the I²C interface.

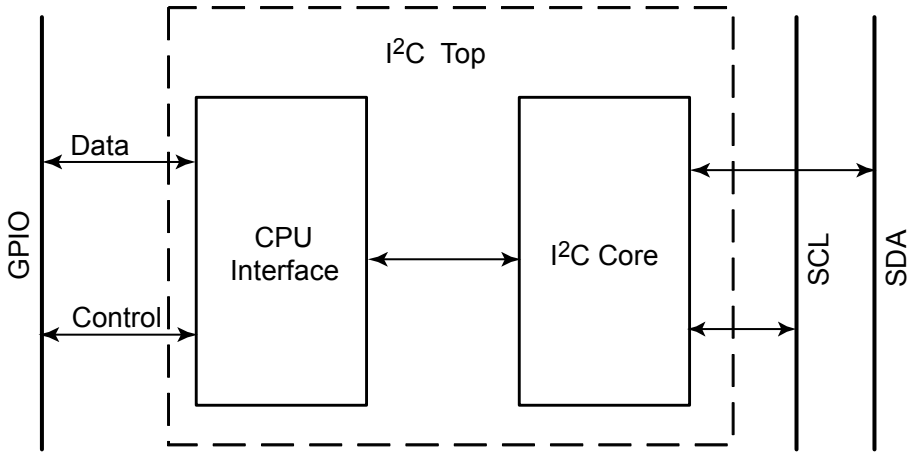


Figure 29: I²C Interface block diagram

8.2 Register Descriptions

The I^2C registers are shown below:

Address	Type	Width	Reset Value	Register Name
0x010040	R/W	8	0x00	I^2C Byte Count
0x010041	R/W	8	0x00	I^2C Control
0x010042	R	8	0x00	I^2C Status
0x010042	W	8	0x00	I^2C Reset
0x010043	R/W	8	0x00	I^2C Slave Address
0x010044 to 0x010053	R/W	8	0x00	I^2C Data

Table 14: I^2C Register Summary

I2C Byte Count

Read/Write MMIO_base + 0x010040

Power-on Default 0x00

7	6	5	4	3	2	1	0
Res				Count R/W			

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3:0	Count	Byte count -1.

I2C Control

Read/Write MMIO_base + 0x010041

Power-on Default 0x00

7	6	5	4	3	2	1	0
Res	Repeat R/W	IntAck R/W	Int R/W	Res	Status R/W	Mode R/W	E R/W

Bit(s)	Name	Description
7	Res	This bit is reserved.
6	Repeat	Repeated Start Enable: 0: Disable. 1: Enable.
5	IntAck	Interrupt Acknowledge: 0: Not acknowledge. 1: Acknowledge.
4	Int	Interrupt Enable: 0: Disable. 1: Enable.
3	Res	This bit is reserved.
2	Status	Start/Stop Status: 0: Stop. 1: Start.
1	Mode	Bus Speed Mode Selection: 0: Standard mode (100kbps). 1: Fast mode (400kbps).
0	E	Controller Enable: 0: Disable. 1: Enable.

I²C Status

Read MMIO_base + 0x010042

Power-on Default 0x00

7	6	5	4	3	2	1	0
Res				Comp R	Err R	Ack R	Busy R

Bit(s)	Name	Description
7:4	Res	These bits are reserved.
3	Comp	Whole Transfer Competed Status: 0: Transfer in progress. 1: Transfer completed.
2	Err	Bus Error Status: 0: Normal. 1: Error.
1	Ack	Slave Acknowledge Received Status: 0: Not received. 1: Received.
0	Busy	Bus Busy: 0: Idle. 1: Busy.

I²C Reset

Write MMIO_base + 0x010042

Power-on Default 0x00

7	6	5	4	3	2	1	0
Res					Err W	Res	

Bit(s)	Name	Description
7:3	Res	These bits are reserved.
2	Err	Bus Error Reset: 0: Clear. 1: Reserved.
1:0	Res	These bits are reserved.

I²C Slave Address

Read/Write MMIO_base + 0x010043

Power-on Default 0x00

7	6	5	4	3	2	1	0
Addr R/W							RW R/W

Bit(s)	Name	Description
7:1	Addr	7-bit Slave Address.
0	RW	Read/Write Selection: 0: Write. 1: Read.

I²C Data

Read/Write MMIO_base + 0x010044 to 0x010053

Power-on Default 0x00

7	6	5	4	3	2	1	0
Data R/W							

Bit(s)	Name	Description
7:0	Data	There are 16 I^2C Data registers that hold the data to be written to or read from the I^2C Slave. These registers can be accessed in 8-bit, 16-bit, or 32-bit mode for very fast FIFO transfer.

9. ZV Port

9.1 Functional Overview

This section covers the ZV Port and the Video Capture Unit.

9.1.1 ZV Port Overview

Incoming video data from the ZV Port can be interlaced or non-interlaced and YUV or RGB format. By disabling the video capture function, the ZV Port can be configured in output mode. In output mode, the ZV Port can send video data and 18-bit graphics in RGB format.

9.1.2 Video Capture Unit Overview

The Video Capture Unit captures incoming video data from the ZV Port and then stores the data into the frame buffer. The Video Capture Unit maintains display quality and balances the capture rate. Its key features are:

- 2-to-1 reduction for horizontal and vertical frame size
- YUV 4:2:2, YUV 4:2:2 with byte swapping, and RGB 5:6:5
- Interlaced data and non-interlaced data capture
- Single buffer and double buffer capture
- Cropping

The SM750 uses the Video Processor block to display captured data on the display (LCD, TV, or CRT). The Video Window displays the captured data. The Video Processor does the stretching, color interpolation, YUV-to-RGB conversion, and color key functions.

9.2 Programmer's Model

Figure 31 shows how this 64kB region in the MMIO space is laid out. It controls the ZV Port capture registers.

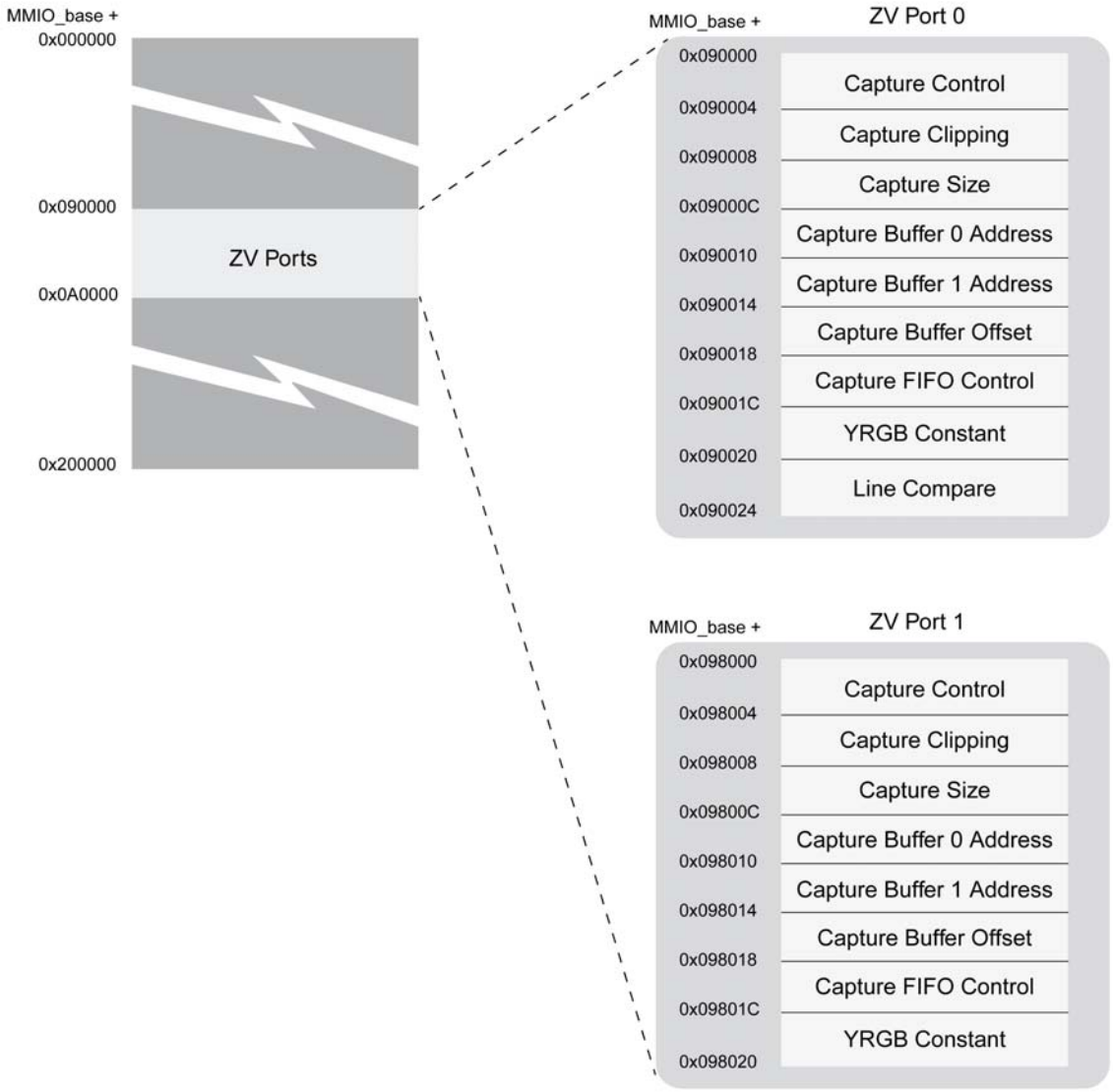


Figure 30: ZV Port Register Space

9.3 Register Descriptions

9.3.1 ZV Port 0 Registers

The ZV Port 0 registers are shown in Table 14.

Offset from MMIO_base	Type	Width	Reset Value[1]	Register Name
0x090000	R/W	32	0b0000.XXXX.0000.0000. 0000.0000.0000.0000	Capture Control
0x090004	R/W	32	Undefined	Capture Clipping
0x090008	R/W	32	Undefined	Capture Size
0x09000C	R/W	32	Undefined	Capture Buffer 0 Address
0x090010	R/W	32	Undefined	Capture Buffer 1 Address
0x090014	R/W	32	Undefined	Capture Buffer Offset
0x090018	R/W	32	0x00000004	Capture FIFO Control
0x09001C	R/W	32	0x00EDEDED	YRGB Constant
0x090020	R/W	32	0x00000000	Line Compare

Table 15: Port 0 Register Summary

1.In the reset values, “X” indicates don’t care.

Capture Control

Read/Write MMIO_base + 0x090000

Power-on Default 0b0000.XXXX.0000.0000.0000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				F R	I R	CB R	VSS R	Res				ADJ R/W	HA R/W	VS R/W	HS R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FD R/W	VP R/W	HP R/W	CP R/W	UVS R/W	BS R/W	CS R/W	CF R/W	FS R/W	W R/W	B R/W	DB R/W	CC R/W	RGB R/W	656 R/W	E R/W

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	F	Field Input Status. This bit is read-only. o: Even field. 1: Odd field.
26	I	Interlace Status. This bit is read-only. 0: Non-interlaced. 1: Interlaced.
25	CB	Current Buffer Status. This bit is read-only. 0: Capturing data into buffer 0. 1: Capturing data into buffer 1.
24	VSS	Vertical Sync Status. This bit is read-only. 0: VSync pulse is inactive. 1: VSync pulse is active.
23:20	Res	These bits are reserved.
19	ADJ	Delay HREF. 0: Do not delay HREF. 1: Delay HREF by one clock.
18	HA	Enable Horizontal Averaging. 0: Disable. 1: Enable.
17	VS	Enable 2÷1 Vertical Shrink. 0: Disable. 1: Enable.
16	HS	Enable 2÷1 Horizontal Shrink. 0: Disable. 1: Enable.
15	FD	Field Detect Method. 0: Rising edge of VSync. 1: Falling edge of VSync.
14	VP	Select VSync Phase. 0: Active high. 1: Active low.
13	HP	Select HRef Phase. 0: Active high. 1: Active low.
12	CP	Select Input Clock Polarity. 0: Active high. 1: Active low.
11	UVS	Enable UV Swap. 0: Disable. 1: Enable.
10	BS	Enable Byte Swap. 0: Disable. 1: Enable.
9	CS	Capture Size. 0: 16-bit. 1: 8-bit.

Bit(s)	Name	Description
8	CF	Capture Format. 0: YUV. 1: RGB.
7	FS	Enable Field Swap. 0: Disable. 1: Enable.
6	W	Enable Interlaced Data Capturing in Weave. 0: Disable. 1: Enable.
5	B	Enable Interlaced Data Capturing in Bob. 0: Disable. 1: Enable.
4	DB	Enable Double Buffering. 0: Disable. 1: Enable.
3	CC	Select Capture Control. 0: Continuous capture. 1: Conditional capture by using the S bit.
2	RGB	Enable YUV to RGB Color Conversion. 0: Disable. 1:Enable.
1	656	Enable 8-bit ITU-656 Input. 0: Disable. 1: Enable.
0	E	Enable Capture. 0: Disable. 1: Enable.

Capture Clipping

Read/Write MMIO_base + 0x090004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res						EYClip R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res						XClip R/W									

Bit(s)	Name	Description
31:26	Res	These bits are reserved.
25:16	EYClip	Number of lines to skip after VSync for even field.
15:10	Res	These bits are reserved.
9:0	XClip	Number of pixels to skip after HRef.

Capture Size

Read/Write MMIO_base + 0x090008

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					Height R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					Width R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	Height	Number of lines to capture.
15:11	Res	These bits are reserved.
10:0	Width	Number of pixels to capture.

Capture Buffer 0 Address

Read/Write MMIO_base + 0x09000C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 0 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer 1 Address

Read/Write MMIO_base + 0x090010

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 1 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer Offset

Read/Write MMIO_base + 0x090014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res						OYClip									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset R/W												0000			

Bit(s)	Name	Description
31:26	Res	These bits are reserved.
25:16	OYClip	Number of lines to skip after VSync for odd field.
15:4	Offset	Number of 128-bit aligned bytes per line of the capture buffer.
3:0	0000	These bits are hardwired to zeros.

Capture FIFO Control

Read/Write MMIO_base + 0x090018

Power-on Default 0x00000004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res													FIFO R/W		

Bit(s)	Name	Description
31:3	Res	These bits are reserved.
2:0	FIFO	FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 000: 2 or more empty. 001: 3 or more empty. 010: 4 or more empty. 011: 5 or more empty. 100: 6 or more empty. 101: 8 or more empty. 110: 10 or more empty. 111: 12 or more empty.

YRGB Constant

Read/Write MMIO_base + 0x09001C

Power-on Default 0x00EDEDED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	B Blue Conversion Constant.

Line Compare

Read/Write MMIO_base + 0x090020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					L-COMP R/W										

Bit(s)	Name	Description
31:11	Res	These bits are reserved.
10:0	L-COMP	Line Compare. The current line number is used to trigger the Primary Display display.

9.3.2 ZV Port 1 Registers

The ZV Port 1 registers are shown in Table 15.

Offset from MMIO_base	Type	Width	Reset Value	Register Name
0x098000	R/W	32	0b0000.XXXX.0000.0000. 0000.0000.0000.0000	Capture Control
0x098004	R/W	32	Undefined	Capture Clipping
0x098008	R/W	32	Undefined	Capture Size
0x09800C	R/W	32	Undefined	Capture Buffer 0 Address
0x098010	R/W	32	Undefined	Capture Buffer 1 Address
0x098014	R/W	32	Undefined	Capture Buffer Offset
0x098018	R/W	32	0x00000004	Capture FIFO Control
0x09801C	R/W	32	0x00EDEDED	YRGB Constant

Table 16: ZV Port 1 Register Summary

Capture Control

Read/Write MMIO_base + 0x098000

Power-on Default 0b0000.XXXX.0000.0000.0000.0000.0000.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				F R	I R	C B	VSS R	Res			Panel R/W	ADJ R/W	HA R/W	VS R/W	HS R/W
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FD R/W	VP R/W	HP R/W	CP R/W	UVS R/W	BS R/W	CS R/W	CF R/W	FS R/W	W R/W	B R/W	DB R/W	CC R/W	RGB R/W	656 R/W	E R/W

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	F	Field Input Status. This bit is read-only. o: Even field. 1: Odd field.
26	I	Interlace Status. This bit is read-only. 0: Non-interlaced. 1: Interlaced.
25	CB	Current Buffer Status. This bit is read-only. 0: Capturing data into buffer 0. 1: Capturing data into buffer 1.
24	VSS	Vertical Sync Status. This bit is read-only. 0: VSync pulse is inactive. 1: VSync pulse is active.
23:21	Res	These bits are reserved.
20	Panel	Enable Capture Panel Output. 0: Disable. 1: Enable.
19	ADJ	Delay HREF. 0: Do not delay HREF. 1: Delay HREF by one clock.
18	HA	Enable Horizontal Averaging. 0: Disable. 1: Enable.
17	VS	Enable 2÷1 Vertical Shrink. 0: Disable. 1: Enable.
16	HS	Enable 2÷1 Horizontal Shrink. 0: Disable. 1: Enable.
15	FD	Field Detect Method. 0: Rising edge of VSync. 1: Falling edge of VSync.
14	VP	Select VSync Phase. 0: Active high. 1: Active low.
13	HP	Select HRef Phase. 0: Active high. 1: Active low.
12	CP	Select Input Clock Polarity. 0: Active high. 1: Active low.
11	UVS	Enable UV Swap. 0: Disable. 1: Enable.
10	BS	Enable Byte Swap. 0: Disable. 1: Enable.

Bit(s)	Name	Description
9	CS	Capture Size. 0: 16-bit. 1: 8-bit.
8	CF	Capture Format. 0: YUV. 1: RGB.
7	FS	Enable Field Swap. 0: Disable. 1: Enable.
6	W	Enable Interlaced Data Capturing in Weave. 0: Disable. 1: Enable.
5	B	Enable Interlaced Data Capturing in Bob. 0: Disable. 1: Enable.
4	DB	Enable Double Buffering. 0: Disable. 1: Enable.
3	CC	Select Capture Control. 0: Continuous capture. 1: Conditional capture by using the S bit.
2	RGB	Enable YUV to RGB Color Conversion. 0: Disable. 1:Enable.
1	656	Enable 8-bit ITU-656 Input. 0: Disable. 1: Enable.
0	E	Enable Capture. 0: Disable. 1: Enable.

Capture Clipping

Read/Write MMIO_base + 0x098004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res						EYClip R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res						XClip R/W									

Bit(s)	Name	Description
31:26	Res	These bits are reserved.
25:16	EYClip	Number of lines to skip after VSync for even field.
15:10	Res	These bits are reserved.
9:0	XClip	Number of pixels to skip after HRef.

Capture Size

Read/Write MMIO_base + 0x098008

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res					Height R/W										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					Width R/W										

Bit(s)	Name	Description
31:27	Res	These bits are reserved.
26:16	Height	Number of lines to capture.
15:11	Res	These bits are reserved.
10:0	Width	Number of pixels to capture.

Capture Buffer 0 Address

Read/Write MMIO_base + 0x09800C

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory
25:4	Memory Address	Memory address of capture buffer 0 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer 1 Address

Read/Write MMIO_base + 0x098010

Power-on Default Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S R/W	Res			Ext R/W	CS R/W	Memory Address R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Memory Address R/W												0000			

Bit(s)	Name	Description
31	S	Status Bit. 0: Flip not pending. 1: Flip pending.
30:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: External memory.
26	CS	Chip Select for External Memory. 0: CS0 of external memory. 1: CS1 of external memory.
25:4	Memory Address	Memory address of capture buffer 1 with 128-bit alignment.
3:0	0000	These bits are hardwired to zeros.

Capture Buffer Offset

Read/Write MMIO_base + 0x098014

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res						OYClip R/W									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Offset R/W												0000			

Bit(s)	Name	Description
31:26	Res	These bits are reserved.
25:16	OYClip	Number of lines to skip after VSync for odd field.
15:4	Offset	Number of 128-bit aligned bytes per line of the capture buffer.
3:0	0000	These bits are hardwired to zeros.

Capture FIFO Control

Read/Write MMIO_base + 0x098018

Power-on Default 0x00000004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res													FIFO R/W		

Bit(s)	Name	Description
31:3	Res	These bits are reserved.
2:0	FIFO	FIFO Request Level. When the FIFO empty level reaches the level specified, a FIFO read request will be generated. 000: 2 or more empty. 001: 3 or more empty. 010: 4 or more empty. 011: 5 or more empty. 100: 6 or more empty. 101: 8 or more empty. 110: 10 or more empty. 111: 12 or more empty.

YRGB Constant

Read/Write MMIO_base + 0x09801C

Power-on Default 0x00EDEDED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Y R/W								R R/W							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G R/W								B R/W							

Bit(s)	Name	Description
31:24	Y	Y Adjustment.
23:16	R	Red Conversion Constant.
15:8	G	Green Conversion Constant.
7:0	B	B Blue Conversion Constant.

10. DMA Controller (DMAC)

10.1 Functional Overview

In the SM750, the Display Controller, Command Interpreter, Draw Engine, and DMA can access system memory through the on-chip system memory controller (see Figure 32).

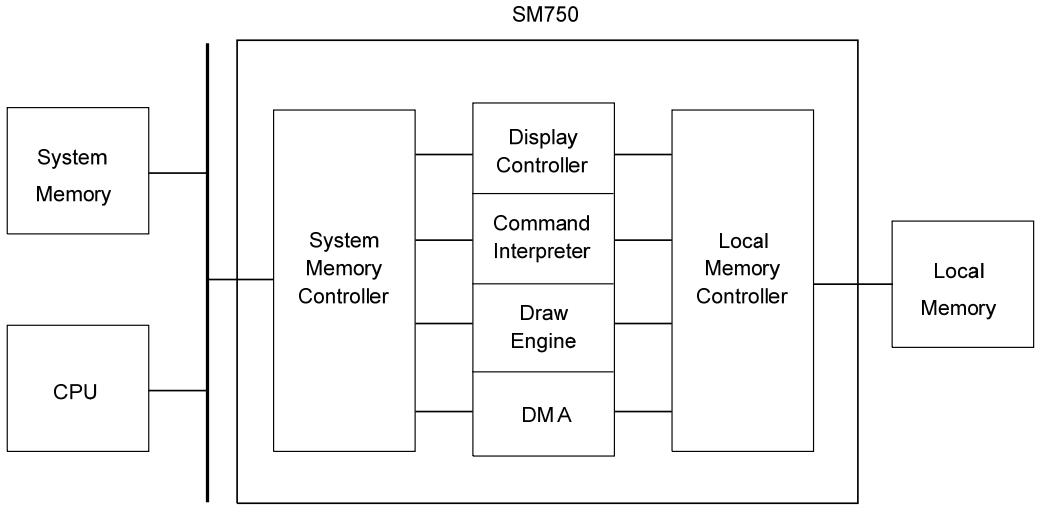


Figure 31: SM750 Functional Block Connections to Memory Controllers

The DMA channel within the SM750 handles memory data transfers, thus offloading the CPU. The DMA channel moves data between internal and system memory.

- DMA1 – Moves data between system memory and local memory (see Figure 33)
  There are four ways to transfer data in DMA1:
  - System memory to system memory
  - System memory to local memory
  - Local memory to system memory
  - Local memory to local memory

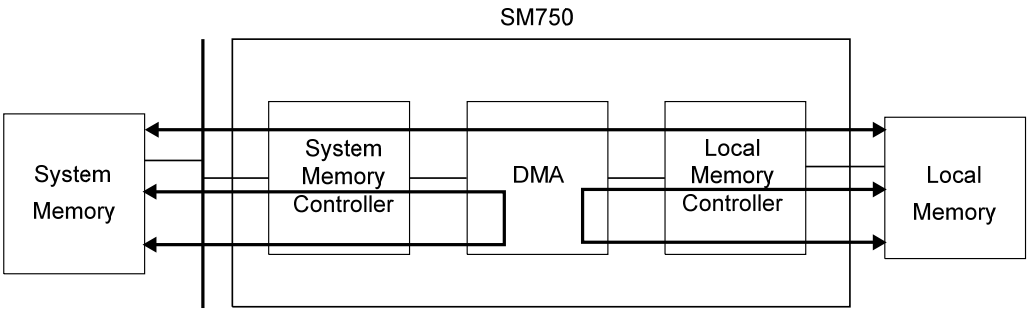
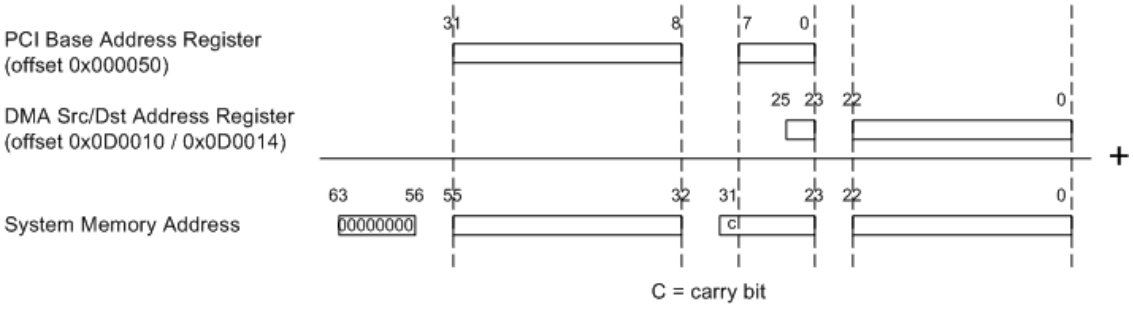


Figure 32: DMA Channel 1

System Memory Addressing Mechanism

When DMA uses bus master to access system memory, it uses the following decoding method:

SM750 DMA Addressing Method



10.2 Register Descriptions

Figure 34 shows how this 64kB region in the MMIO space is laid out. It controls the DMA registers.

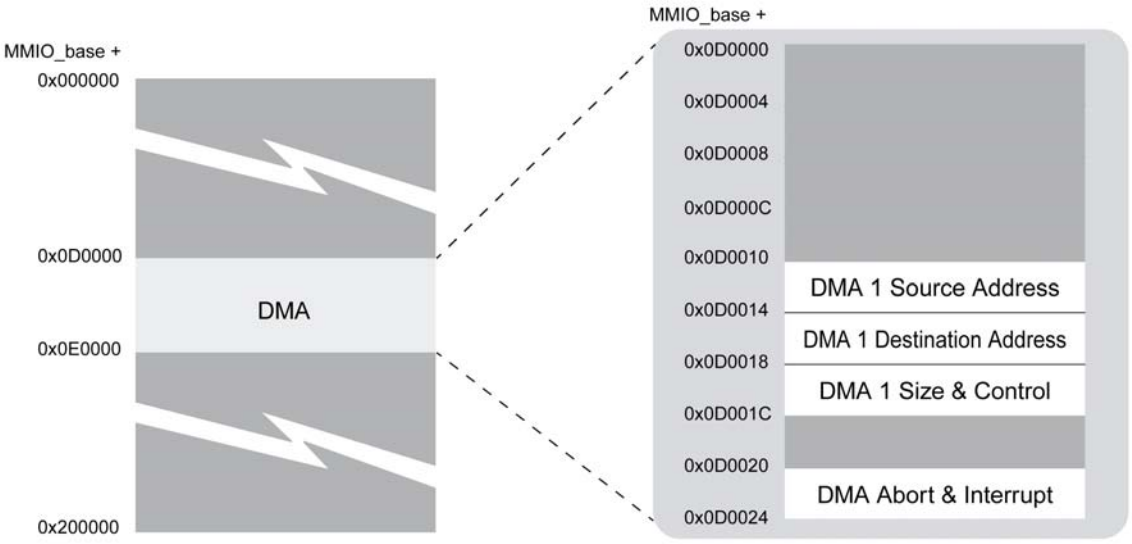


Figure 33: DMA Register Space

Table 16 shows the DMA Controller registers.

Offset from MMIO_base	Type	Width	Reset Value	Register Name
0x0D0010	R/W	32	0x00000000	DMA 1 Source Address
0x0D0014	R/W	32	0x00000000	DMA 1 Destination Address
0x0D0018	R/W	32	0x00000000	DMA 1 Size & Control
0x0D0020	R/W	32	0x00000000	DMA Abort & Interrupt

Table 17: DMA Controller Register Summary

DMA 1 Source Address

Read/Write MMIO_base + 0x0D0010

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W														00	

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:2	Memory Address	Memory address with 32-bit alignment.
1:0	00	00 These bits are hardwired to zeros.

DMA 1 Destination Address

Read/Write MMIO_base + 0x0D0014

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res				Ext R/W	CS R/W	Memory Address R/W									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Address R/W														00	

Bit(s)	Name	Description
31:28	Res	These bits are reserved.
27	Ext	Memory Selection. 0: Local memory. 1: System memory.
26	CS	Chip Select for System Memory. 0: CS0 of system memory. 1: CS1 of system memory.
25:2	Memory Address	Memory address with 32-bit alignment.
1:0	00	00 These bits are hardwired to zeros.

DMA 1 Size & Control

Read/Write MMIO_base + 0x0D0018

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Act R/W	Res							Size R/W							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Size R/W														00	

Bit(s)	Name	Description
31	Act	DMA Channel 1 Activation. The Act bit will be cleared to “0” by the hardware when the DMA is finished. 0: Idle. 1: Activate DMA channel 1.
30:24	Res	These bits are reserved.
23:2	Size	Number of 32-bit aligned bytes to transfer (up to 16MB).
1:0	00	These bits are hardwired to zeros.

DMA Abort & Interrupt

Read/Write MMIO_base + 0x0D0020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Res										$Abort_{1:0}$ R/W		Res		$Int_{1:0}$ R/W	

Bit(s)	Name	Description
31:6	Res	These bits are reserved.
5:4	$Abort_{1:0}$	Enable or Abort DMA Channel. Aborting will reset the corresponding DMA controller. For normal operation, the Abort bits should be set to “0”. 0: Enable corresponding DMA channel. 1: Abort corresponding DMA channel.
3:2	Res	These bits are reserved.
1:0	$Int_{1:0}$	Interrupt Status Bit. The Int bit should be cleared to “0” by software when the interrupt has been serviced. Writing a “1” has no effect. 0: DMA is not active or still busy – no interrupt. 1: DMA is finished – interrupt.

11. PWM Specification

11.1 Functional Overview

The Pulse Width Modulation (PWM) module is a simple counter that can pulse with programmable pulse widths. The pulse optionally can be tied to the PWM interrupt signal to generate a periodic interrupt for timing or watchdog support. The input clock is the peripheral clock at 96 MHz. The output pulse starts high.

The following subsections provide some different samples of PWM usage.

11.1.1 Delay Counter with Interrupt

Any of the three available PWM circuits can be programmed to perform a single shot delay. Once the delay is finished, an interrupt is triggered. The required delay is assumed to be 20 ms.

The values for the PWM n register are calculated as follows:

- Delay * clock = 20 ms * 96 MHz = 1,920,000
- A 50% duty cycle means 960,000 clocks are LOW and 960,000 clocks are HIGH
- The shift to a 12-bit value is done by dividing by 2^8: (3,750 – 1) clocks LOW and (3,750 – 1) clocks HIGH
- The value for the PWM n register is: 0xEA5EA585

11.1.2 Internal Timer with Interrupt

Any of the three available PWM circuits can be programmed to act as a periodic timer to support a clock. The periodic timer generates an interrupt after each cycle. The required periodic interval is assumed to be 1 s. For this example, there is a 30/70% duty cycle.

The values for the PWM n register are calculated as follows:

- Delay * clock = 1 s * 96 MHz = 96,000,000
- A 30% duty cycle means 28,800,000 clocks are LOW and 67,200,000 clocks are HIGH
- The shift to a 12-bit value is done by dividing by 2^{15}: (879 – 1) clocks LOW and (2,051 – 1) clocks HIGH
- The value for the PWM n register is: 0x80236EF5

11.1.3 External Pulse

In this example, the PWM is programmed for an external pulse with a frequency of 44.1 kHz and a duty cycle of 15%.

The values for the PWM n register are calculated as follows:

- Delay * clock = (1 / 44.1 kHz) * 96 MHz = 2,177
- A 15% duty cycle means (327 – 1) clocks are LOW and (1,850 – 1) clocks are HIGH
- The value for the PWM n register is: 0x73914601

11.2 Register Descriptions

The PWM registers are shown in Table 17.

Offset from MMIO_base	Type	Width	Reset Value	Register Name
0x010020	R/W	32	0x00000000	PWM 0
0x010024	R/W	32	0x00000000	PWM 1
0x010028	R/W	32	0x00000000	PWM 2

Table 18: PWM Register Summary

The PWM registers control the three PWM pins. It contains three registers, one for each PWM pin. Figure 35 defines the register layout for the PWM registers.

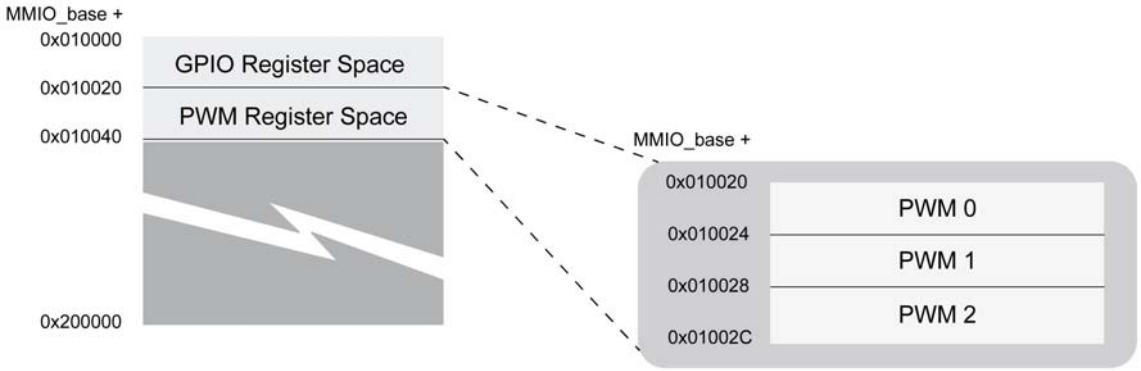


Figure 34: PWM Register Space

PWM 0

Read/Write Address 0x010020

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Low Counter R/W								Clock Divide R/W				IP R/W	I R/W	Res	E R/W

Bit(s)	Name	Description
31:20	High Counter	Number of clocks – 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks – 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96 MHz input clock.
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a “1” in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	Enable or Disable the PWM. 0: Disabled. 1: Enabled.

0000	÷1	96 MHz	1000	÷256	375 kHz
0001	÷2	48 MHz	1001	÷512	187.5kHz
0010	÷4	24 MHz	1010	÷1,024	93.75 kHz
0011	÷8	12 MHz	1011	÷2,048	46.875 kHz
0100	÷16	6 MHz	1100	÷4,096	23.438 kHz
0101	÷32	3 MHz	1101	÷8,192	11.719 kHz
0110	÷64	1.5 MHz	1110	÷16,384	5.859 kHz
0111	÷128	750 kHz	1111	÷32,768	2.93 kHz

PWM 1

Read/Write Address 0x010024

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Low Counter R/W								Clock Divide R/W				IP R/W	I R/W	Res	E R/W

Bit(s)	Name	Description
31:20	High Counter	Number of clocks – 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks – 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96 MHz input clock.
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a “1” in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	0 E Enable or Disable the PWM. 0: Disabled. 1: Enabled.

0000	÷1	96 MHz	1000	÷256	375 kHz
0001	÷2	48 MHz	1001	÷512	187.5kHz
0010	÷4	24 MHz	1010	÷1,024	93.75 kHz
0011	÷8	12 MHz	1011	÷2,048	46.875 kHz
0100	÷16	6 MHz	1100	÷4,096	23.438 kHz
0101	÷32	3 MHz	1101	÷8,192	11.719 kHz
0110	÷64	1.5 MHz	1110	÷16,384	5.859 kHz
0111	÷128	750 kHz	1111	÷32,768	2.93 kHz

PWM 2

Read/Write Address 0x010028

Power-on Default 0x00000000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
High Counter R/W												Low Counter R/W			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Low Counter R/W								Clock Divide R/W				IP R/W	I R/W	Res	E R/W

Bit(s)	Name	Description
31:20	High Counter	Number of clocks – 1 the PWM should remain high before switching to low.
19:8	Low Counter	Number of clocks – 1 the PWM should remain low before switching to high.
7:4	Clock Divide	Select divisor for 96 MHz input clock.
3	IP	PWM Interrupt Pending. In order to clear a pending interrupt, write a “1” in the IP bit. 0: No interrupt pending. 1: Interrupt pending.
2	I	Enable or Disable PWM Interrupt. 0: Disable PWM interrupt. 1: Enable PWM interrupt whenever a single cycle is completed.
1	Res	This bit is reserved.
0	E	Enable or Disable the PWM. 0: Disabled. 1: Enabled.

0000	÷1	96 MHz	1000	÷256	375 kHz
0001	÷2	48 MHz	1001	÷512	187.5kHz
0010	÷4	24 MHz	1010	÷1,024	93.75 kHz
0011	÷8	12 MHz	1011	÷2,048	46.875 kHz
0100	÷16	6 MHz	1100	÷4,096	23.438 kHz
0101	÷32	3 MHz	1101	÷8,192	11.719 kHz
0110	÷64	1.5 MHz	1110	÷16,384	5.859 kHz
0111	÷128	750 kHz	1111	÷32,768	2.93 kHz

12. Specifications

12.1 Soldering Profile

Figure 36 shows the soldering profile for the SM750 device. This profile is designed for use with Sn63 or Sn62 (tin measurements in the PCB) and can serve as a general guideline in establishing a reflow profile.

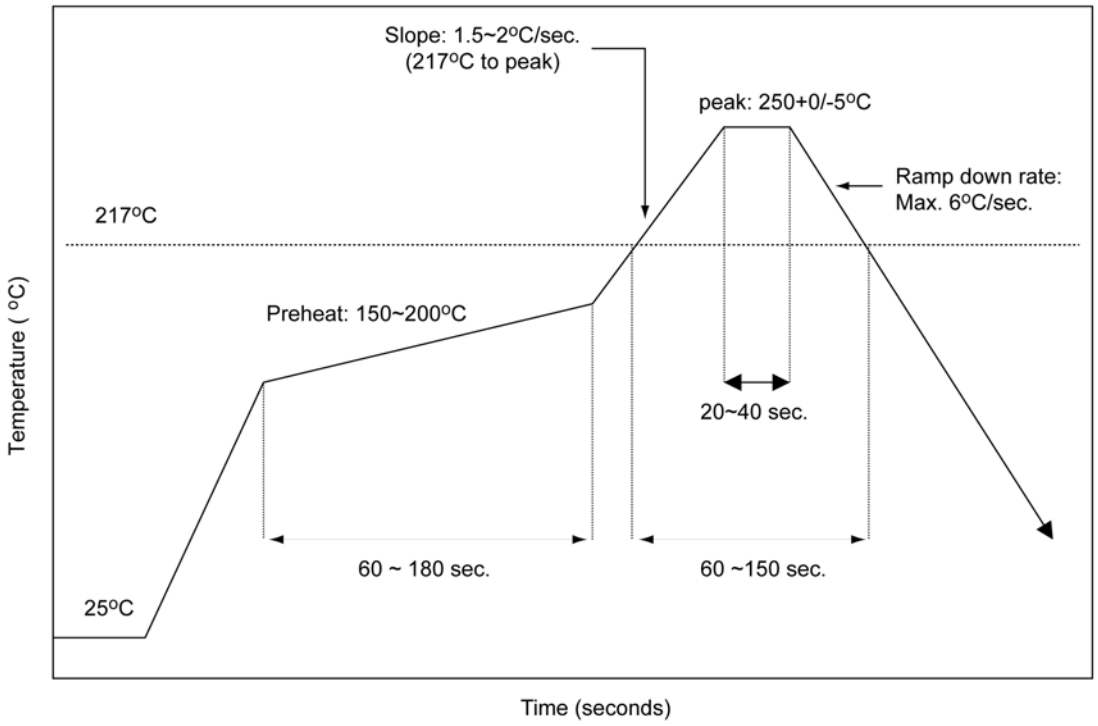


Figure 35: Temperature Profile

The reflow profile is defined as follows:

- Average ramp-up rate (217°C to peak): 1.5~2°C/second
- Preheat (150~200°C): 60~180 seconds
- Temperature maintained above 217°C: 60~150 seconds
- Time within 5°C of actual peak temperature: 20 ~ 40 seconds
- Peak temperature: 250+0/-5°C
- Ramp-down rate: 6°C/second max.
- Time 25°C to peak temperature: 8 minutes max.
- Cycle interval: 5 minutes

12.2 DC Characteristics

Parameter	Min	Typ	Max	Unit
Operation Temperature	0		75	˚C
VDD I/O[1] with respect to VSS	3.125	3.3	3.465	V
VDD core with respect to VSS	1.14	1.2	1.26	V
MVDD/MVDD2	2.375	2.5	2.625	V
Voltage on I/O pins with respect to VSS	-0.5		VDD + 5%	V

Table 19: Recommend Operating Condition

1.VDD I/O refers to AVDD, GVDD, HVDD, PVDD, and XTALPWR.

Parameter	Max	Unit
VDD I/O[1] with respect to VSS	3.3 +/- 5%	V
VDD core with respect to VSS	1.2 +/- 5%	V
MVDD/MVDD2	2.5 +/- 5%	V
ESD Rating (Human Body), all signal pins	> 2000	V
ESD Rating (Human Body), all VDD pins (AVDD,PVDD,VDD)	> 1500	V
Voltage on I/O pins with respect to VSS	-0.5V to VDD + 5%	V

Table 20: Absolute Maximum Ratings

1.VDD I/O refers to AVDD, GVDD, HVDD, PVDD, and XTALPWR.

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage	-0.3	0.8	V
V_{IH}	Input High Voltage	2.4	5.5	V
V_{OL}	Output Low Voltage	–	0.4	V
V_{OH}	Output High Voltage	2.8	VDD + 0.5	V
I_{OZL}	Output 3-State Current	–	10	µA
I_{OZH}	Output 3-State Current	–	10	µA
I_{OZL} (pull up pins)	Output 3-State Current	-130	-10	µA
I_{OZH} (pull up pins)	Output 3-State Current	–	10	µA
I_{OZL} (pull down pins)	Output 3-State Current	–	10	µA
I_{OZH} (pull down pins)	Output 3-State Current	10	130	µA
C_{IN}	Input Capacitance	–	7	pF
C_{OUT}	Output Capacitance	–	7	pF

Table 21: DC Characteristics

12.3 AC Timing

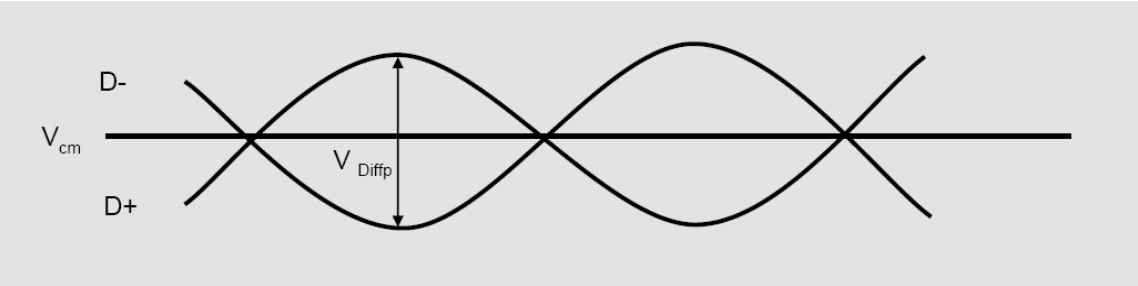
This section provides the AC timing waveforms and parameters:

- "PCI Express Timing"
- "Display Controller Timing"
- "ZV Port Timing"
- "Local DDR Timing"

12.3.1 PCI Express Timing

Transmitter Differential Peak voltage (V Diffp) = 0.4 – 0.6 V

Transmitter Common Mode voltage (V cm) = 0 – 3.6 V



12.3.2 Display Controller Timing

Color TFT Interface

Figure 37 shows the timing waveforms for the FP and FP_DISP signals. Figure 63 shows the timing waveforms for the FP_HSYNC and FP_VSYNC signals. Table 21 lists the AC timing values for the parameters shown in the two figures.

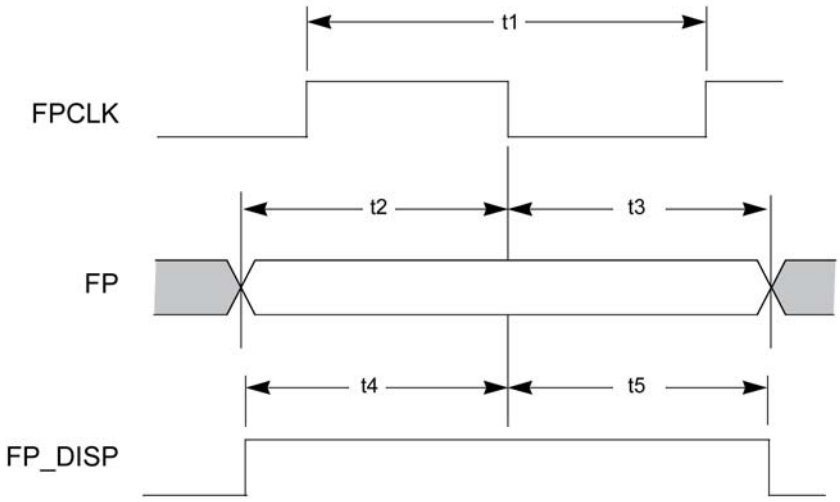
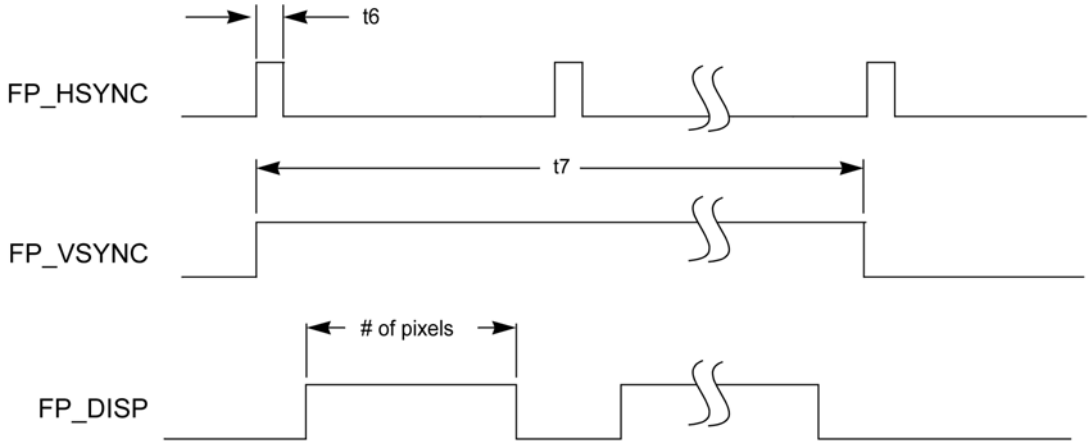


Figure 36: FP and FP_DISP Timing



Note: Number of pixels is programmed in the Panel Horizontal Total register, bits [11:0] (see "Panel Horizontal Total" on page 5-15).

Figure 37: FHSYNC and FVSYNC Timing

Symbol	Parameter	Min	Max	Unit
t1	TFT FPCLK cycle time	12		ns
t2	FP setup to FPCLK falling edge	0.5*T[1] – 2		ns
t3	FP hold from FPCLK falling edge	0.5*T – 2		ns
t4	FP_DISP setup to FPCLK falling edge	0.5*T – 2		ns
t5	FP_DISP hold from FPCLK falling edge	0.5*T – 2		ns
t6	FP_HSYNC pulse width	8	16	T
t7	FP_VSYNC pulse width	1		FP_HSYNC

Table 22: Color TFT Interface Timing Parameters

1.T is pixel clock rate on LCD.

12.3.3 ZV Port Timing

Figure 39 depicts the relationship amongst the ZV Port signals. Table 20 shows the AC parameters associated with the ZV Port signals when the ZV Port custom interface is in use at 50 MHz.

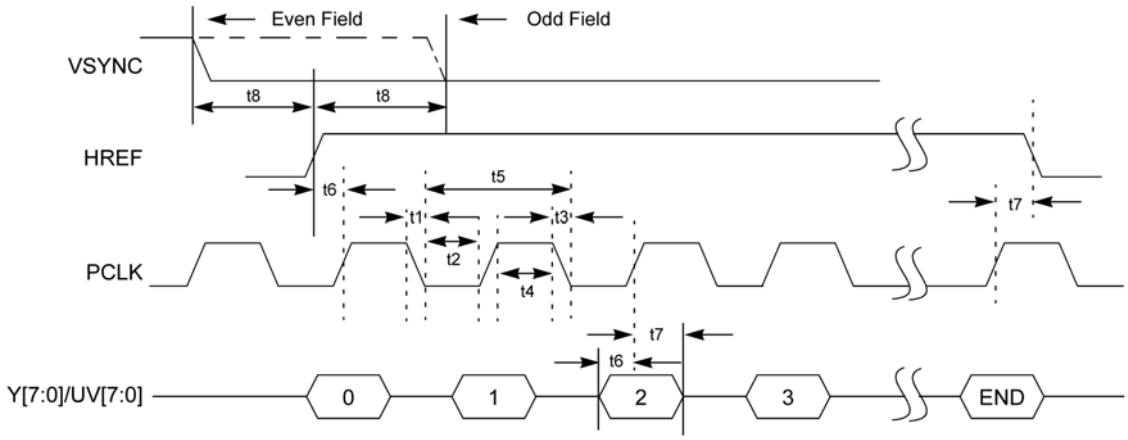


Figure 38: ZV Port Timing

Symbol	Parameter	Min	Max	Unit
t1	PCLK fall time	2		ns
t2	PCLK low time	7		ns
t3	PCLK rise time	2		ns
t4	PCLK high time	7		ns
t5	PCLK cycle time	20		ns
t6	Y[7:0] / UV[7:0] / HREF setup time	10		ns
t7	Y[7:0] / UV[7:0] / HREF hold time	3		T
t8	VSYNC setup / hold time to HREF	30		ns

Table 23: ZV Port Timing Parameters

Notes: All video signals have minimum rise and fall times of 4 ns and maximum rise and fall times of 8 ns. Non-interlaced data asserts VSYNC at the Odd Field timing.

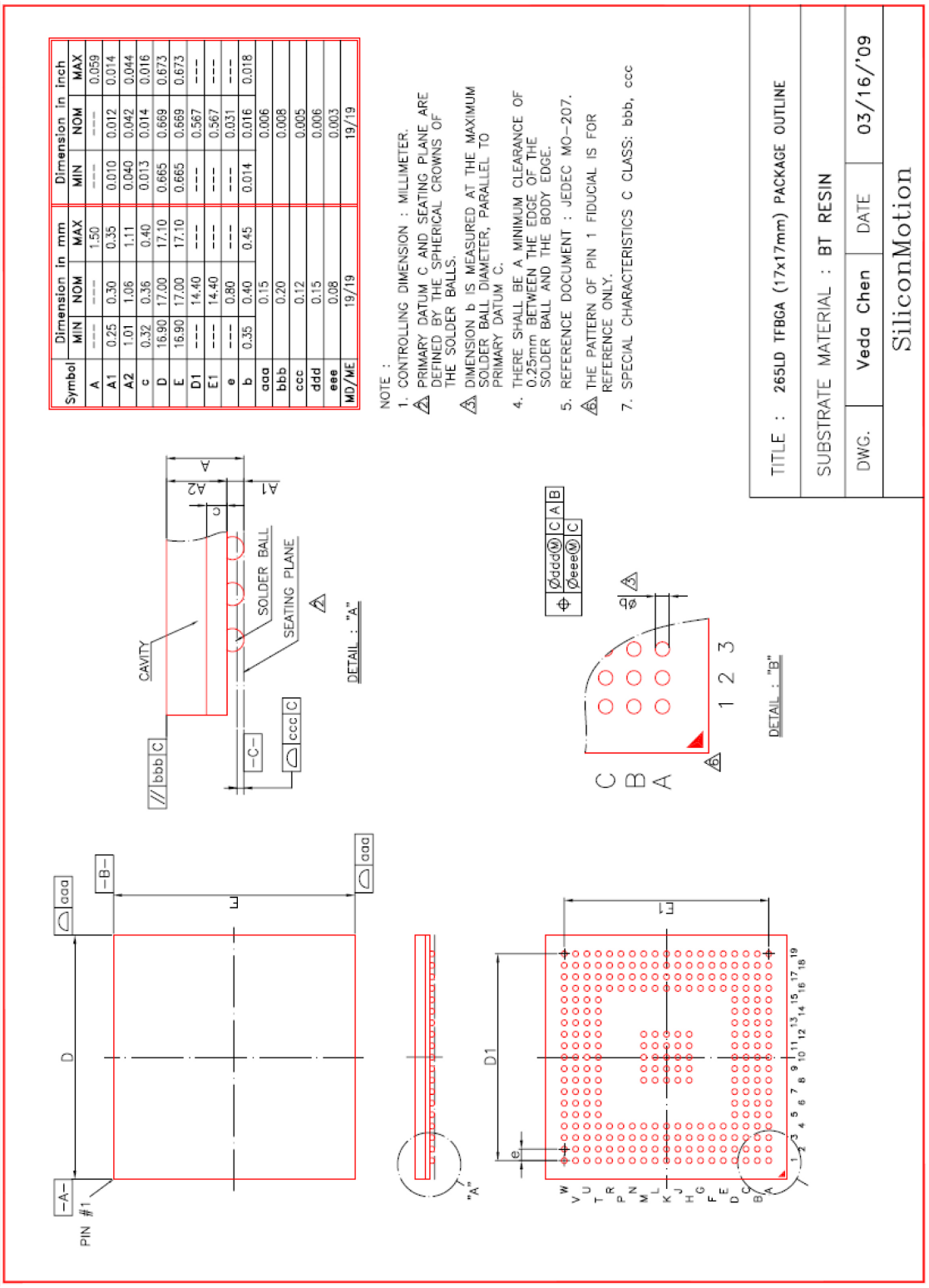
12.3.4 Local DDR Timing

Please refer to the application note “SM750 DDR Req” for details about the DDR timing and requirement.

13. Packaging Information

13.1 Packaging

The SM750 is available in a 265-pin BGA package. The total package size is 17mm x 17mm.



13.2 Top Marking

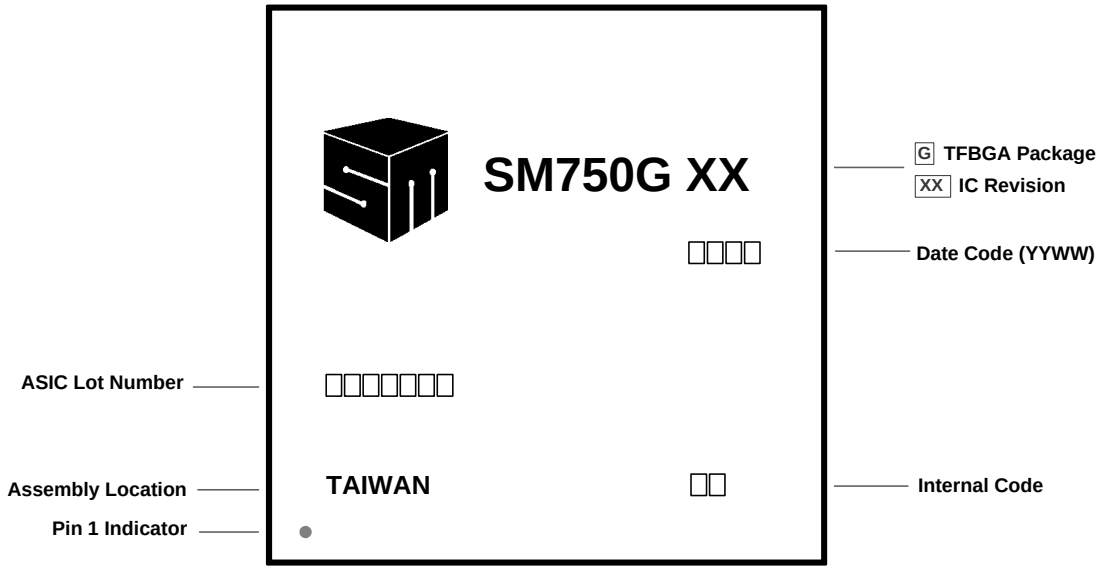


Figure 39: SM750 0MB IC Marking (Commercial version)

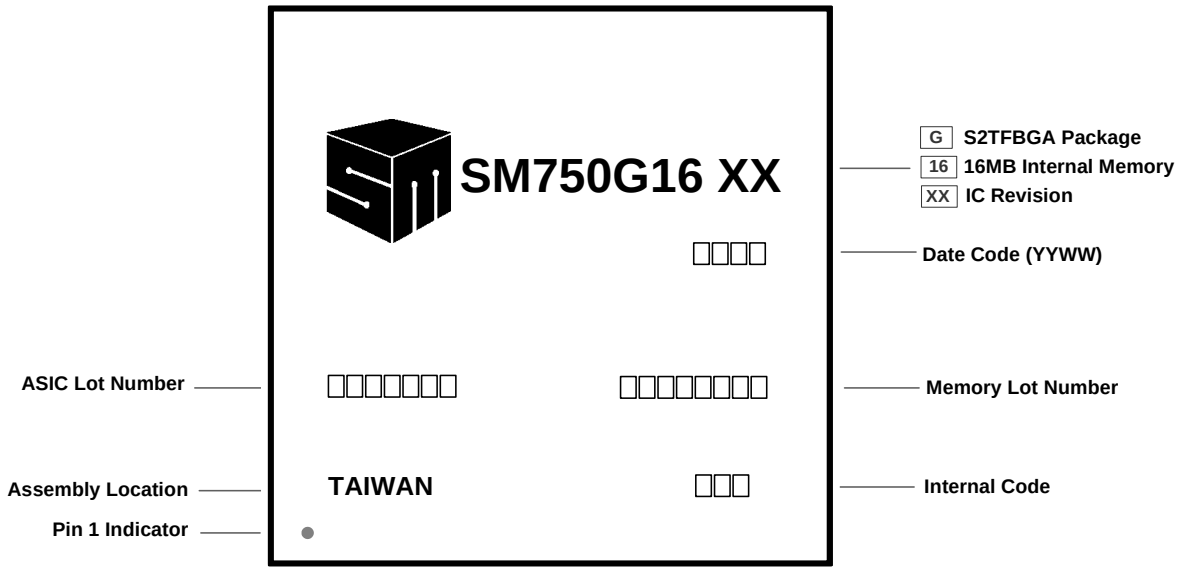


Figure 40: SM750 16MB IC Marking (Commercial version)

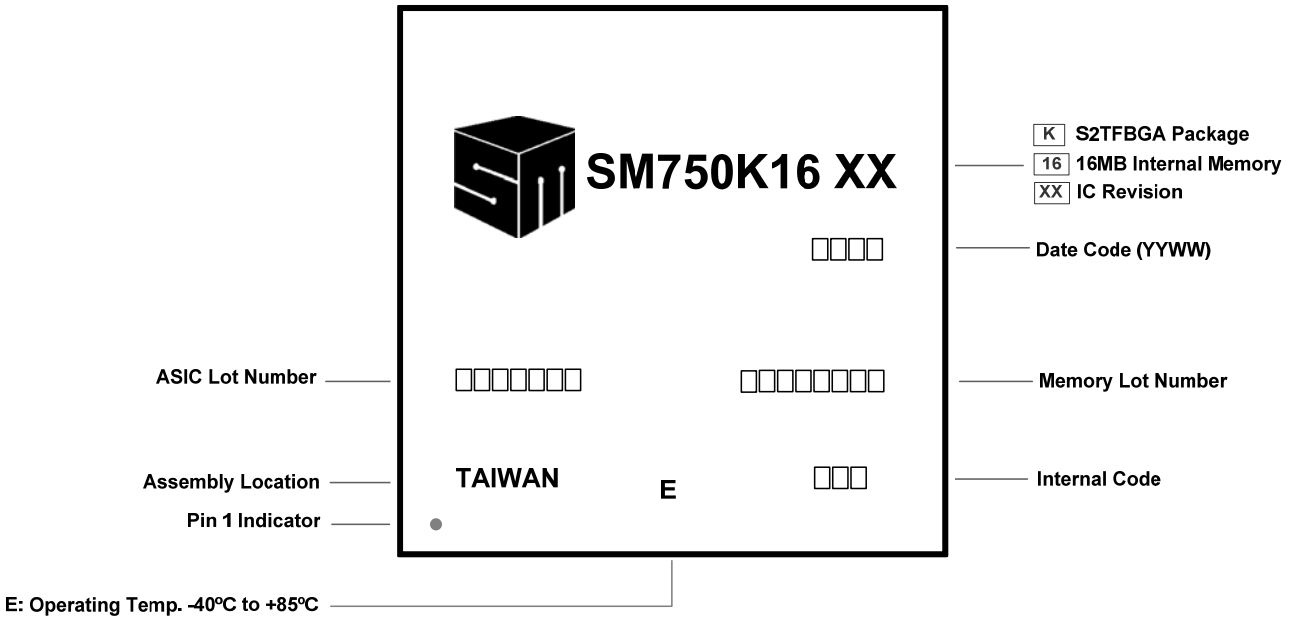


Figure 41: SM750 16MB IC Marking (Industrial version)

14. Product Ordering Information

Part Number	Internal Memory	Operating Temperature	Package Type
SM750GX000000-XX	N/A	0°C ~+70°C	TFBGA 265 pins (17mm x 17mm)
SM750GX160000-XX	16MB DDR	0°C ~+70°C	S2TFBGA 265 pins (17mm x 17mm)
SM750KE160000-XX	16MB DDR	-40°C ~+85°C	S2TFBGA 265 pins (17mm x 17mm)

Note: The suffix “XX” denotes the IC revision.