SM802141

ClockWorks™ Selectable 62.5MHz, 125MHz, 156.25MHz and 312.5MHz Ultra-Low Jitter, LVPECL Frequency Synthesizer

General Description

The SM802141 is a part of Micrel's ClockWorks™ family of devices and provides an extremely low-noise timing solution for Ethernet clock signals.

The device operates from a 3.3V or 2.5V power supply and synthesizes differential LVPECL output clocks at 62.5MHz, 125MHz, 156.25MHz or 312.5MHz, selectable through logic control pins. The SM802141 accepts a 25MHz crystal or LVCMOS reference clock.

Data sheet and support documentation can be found on Micrel's web site at: www.micrel.com.

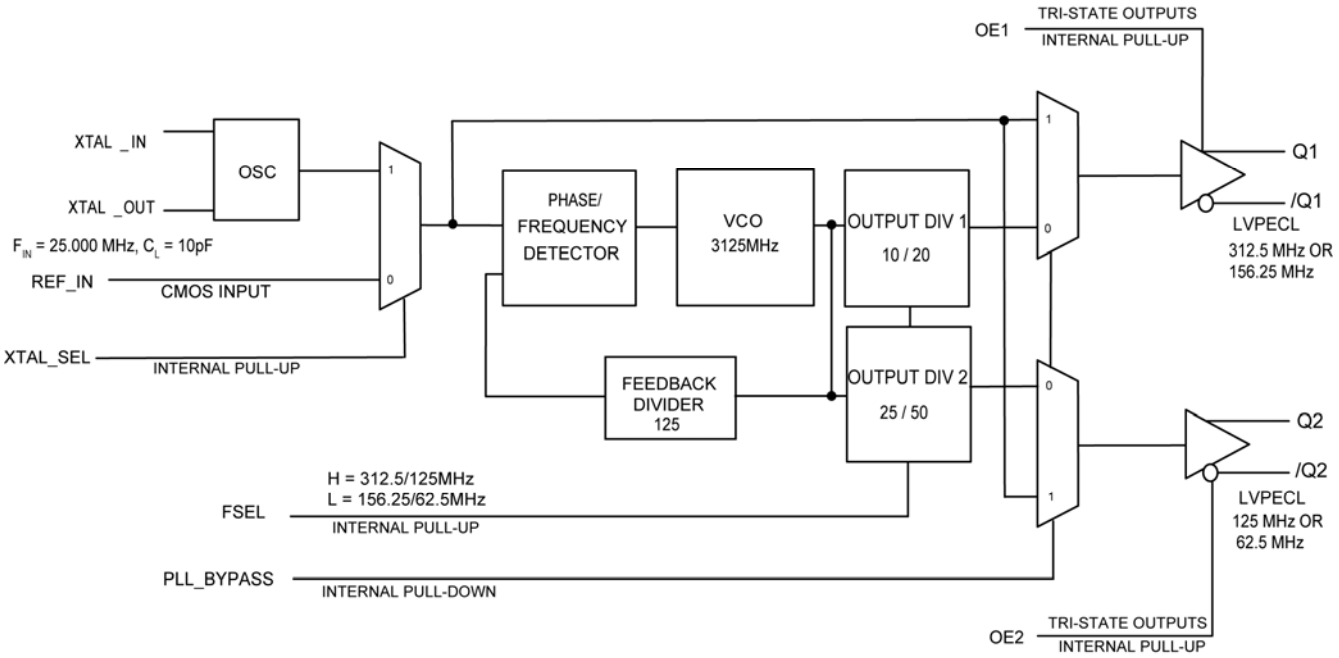
Features

- Configurable to generate up to four different LVPECL clock frequencies
- 2.5V or 3.3V operating range
- Typical phase jitter @ 125MHz (12kHz to 20MHz): 255 fs_{rms}
- Industrial temperature range (–40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 24-pin 4mm × 4mm QFN package

Applications

- Ethernet PHY
- Storage networking (SAN, NAS)

Block Diagram



ClockWorks is a trademark of Micrel, Inc.

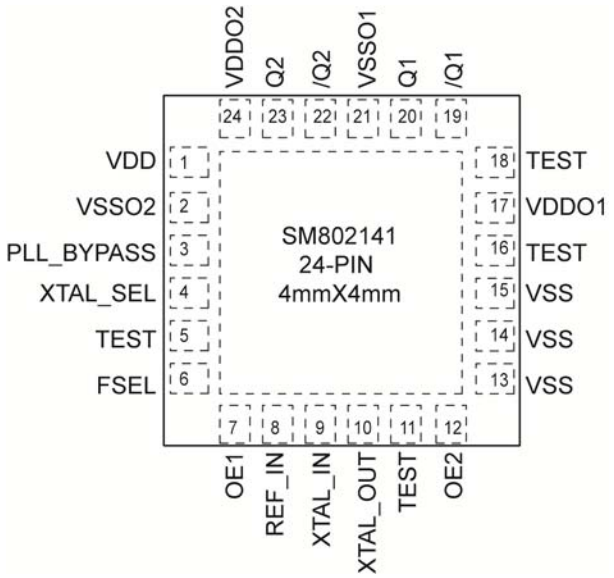
Ordering Information[1]

Part Number	Marking	Shipping	Temperature Range	Package
SM802141UMG	802141	Tube	–40°C to +85°C	24-Pin QFN
SM802141UMGTR	802141	Tape and Reel	–40°C to +85°C	24-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



24-Pin QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
19, 20	/Q1, Q1	O, (DIF)	LVPECL	Differential Clock Output from Bank 1, 156.25MHz or 312.5MHz.
22, 23	/Q2, Q2	O, (DIF)	LVPECL	Differential Clock Output from Bank 2, 62.5MHz or 125MHz.
24	VDDO2	PWR		Power Supply for Output Bank 2.
2	VSSO2	PWR		Power Supply Ground for Output Bank 2.
3	PLL_BYPASS	I, (SE)	LVCMOS	PLL Bypass, Selects Output Source, 0 = Normal PLL Operation, 1 = Output from Input Reference Clock or Crystal 45KΩ pull-down.
4	XTAL_SEL	I, (SE)	LVCMOS	Selects PLL Input Reference Source (0 = REF_IN, 1 = XTAL, 45KΩ pull-up).

Pin Description (Continued)

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
5, 11, 16, 18	TEST			Factory test pins. Do not connect anything to these pins.
1	VDD	PWR		Core Power Supply .
13, 14, 15	VSS (Exposed Pad)	PWR		Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
17	VDDO1	PWR		Power Supply for Output Bank 1.
21	VSSO1	PWR		Power Supply Ground for Output Bank 1.
8	REF_IN	I, (SE)	LVCMOS	Reference Clock Input.
9	XTAL_IN	I, (SE)	XTAL	Crystal Reference Input. No load caps needed (see Figure 5).
10	XTAL_OUT	O, (SE)	XTAL	Crystal Reference Output. No load caps needed (see Figure 5).
6	FSEL	I, (SE)	LVCMOS	Frequency Select, 1 = 312.5/125 MHz, 0 = 156.25/62.5MHz, 45KΩ pull-up.
7	OE1	I, (SE)	LVCMOS	Output Enable, Q1 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ pull-up.
12	OE2	I, (SE)	LVCMOS	Output Enable, Q2 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ pull-up.

Truth Table

PLL_BYPASS	XTAL_SEL	OE1	OE2	INPUT	OUTPUT
0	–	1	1	–	PLL
1	–	1	1	–	XTAL/REF_IN
–	0	1	1	REF_IN	–
–	1	1	1	XTAL	–
–	–	0	1	–	Q1 Tri-State
–	–	1	0	–	Q2 Tri-State

Output Selection Table

XTAL_SEL	PLL_Bypass	F SEL	OE1	OE2	Div 1	Div 2	Q1	Q2
L	H	x	H	L	x	x	Reference Input	Hi-Z
H (Default)	H	x	H	L	x	x	25	Hi-Z
H (Default)	L (Default)	H (Default)	H	L	10	25	312.5	Hi-Z
H (Default)	L (Default)	H (Default)	L	H	10	25	Hi-Z	125
H (Default)	L (Default)	L	H	L	20	50	156.25	Hi-Z
H (Default)	L (Default)	L	L	H	20	50	Hi-Z	62.5

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s) ..... 260°C
Case Temperature ..... 115°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[3]
QFN (θ_{JA})
Still-Air ..... 50°C/W
QFN (ψ_{JB})
Junction-to-Board ..... 30°C/W

DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1, 2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5% & $V_{DDO1,2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, $V_{DDO1/2}$	2.5V Operating Voltage		2.375	2.5	2.625	V
V_{DD}, $V_{DDO1/2}$	3.3V Operating Voltage		3.135	3.3	3.465	V
I_{DD} XTAL	Supply Current V_{DD} + V_{DDO} XTAL_SEL = 1 Outputs Open	62.5MHz; 1 output enabled		80		mA
		125MHz; 1 output enabled		86		
		156.25MHz; 1 output enabled		88		
		312.5MHz; 1 output enabled		97	125	

LVPECL OUTPUT DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1, 2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5% & $V_{DDO1, 2}$ = 3.3V ±5% or 2.5V ±5%,

T_A = –40°C to +85°C, R_L = 50Ω to V_{DDO} – 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		V_{DDO} – 1.145	V_{DDO} – 0.97	V_{DDO} – 0.845	V
V_{OL}	Output Low Voltage		V_{DDO} – 1.945	V_{DDO} – 1.77	V_{DDO} – 1.645	V
V_{SWING}	Output Voltage Swing		0.6	0.8	1.0	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

LVCMOS (PLL_BYPASS, XTAL_SEL, OE1/2, FSEL) DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

REF_IN DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.6	V
I_{IN}	Input Current	XTAL_SEL = V_{IL}, V_{IN} = 0V to V_{DD}	–5		5	µA
		XTAL_SEL = V_{IH}, V_{IN} = V_{DD}		20		µA

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	10pF Load	**Fundamental, Parallel Resonant**			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			1	5	pF
Correlation Drive Level			10	100	uW

AC Electrical Characteristics[4, 5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5% & $V_{DDO1, 2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C, R_L = 50Ω to V_{DDO} – 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT1}	Output Frequency 1[7]	XTAL_SEL = H, FSEL =X, OE1 = H, OE2 = L, PLL Bypass = H		25		MHz
F_{OUT2}	Output Frequency 2[7]	XTAL_SEL = H, FSEL =1, OE1 = H, OE2 = H, PLL Bypass = L		312.5/ 125		MHz
F_{OUT3}	Output Frequency 3[7]	XTAL_SEL = H, FSEL =0, OE1 = H, OE2 = H, PLL Bypass = L		156.25/ 62.5		MHz
F_{OUT4}	Output Frequency 4[7]	XTAL_SEL = L, FSEL =X, OE1 = H, OE2 = L, PLL Bypass = H		REF_IN		MHz
F_{REF}	Reference Input Frequency			25		MHz
T_R/T_F	LVPECL Output Rise/Fall Time	20% – 80%	80	175	350	ps
ODC	Output Duty Cycle		48	50	52	%
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[6]	25MHz Integration Range (12kHz – 5MHz) 62.5MHz Integration Range (12kHz – 10MHz) 125MHz Integration Range (12kHz – 20MHz) 156.25MHz Integration Range (12kHz – 20MHz) 312.5MHz Integration Range (12kHz – 20MHz)		240 315 255 245 250		fs_{rms}
	Spurious Noise Components	12.5MHz using 62.5MHz 25MHz using 125MHz 6.25MHz using 156.25MHz 25MHz using 156.25MHz 12.5MHz using 312.5MHz		-76 -80 -82 -62 -79		dBc

Notes:

5. All phase-noise measurements were taken with an Agilent 5052B phase-noise system.
6. Measured using 25MHz crystal as the input reference source. If using an external reference input, use a low phase-noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.
7. When output bank Q1 and output bank Q2 are externally tied together. Refer to Output selection Table.

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz Crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for further details.

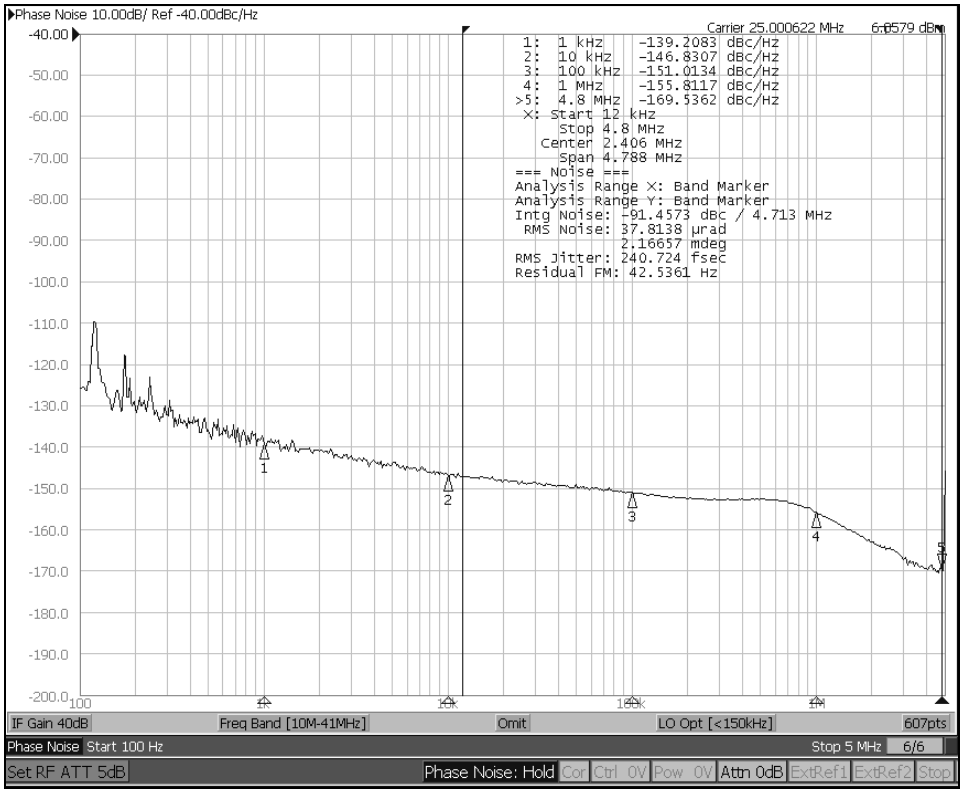
Contact Micrel's HBW applications group if you need assistance on selecting a suitable crystal for your application at hbwhelp@micrel.com.

Parallel outputs to achieve four frequencies

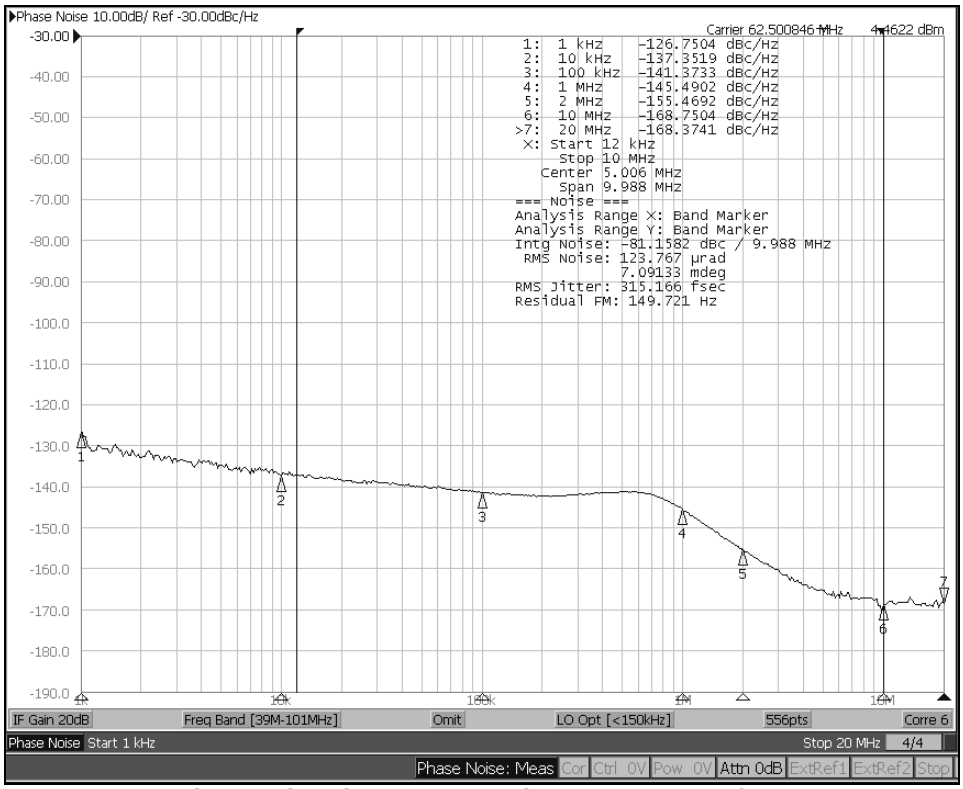
Four frequencies, 62.5MHz, 125MHz, 156.25MHz and 312.5MHz can be achieved in one output channel by shorting Q1 and Q2 outputs together at the device pins.

Frequency selection is achieved using FSEL, OE1 and OE2 pins as outlined in the Output Selection Table.

Phase Noise Plots

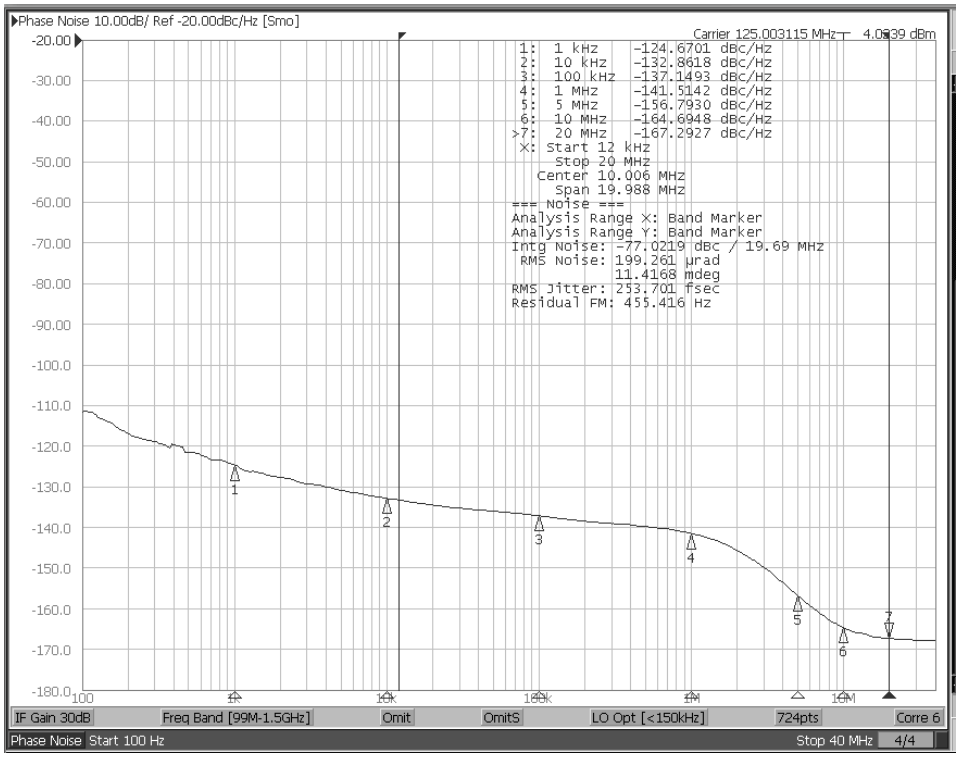


Phase Noise Plot: 25MHz, 12kHz – 5MHz, 241 fs_{rms}

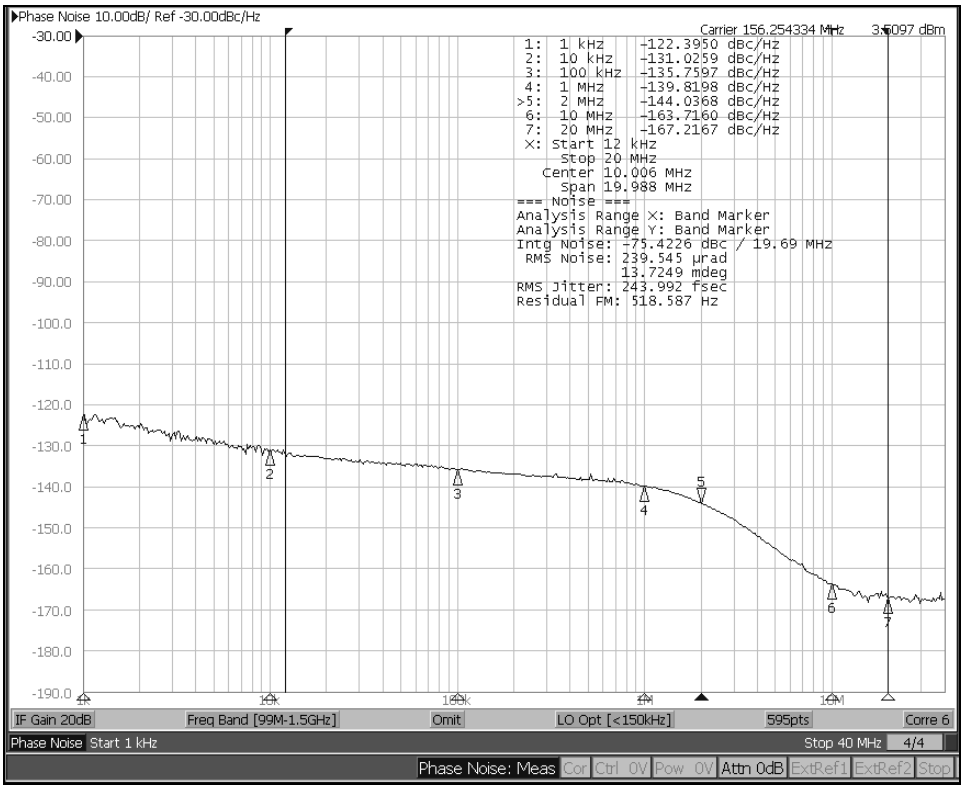


Phase Noise Plot: 62.5MHz, 12kHz – 10MHz, 315 fs_{rms}

Phase Noise Plots (Continued)

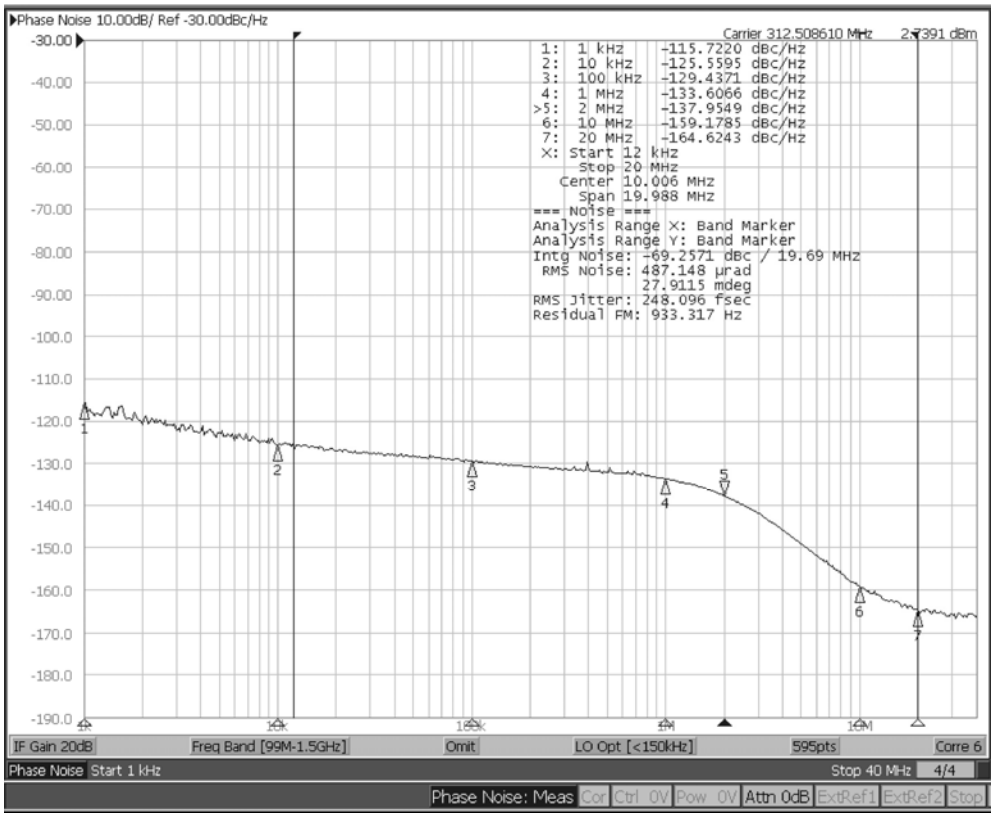


Phase Noise Plot: 125MHz, 12kHz – 20MHz, 254 fs_{rms}



Phase Noise Plot: 156.25MHz, 12kHz – 20MHz, 244 fs_{rms}

Phase Noise Plots (Continued)



Phase Noise Plot: 312.5MHz, 12kHz – 20MHz, 248 fs_{rms}

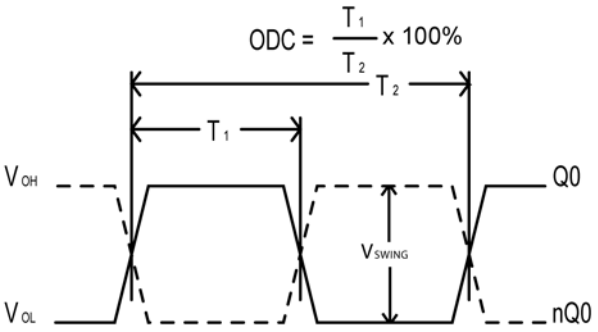


Figure 1. Duty Cycle Timing

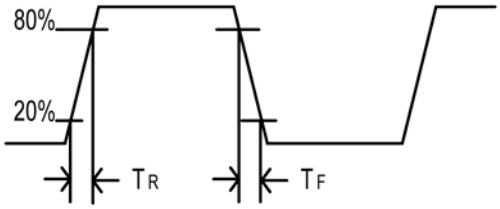


Figure 2. All Outputs Rise/Fall Time

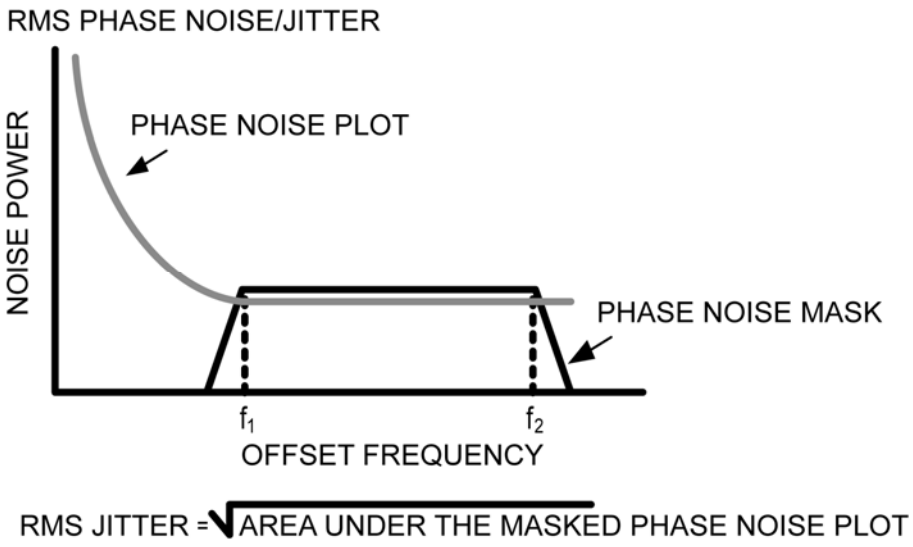


Figure 3. RMS Phase Noise Jitter

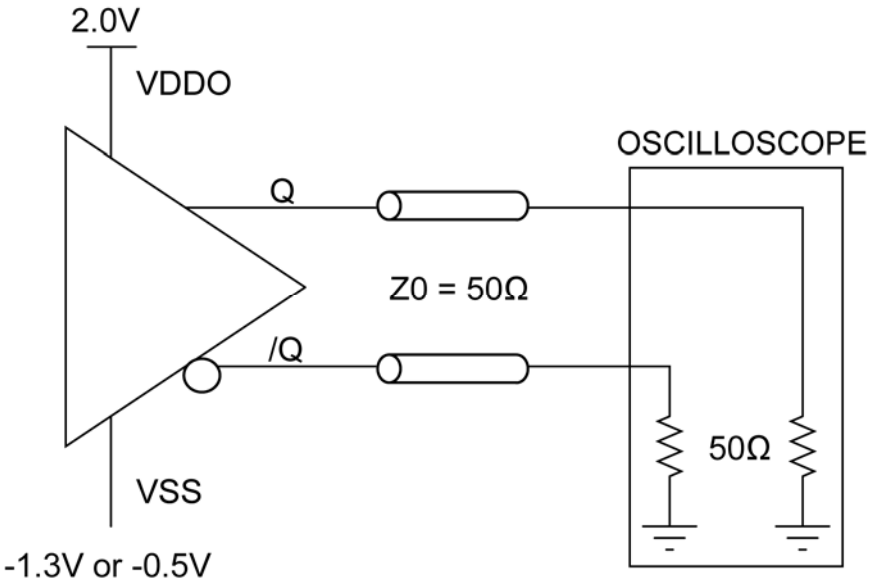


Figure 4. LVPECL Output Load and Test Circuit

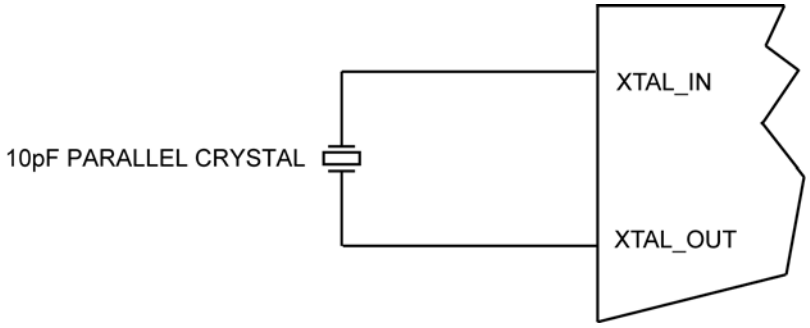
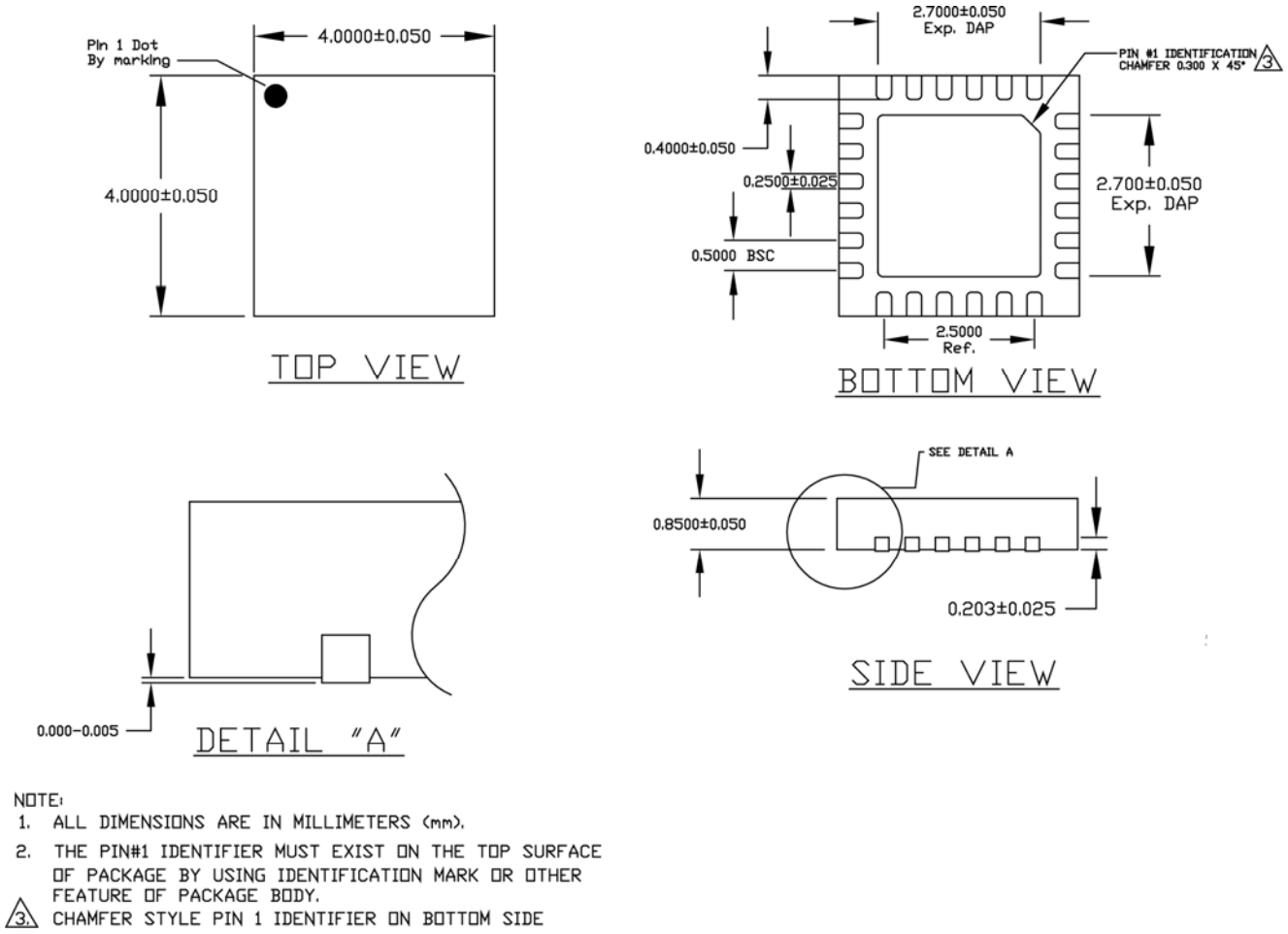


Figure 5. Crystal Input Interface

Package Information



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin QFN

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com