



**SILERGY**

# Application Note: SM8082A

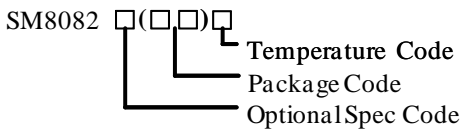
High Efficiency, 1.5MHz, 2A  
Synchronous Step Down Regulator

## General Description

The SM8082A is a high efficiency 1.5MHz synchronous step down DC/DC regulator, which is capable of delivering up to 2A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1.5MHz switching frequency.

## Ordering Information



Ordering Number	Package type	Note
SM8082AAAC	SOT23-5	--

## Features

- 2.5V to 5.5V Input Voltage Range
- 70 $\mu$ A Low Quiescent Current
- Low  $R_{DS(ON)}$  for Internal Switches (Top/Bottom) 130m $\Omega$  /90m $\Omega$
- High Switching Frequency 1.5MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Hic-cup for Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: SOT23-5

## Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart phone

## Typical Applications

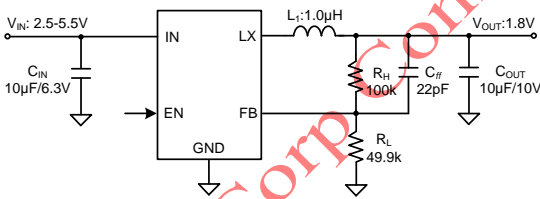


Figure1. Schematic Diagram

Inductor and  $C_{OUT}$  Selection Table

$V_{OUT}$ [V]	L [ $\mu$ H]	$C_{OUT}$ [ $\mu$ F]			
		4.7	10	22	2 $\times$ 22
1.2 / 1.8 / 3.3	0.47		√	√	√
	1.0		☆	√	√
	2.2			√	√

Note: '☆' means recommended for most applications.

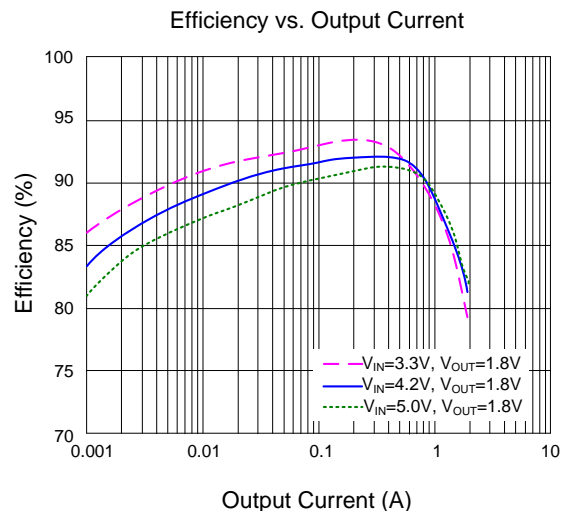
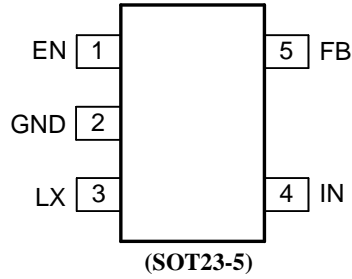


Figure2. Efficiency vs. Output Current

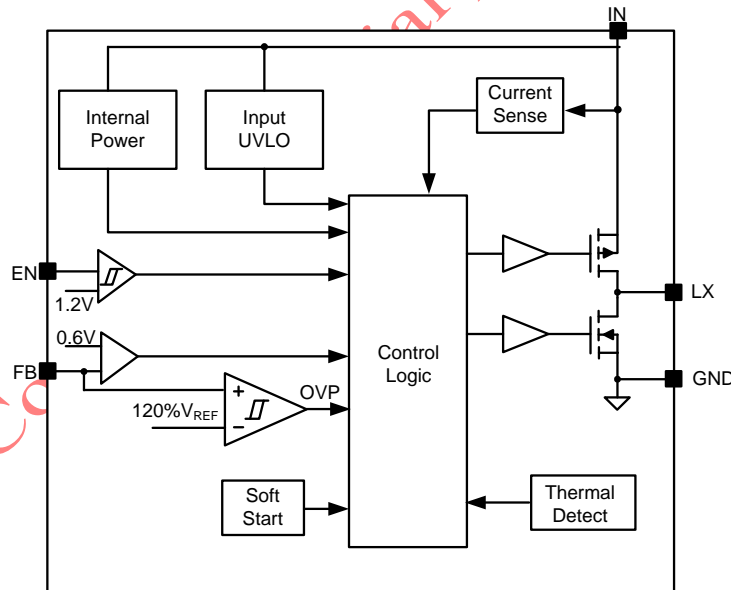
## Pinout (Top View)



**Top Mark:K6xyz** (device code: K6, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull high to turn on. Do not leave it floating.
GND	2	Ground pin.
LX	3	Inductor pin. Connect this pin to the switching node of the inductor.
IN	4	Input pin. Decouple this pin to the GND pin with at least a 10 $\mu$ F ceramic capacitor.
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_H/R_L)$ .

## Block Diagram



**Figure3. Block Diagram**



**Absolute Maximum Ratings** (Note 1)

Supply Input Voltage	-0.3V to 6.0V
FB, EN Voltage	-0.3V to $V_{IN}+0.6V$
LX Voltage	-0.3V <sup>(*1)</sup> to 6.0V <sup>(*2)</sup>
Power Dissipation, $P_D$ @ $T_A = 25\text{ }^\circ\text{C}$	0.83W
Package Thermal Resistance (Note 2)	
$\theta_{JA}$	120 $^\circ\text{C/W}$
$\theta_{JC}$	20 $^\circ\text{C/W}$
Junction Temperature Range	-40 $^\circ\text{C}$ to 150 $^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	260 $^\circ\text{C}$
Storage Temperature Range	-65 $^\circ\text{C}$ to 150 $^\circ\text{C}$
(*1) LX Voltage Tested Down to -3V<40ns	
(*2) LX Voltage Tested Up to +7V<40ns	

**Recommended Operating Conditions** (Note 3)

Supply Input Voltage	2.5V to 5.5V
Junction Temperature Range	-40 $^\circ\text{C}$ to 125 $^\circ\text{C}$
Ambient Temperature Range	-40 $^\circ\text{C}$ to 85 $^\circ\text{C}$

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## Electrical Characteristics

( $V_{IN} = 5V$ ,  $V_{OUT} = 1.8V$ ,  $L = 1.0\mu H$ ,  $C_{OUT} = 10\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise specified)

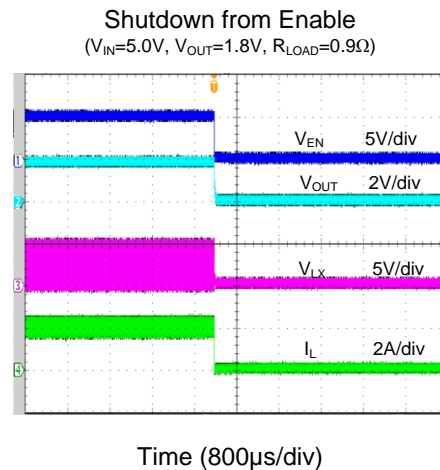
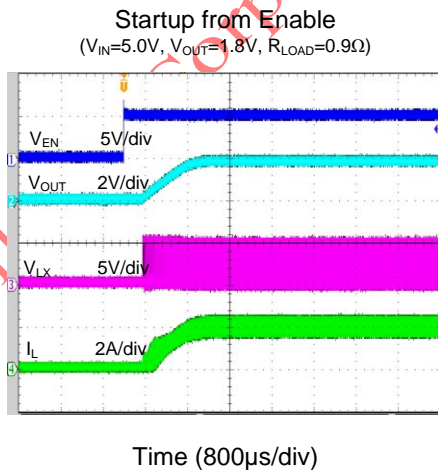
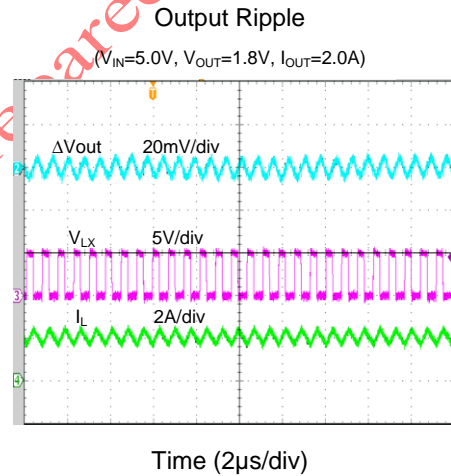
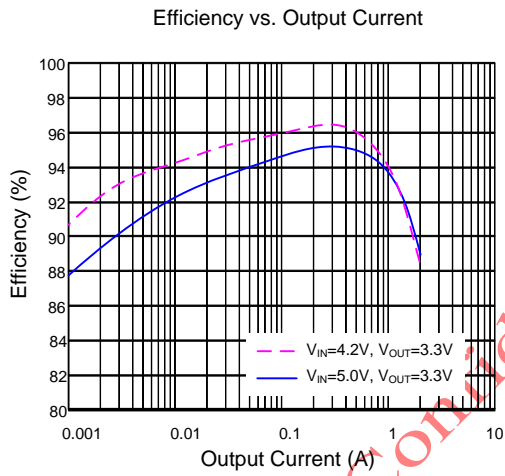
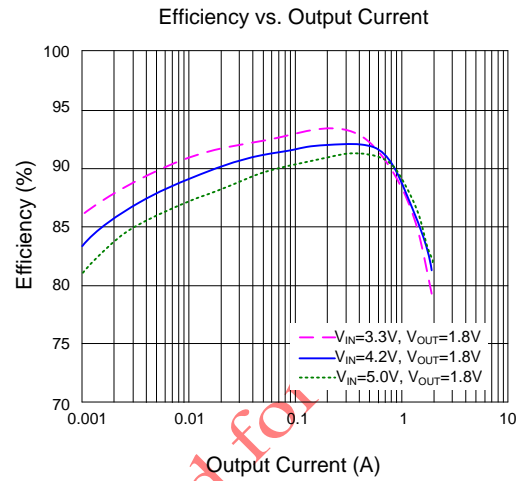
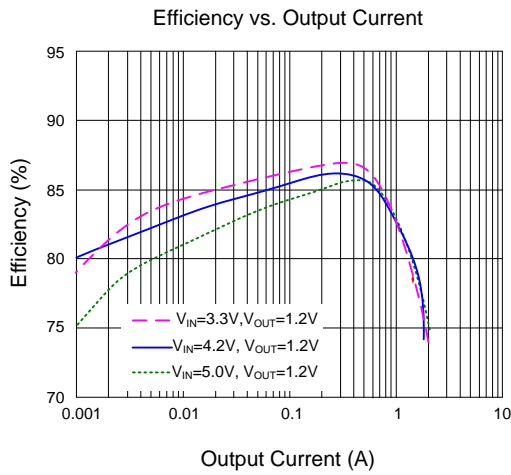
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		2.5		5.5	V
Input UVLO Threshold	$V_{UVLO}$				2.5	V
Input UVLO Hysteresis	$V_{HYS}$			150		mV
Quiescent Current	$I_Q$	$V_{FB} = V_{REF} \times 105\%$		70	100	$\mu A$
Shutdown Current	$I_{SHDN}$	$V_{EN} = 0V$		0.1	1	$\mu A$
Feedback Reference Voltage	$V_{REF}$	$I_{OUT} = 0.5A$ , CCM	588	600	612	mV
LX Node Discharge Resistance	$R_{DIS}$			50		$\Omega$
Top FET $R_{ON}$	$R_{DS(ON)1}$			130		m $\Omega$
Bottom FET $R_{ON}$	$R_{DS(ON)2}$			90		m $\Omega$
EN Input Voltage High	$V_{EN,H}$		1.2			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
Min on Time	$t_{ON,MIN}$			60		ns
Maximum Duty Cycle	$D_{MAX}$		100			%
Turn on Delay	$t_{ON,DLY}$	from EN high to LX start switching		0.5		ms
Soft-start Time	$t_{SS}$	$V_{OUT}$ from 0% to 100%		1		ms
Switching Frequency	$f_{SW}$	$I_{OUT} = 0.5A$ , CCM		1.5		MHz
Top FET Current Limit	$I_{LMT, TOP}$		3.5			A
Thermal Shutdown Temperature	$T_{SD}$			150		$^\circ C$
Thermal Shutdown Hysteresis	$T_{HYS}$			20		$^\circ C$

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  of SM8082A is measured in the natural convection at  $T_A = 25^\circ C$  on a 2OZ two-layer Silergy evaluation board. Pin 3 is the case position for  $\theta_{JC}$  measurement.

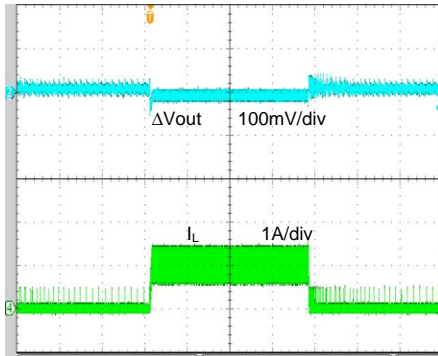
**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Typical Performance Characteristics



### Load Transient

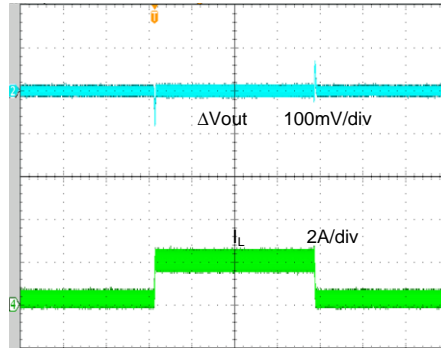
( $V_{IN}=5.0V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=0\sim 1.0A$ )



Time (400μs/div)

### Load Transient

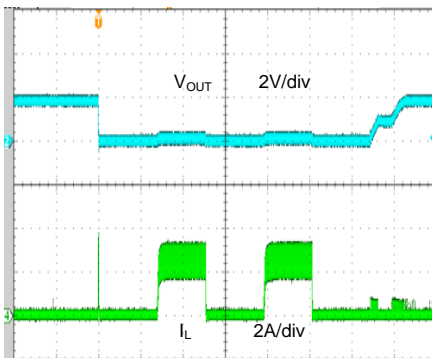
( $V_{IN}=5.0V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=0.2\sim 2.0A$ )



Time (400μs/div)

### Short Circuit Protection

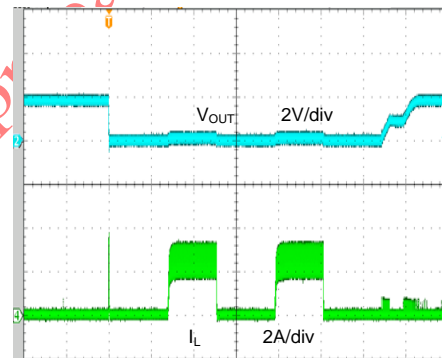
( $V_{IN}=5.0V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=0\sim \text{Short}$ )



Time (2ms/div)

### Short Circuit Protection

( $V_{IN}=5.0V$ ,  $V_{OUT}=1.8V$ ,  $I_{OUT}=2.0A\sim \text{Short}$ )



Time (2ms/div)

## Operation

The SM8082A is a high efficiency 1.5MHz synchronous step down DC/DC regulator, which is capable of delivering up to 2A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

## Applications Information

Because of the high integration in the SM8082A, the application circuit based on this regulator IC is rather simple. Only input capacitor  $C_{IN}$ , output capacitor  $C_{OUT}$ , output inductor  $L$  and feedback resistors ( $R_H$  and  $R_L$ ) need to be selected for the targeted applications specifications.

### Feedback Resistor Dividers $R_H$ and $R_L$

Choose  $R_H$  and  $R_L$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_H$  and  $R_L$ . A value of between 10k and 200k is highly recommended for  $R_L$ . If  $R_L=100k$  is chosen, then  $R_H$  can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6V) \cdot R_L}{0.6V}$$

### Input Capacitor $C_{IN}$

A typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 10 $\mu$ F capacitance is recommended. This ceramic capacitor need to be placed really close to the IN and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by  $C_{IN}$ , and IN/GND pins.

### Output Capacitor $C_{OUT}$

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 10V rating and greater than 10 $\mu$ F capacitance.

### Output Inductor $L$

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple

current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where  $F_{SW}$  is the switching frequency and  $I_{OUT,MAX}$  is the maximum load current.

The SM8082A regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 30m\Omega$  to achieve a good overall efficiency.

### Load Transient Considerations

The SM8082A integrates the compensation components to achieve good stability and fast transient responses. In some application, adding a ceramic capacitor (feed-forward capacitor,  $C_{ff}$ ) in parallel with  $R_H$  may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements. Typically, for 1.2V/1.8V/3.3V output, the  $R_H$ ,  $R_L$ ,  $C_{ff}$  is recommended as below:

**Table1. Recommended Component Selection**

$V_{OUT}$	$R_H$	$R_L$	$C_{ff}$
1.2V	49.9k $\Omega$	49.9k $\Omega$	22pF
1.8V	100k $\Omega$	49.9k $\Omega$	22pF
3.3V	100k $\Omega$	22.1k $\Omega$	22pF

### OCP and SCP Protection Method

With load current increasing, as soon as the high side FET current gets higher than peak current limit threshold, the high side FET will turn off. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 50% of the regulation level, the output UVP will be detected and SM8082A will operate in hip-cup mode. The hip-cup frequency is 190Hz, the hip-cup duty cycle is 50%. If the hard short is removed, the IC will return to normal operation.

## Layout Design

The layout design of the SM8082A regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC:  $C_{IN}$ , L,  $R_H$  and  $R_L$ .

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2)  $C_{IN}$  must be close to Pins IN and GND. The loop area formed by  $C_{IN}$  and GND must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The components  $R_H$  and  $R_L$ , and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-ion battery, it is desirable to add a pull down  $1M\Omega$  resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

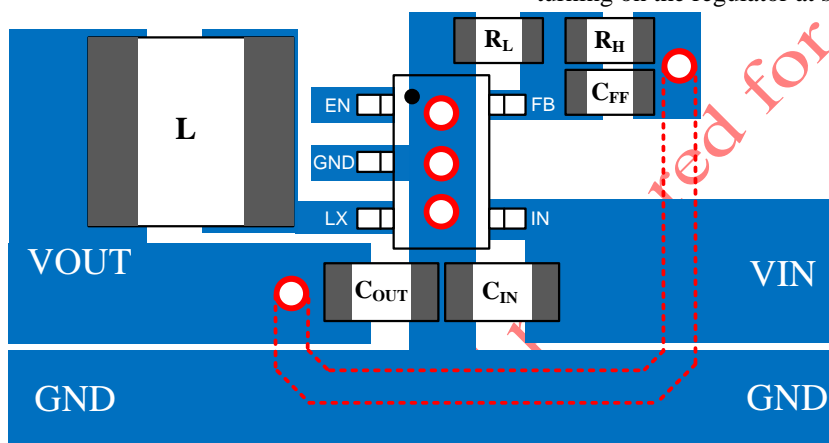
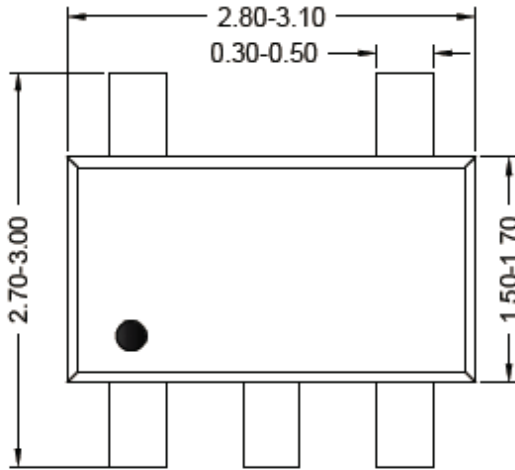


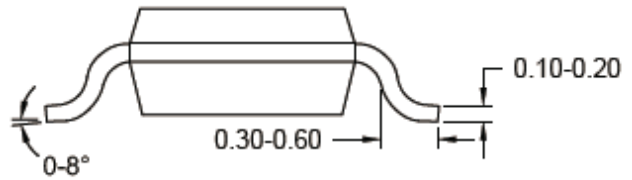
Figure4. PCB Layout Suggestion



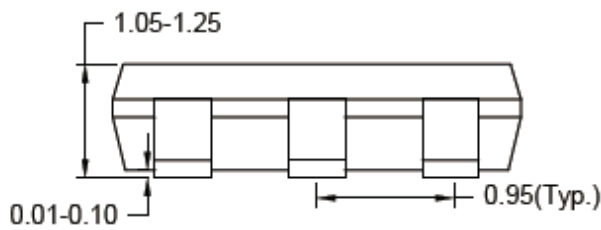
## SOT23-5 Package Outline & PCB layout



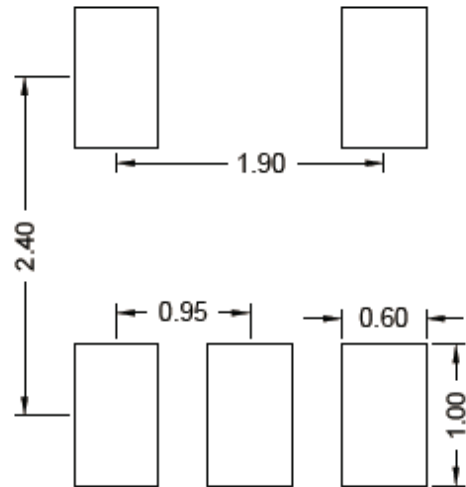
Top view



Side view



Front view



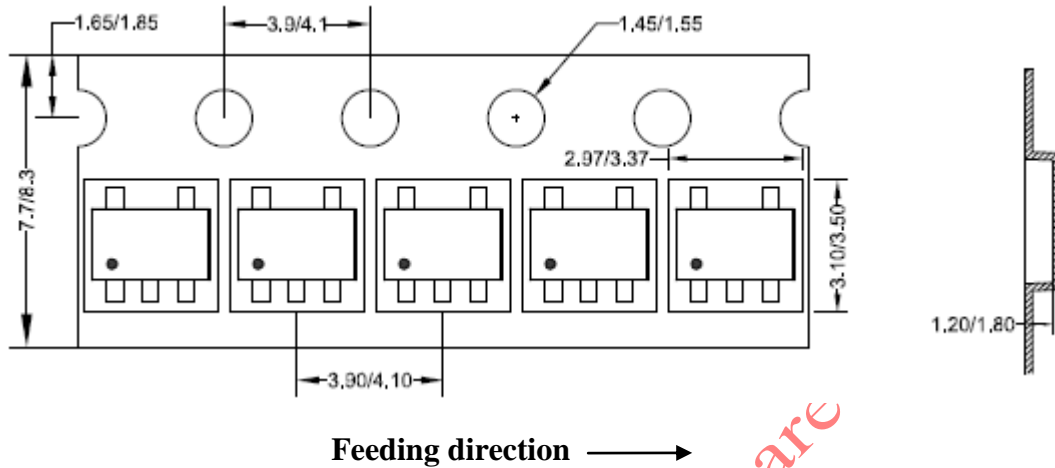
Recommended Pad Layout

**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

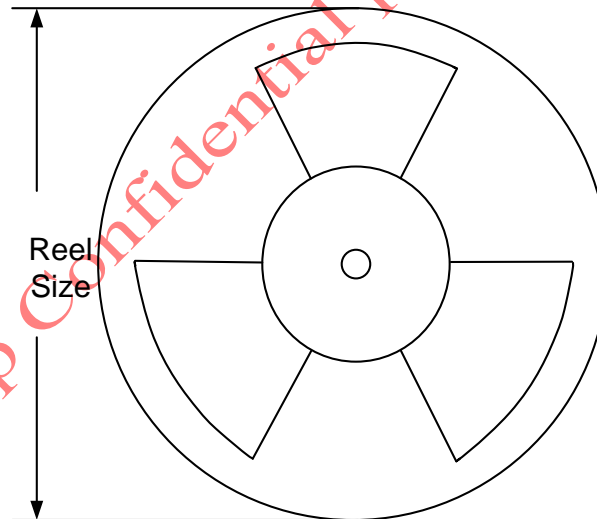
## Taping & Reel Specification

### 1. Taping orientation

SOT23-5



### 2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000

### 3. Others: NA