SM813XXX

Flexible Ultra-Low Jitter Clock Synthesizer

Features

- Generates Up to 8 Differential or Single-Ended Outputs
- <65 fs Phase Jitter @ 156.25 MHz (1.875 MHz to 20 MHz)
- <115 fs Phase Jitter @ 156.25 MHz (12 kHz to 20 MHz)
- On-Chip Power Supply Regulation for Excellent Power Supply Noise Immunity
- Two High-Performance PLL Synthesizers to Generate Multiple Frequencies
- Independently Programmable Output Logic and Frequency:
  - Output Logic: LVPECL, LVDS, HCSL, LVCMOS
- Fundamental Mode Crystal: 31.25 MHz to 156.250 MHz
- No External Crystal Oscillator Capacitors Required
- 2.5V or 3.3V Operating Power Supply
- Separate Output Power Supplies:
  - Each Bank can be at Different Power Supply Voltage Levels (4 Banks of 2 Outputs Each)
- Industrial Temperature Range, –40°C to +85°C
- Green, RoHS-, and PFOS-Compliant 48-Pin 7 mm x 7 mm QFN Package

Applications

- 1/10/40/100 Gigabit Ethernet (GbE)
- SONET/SDH
- PCI-Express
- CPRI/OBSAI – Wireless Base Station
- Fibre Channel
- SAS/SATA
- DIMM (DDR2/DDR3/AMB)
- HDMI

General Description

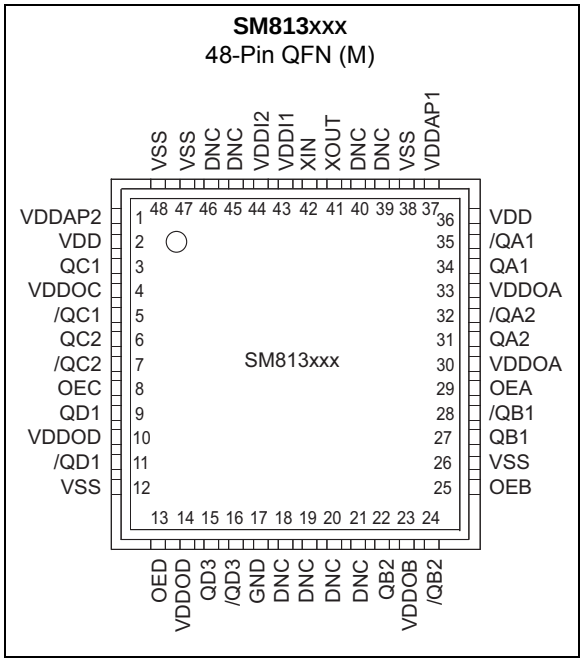
The SM813xxx is a dual-PLL clock generator that achieves ultra-low phase jitter (<65 fs_{RMS}). With 8 total outputs and dividers on each output, this device can generate 8 different frequencies up to 850 MHz, from a low-cost quartz crystal.

Each of 8 outputs can be independently programmed to LVPECL, LVDS, HCSL, or LVCMOS logic. For LVCMOS, only the true side of the channel is used.

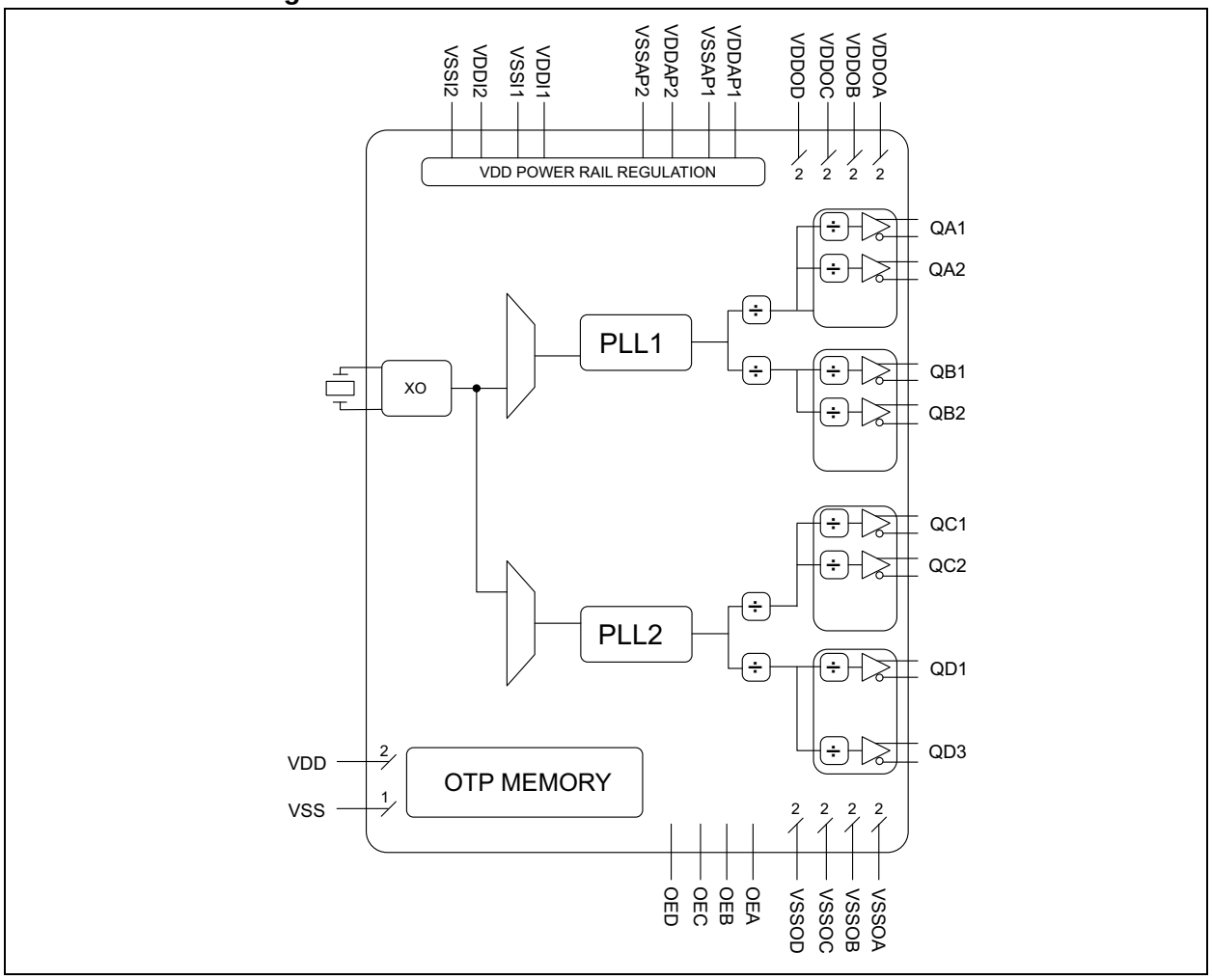
The SM813xxx is packaged in a 48-pin QFN with up to 8 outputs.

Package Type

SM813xxx
48-Pin QFN (M)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}, V_{DDA}, V_{DDI}, V_{DDO}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to +4.6V
ESD Rating (MM)(1) 200V
ESD Rating (HBM)(1) ..... 2 kV

Operating Ratings ‡

Supply Voltage (V_{DD}, V_{DDO}) ..... +2.375V to +3.465V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Typical values are T_A = +25°C, min./max. across –40°C ≤ T_A ≤ +85°C, unless otherwise noted.						
Symbol	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Condition**
V_{DD}, V_{DDO}	Supply Voltage	2.375	2.5	2.625	V	2.5V Operation
		3.135	3.3	3.465		3.3V Operation
V_{DDI1}, V_{DDI2}	Analog Supply Voltage	2.375	—	3.465	V	—
V_{DDA}	PLL Core Voltage	2.375	—	3.465	V	—
I_{DDA}	PLL Core Current Consumption (Note 1)	—	—	60	mA	Per Active PLL
I_{DDI}	Analog Current Consumption (Note 1)	—	—	10	mA	—
I_{DDO}	Output Stage Current Consumption (Note 1)	—	—	70	mA	Per Output Bank, Unloaded.
I_{DD}	Miscellaneous Logic	—	—	8	mA	—

Note 1: Supply current may change depending on the device’s configuration.

TABLE 1-2: LVPECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO} - 2V.

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output High Voltage	V_{DDO} - 1.35	V_{DDO} - 1.01	V_{DDO} - 0.8	V	—
V_{OL}	Output Low Voltage	V_{DDO} - 2	V_{DDO} - 1.78	V_{DDO} - 1.6	V	—
V_{SWING}	Peak-to-Peak Output Voltage	0.65	0.77	0.95	V	Figure 4-3

TABLE 1-3: LVDS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 100Ω between Q and /Q.

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
V_{OD}	Differential Output Voltage	245	350	530	mV	Figure 4-3
V_{CM}	Common Mode Voltage	1.125	1.2	1.375	V	—
V_{OH}	Output High Voltage	1.248	1.375	1.602	V	—
V_{OL}	Output Low Voltage	0.898	1.025	1.252	V	—

TABLE 1-4: HCSL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{SS}.

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output High Voltage	660	700	850	mV	—
V_{OL}	Output Low Voltage	–150	0	27	mV	—
V_{CROSS}	Crossing Point Voltage	—	350	—	V	—

TABLE 1-5: LVCMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO}/2.

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output High Voltage	V_{DD} - 0.8	—	—	V	Highest Drive (default)
V_{OL}	Output Low Voltage	—	—	0.5	V	—
V_{IH}	Input High Voltage	V_{DD} - 0.7	—	V_{DD} + 0.3	V	—
V_{IL}	Input Low Voltage	V_{SS} - 0.3	—	0.3 x V_{DD}	V	—
I_{IH}	Input High Current	—	—	5	µA	V_{DD} = V_{IN} = 3.465V
I_{IL}	Input Low Current	–150	—	—	µA	V_{DD} = 3.465V, V_{IN} = 0V

TABLE 1-6: CRYSTAL CHARACTERISTICS

Parameters	Min.	Typ.	Max.	Units	Conditions
Mode of Oscillation	Fundamental, Parallel Resonant				—
Frequency	31.25	—	156.25	MHz	—

TABLE 1-6: CRYSTAL CHARACTERISTICS (CONTINUED)

Parameters	Min.	Typ.	Max.	Units	Conditions
Equivalent Series Resistance (ESR)	—	—	80	Ω	Saunders 250B, 25Ω Pi Network
Load Capacitance (C_L)	—	8	—	pF	Device Equivalent Load
Shunt Capacitor, C0	—	1	2	pF	—
Correlation Drive Level	—	10	100	µW	—

TABLE 1-7: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C.						
Symbol	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
F_{IN}	Input Frequency	31.25	50	156.25	MHz	XO
F_{OUT}	Output Frequency	12	—	850	MHz	LVPECL, LVDS, HCSL
		12	—	250		LVCMOS
t_r/t_f	Output Rise/Fall Time (Note 1)	85	135	350	ps	LVPECL Output
		85	140	300		LVDS Output
		175	300	450		HCSL Output
		100	200	400		LVCMOS Output
ODC	Output Duty Cycle	45	50	55	%	All Output Frequencies
		48	50	52		<350 MHz Output Frequencies
T_{SKEW}	Output-to-Output Skew (Note 2, Note 3)	—	—	50	ps	Note 3, Same Output Bank
T_{LOCK}	PLL Lock Time	—	5	20	ms	V_{DD} = 90%
$T_{jit(Ø)}$	RMS Phase Jitter (Note 4, Note 5)	—	112	150	fs	Integration Range 12 kHz - 20 MHz
		—	64	—		Integration Range 1.875 MHz - 20 MHz

Note 1: See Figure 4-6.

2: Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.

3: Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output logic type setting.

4: All phase noise measurements were taken with an Agilent 5052B phase noise system.

5: Measured using a 52.0833 MHz crystal as the input reference source.

There are sufficient feedback dividers to support below 20 MHz, down to about 12 MHz, but phase noise performance will be impacted. Please contact Microchip TCG Applications for more information.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature	T_A	–40	—	+85	°C	Note 1
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20s
Case Temperature	—	—	—	+115	°C	—
Package Thermal Resistances						
Junction Thermal Resistance QFN, Still Air	θ_{JA}	—	24	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Pin Level	Description
34, 35	QA1, /QA1	O (DIF, SE)	LVPECL LVDS HCSL LVCMOS (Q only)	Differential/Single-Ended Clock Output (LVCMOS)
31, 32	QA2, /QA2			
27, 28	QB1, /QB1			
22, 24	QB2, /QB2			
3, 5	QC1, /QC1			
6, 7	QC2, /QC2			
9, 11	QD1, /QD1			
15, 16	QD3, /QD3			
2, 36	V_{DD}	PWR	—	Power Supply
30, 33	V_{DDOA}	PWR	—	Power Supply for Outputs QA1–2
23	V_{DDOB}	PWR	—	Power Supply for Outputs QB1–2
4	V_{DDOC}	PWR	—	Power Supply for Outputs QC1–2
10, 14	V_{DDOD}	PWR	—	Power Supply for Outputs QD1 and QD3
37	V_{DDAP1}	PWR	—	Power Supply for PLL1
1	V_{DDAP2}	PWR	—	Power Supply for PLL2
43	V_{DDI1}	PWR	3.3V Only	Power Supply for Input Circuits
44	V_{DDI2}	PWR	3.3V Only	Power Supply for Input Circuits
12, 26, 38 47, 48, ePAD	V_{SS} (Exposed Pad)	PWR	—	Power Supply Ground. The exposed pad must be connected to the V_{SS} ground plane.
29	OEA1/2	I, (SE)	LVCMOS	Output Enable, Outputs QA1/2 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75 kΩ pull-up
25	OEB1/2	I, (SE)	LVCMOS	Output Enable, Outputs QB1/2 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75 kΩ pull-up
8	OEC1/2	I, (SE)	LVCMOS	Output Enable, Outputs QC1/2 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75 kΩ pull-up
13	OED1/3	I, (SE)	LVCMOS	Output Enable, Outputs QD1/3 disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75 kΩ pull-up
42	XIN	I, (SE)	8 pF Crystal	Crystal Reference Input, no load caps needed
41	XOUT	O, (SE)	8 pF Crystal	Crystal Reference Output, no load caps needed
18, 19, 20, 21	DNC	DNC	—	Leave open; for normal operation, do not connect to anything.
17	GND	I	—	This pin is not Power Supply ground, but must be tied to V_{SS} for proper operation.

TABLE 2-2: TRUTH TABLE

OEA	OEB	OEC	OED	Output
0	1	1	1	2 QA outputs tri-state
1	0	1	1	2 QB outputs tri-state
1	1	0	1	2 QC outputs tri-state
1	1	1	0	2 QD outputs tri-state

2.1 Key Programmable Parameters

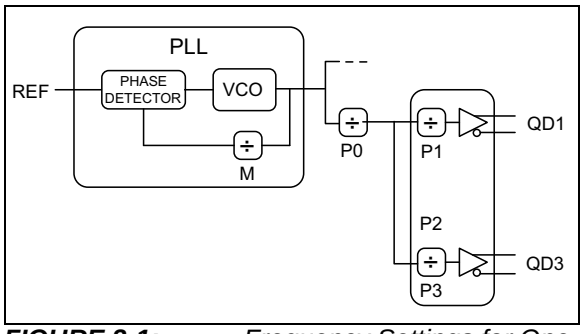


FIGURE 2-1: *Frequency Settings for One PLL and One Output Bank.*

The VCO in the PLL has a range of ~2875 MHz to 3510 MHz.

Counters M and P0 have a range of 4 to 259.

Counters P1, P2, and P3 have a range of 1 to 16.

EQUATION 2-1:

$$F_{VCO} = REF \times M$$

EQUATION 2-2:

$$QD1 = F_{VCO} \div (P0 \times P1)$$

EQUATION 2-3:

$$QD3 = F_{VCO} \div (P0 \times P3)$$

2.1.1 OUTPUT LOGIC PROGRAMMING

Available output logic types are LVPECL, LVDS, HCSL, and LVCMOS.

Each output can be programmed individually to one of the four logic types.

All logic types are differential, except LVCMOS. For LVCMOS, only the true channel of the output pair is enabled and the complementary channel is disabled. With LVCMOS there is also an output drive setting. There is one setting for all LVCMOS outputs, so all LVCMOS outputs will have the same drive strength.

Unused outputs are disabled to high impedance.

3.0 PHASE NOISE PERFORMANCE

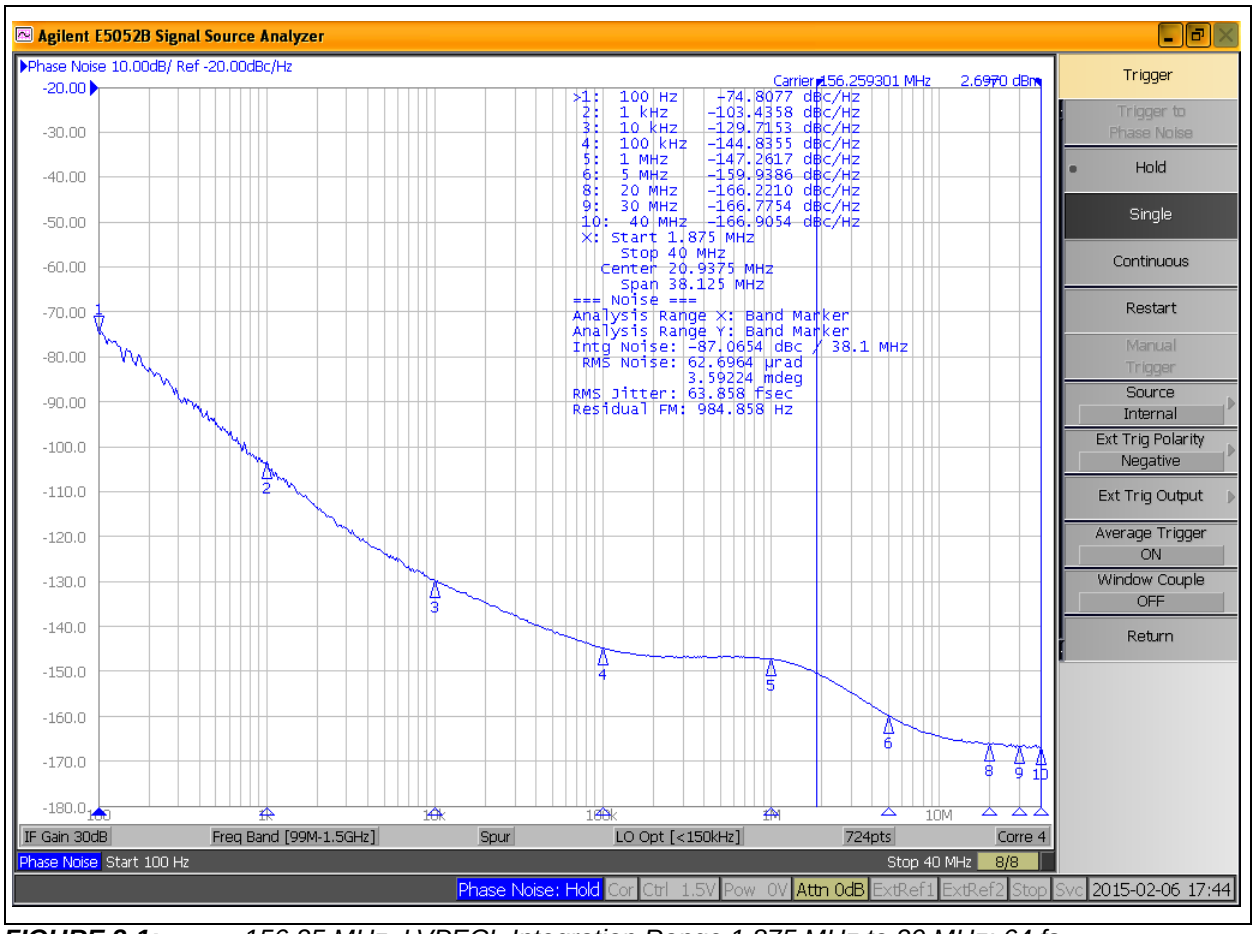


FIGURE 3-1: *156.25 MHz, LVPECL Integration Range 1.875 MHz to 20 MHz: 64 fs_{RMS}.*

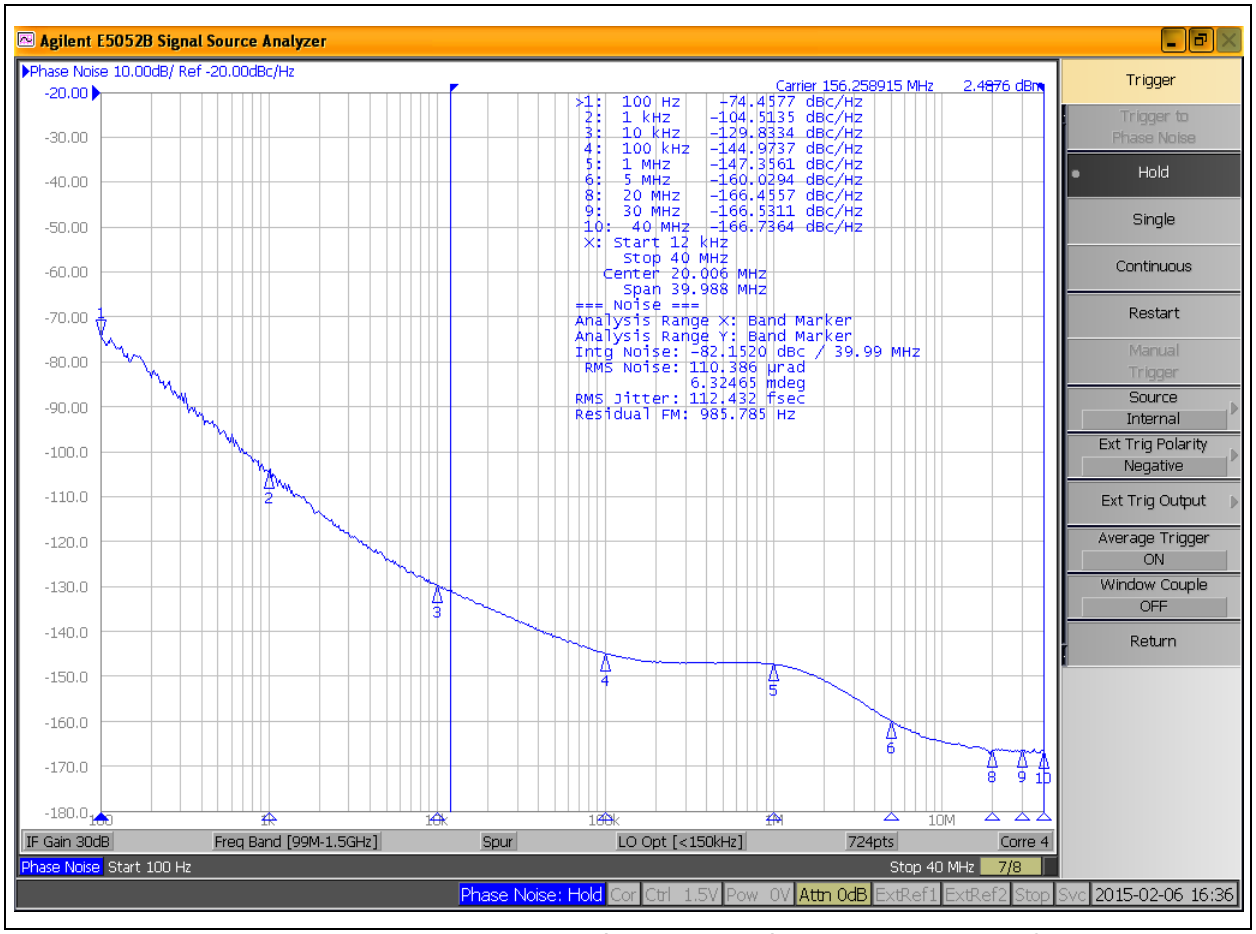


FIGURE 3-2: *156.25 MHz, LVPECL Integration Range 12 kHz to 40 MHz: 112.4 fs_{RMS}.*

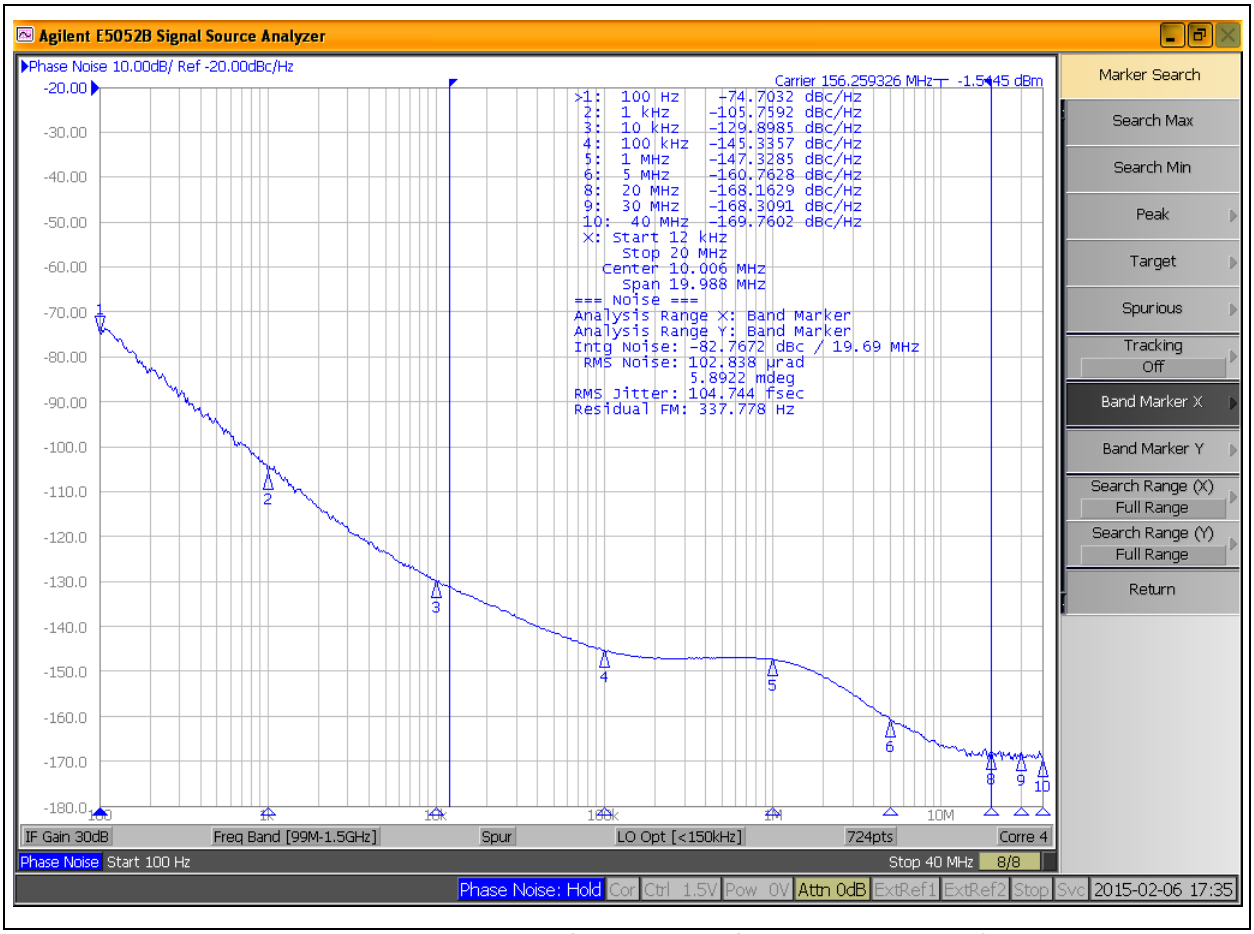


FIGURE 3-3: *156.25 MHz, LVDS Integration Range 12 kHz to 20 MHz: 105 fs_{RMS}.*

4.0 APPLICATION INFORMATION

4.1 Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the *ANTC207* application note for further details.

If you need help selecting a suitable crystal for your application, contact Microchip's TCG applications group at: tcghelp@microchip.com.

4.2 Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin, and start a 50Ω trace on the other side of the resistor.

For differential traces, use either a differential design or two separate 50Ω traces. For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC-coupled or DC-coupled to its termination.

4.3 Power Supply Filtering Recommendations

- Use the power supply filtering shown in Figure 4-1 for V_{DDAP1}, V_{DDAP2}, V_{DDI1} and V_{DDI2}.
- Connect the V_{DDO} and V_{DD} pins directly to the V_{DD} power plane.
- Connect all V_{SS} pins directly to the ground power plane.
- Recommended ferrite bead properties are 80Ω to 240Ω impedance and >250 mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, Microchip's Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in Figure 4-2 and can be used for any of the above V_{DD} sections in Figure 4-1.

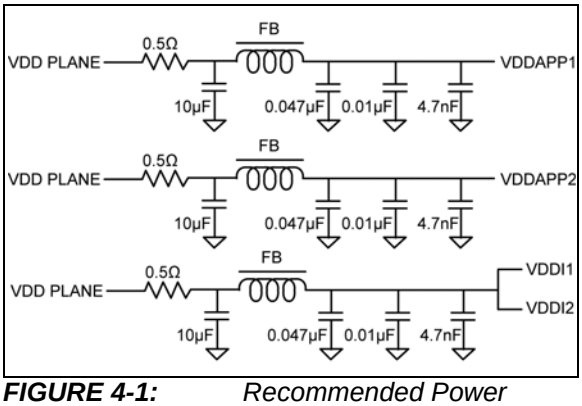


FIGURE 4-1: *Recommended Power Supply Filtering.*

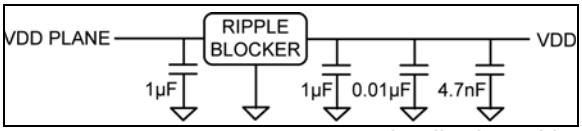


FIGURE 4-2: *Power Supply Filtering with Ripple Blocker.*

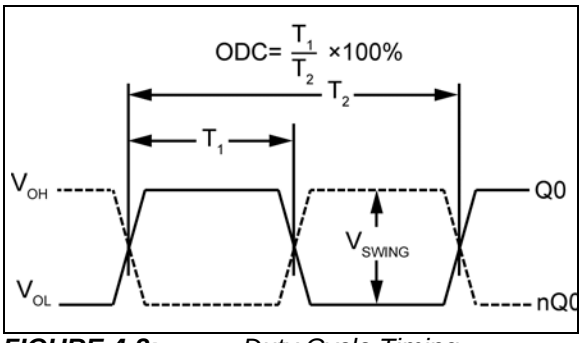


FIGURE 4-3: *Duty Cycle Timing.*

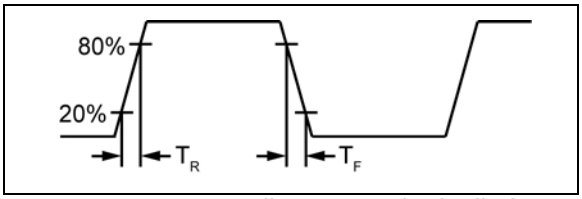


FIGURE 4-4: *All Outputs Rise/Fall Time.*

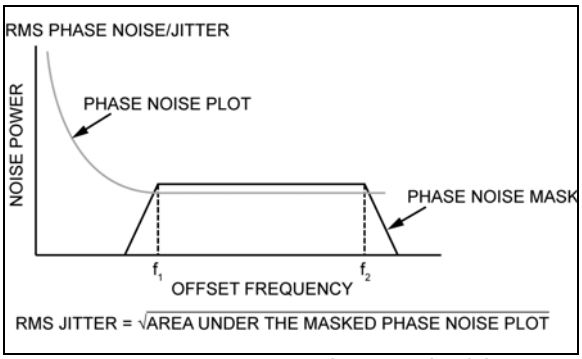


FIGURE 4-5: *RMS Phase Noise/Jitter.*

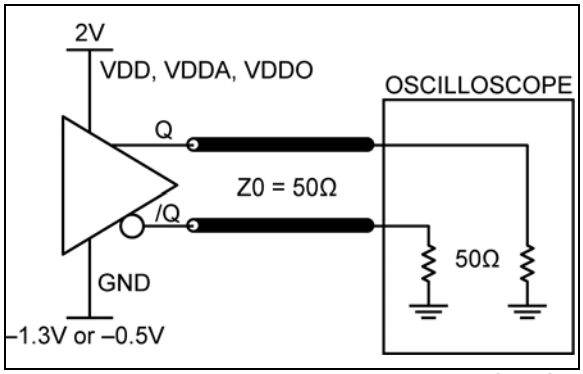


FIGURE 4-6: *LVPECL Output Load and Test Circuit.*

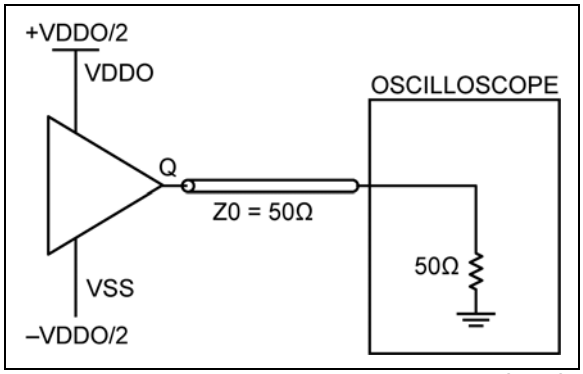


FIGURE 4-9: *LVCMOS Output Load and Test Circuit.*

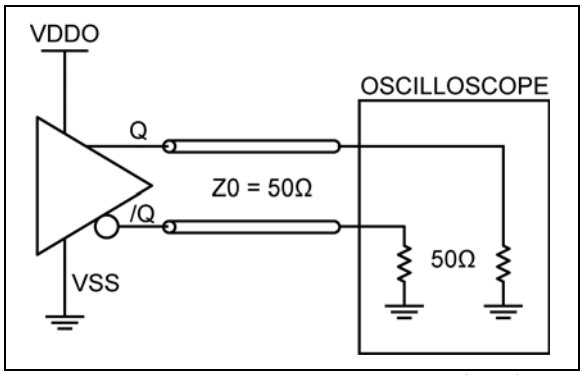


FIGURE 4-7: *HCSL Output Load and Test Circuit.*

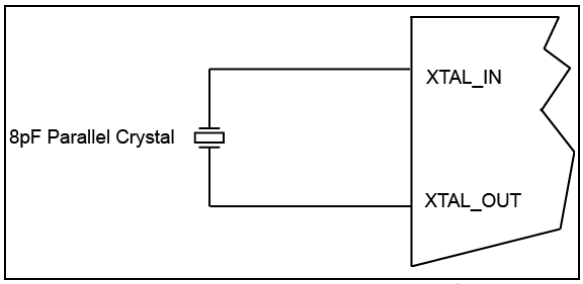


FIGURE 4-10: *SM813xxx Crystal Input Interface.*

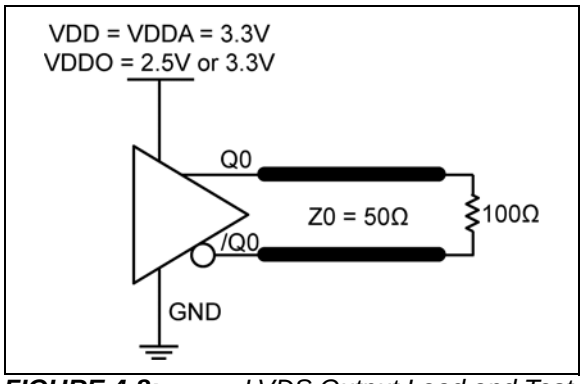


FIGURE 4-8: *LVDS Output Load and Test Circuit.*

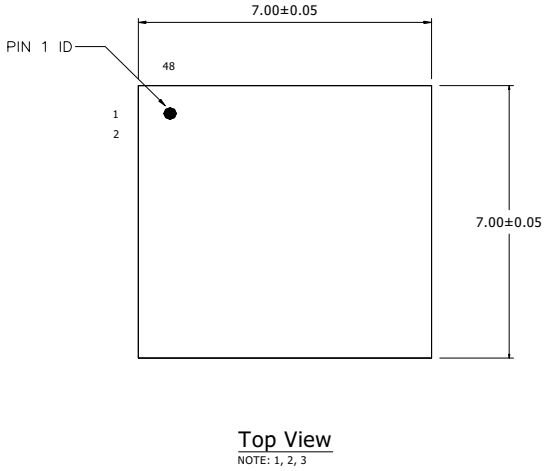
5.0 PACKAGING INFORMATION

48-Lead QFN 7 mm x 7 mm Package Outline and Recommended Land Pattern

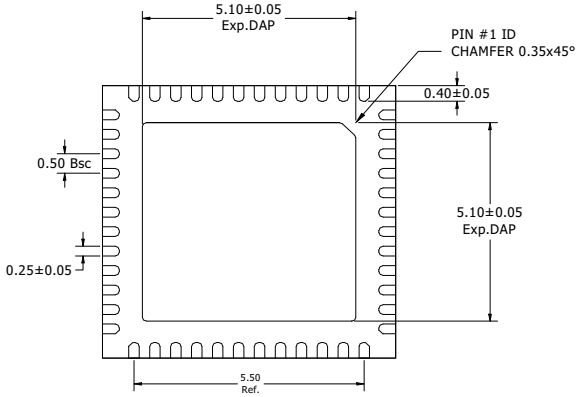
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TITLE
48 LEAD QFN 7x7mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

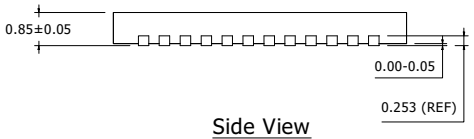
DRAWING #	QFN77-48LD-PL-1	**UNIT**	MM



Top View
NOTE: 1, 2, 3



Bottom View
NOTE: 1, 2, 3

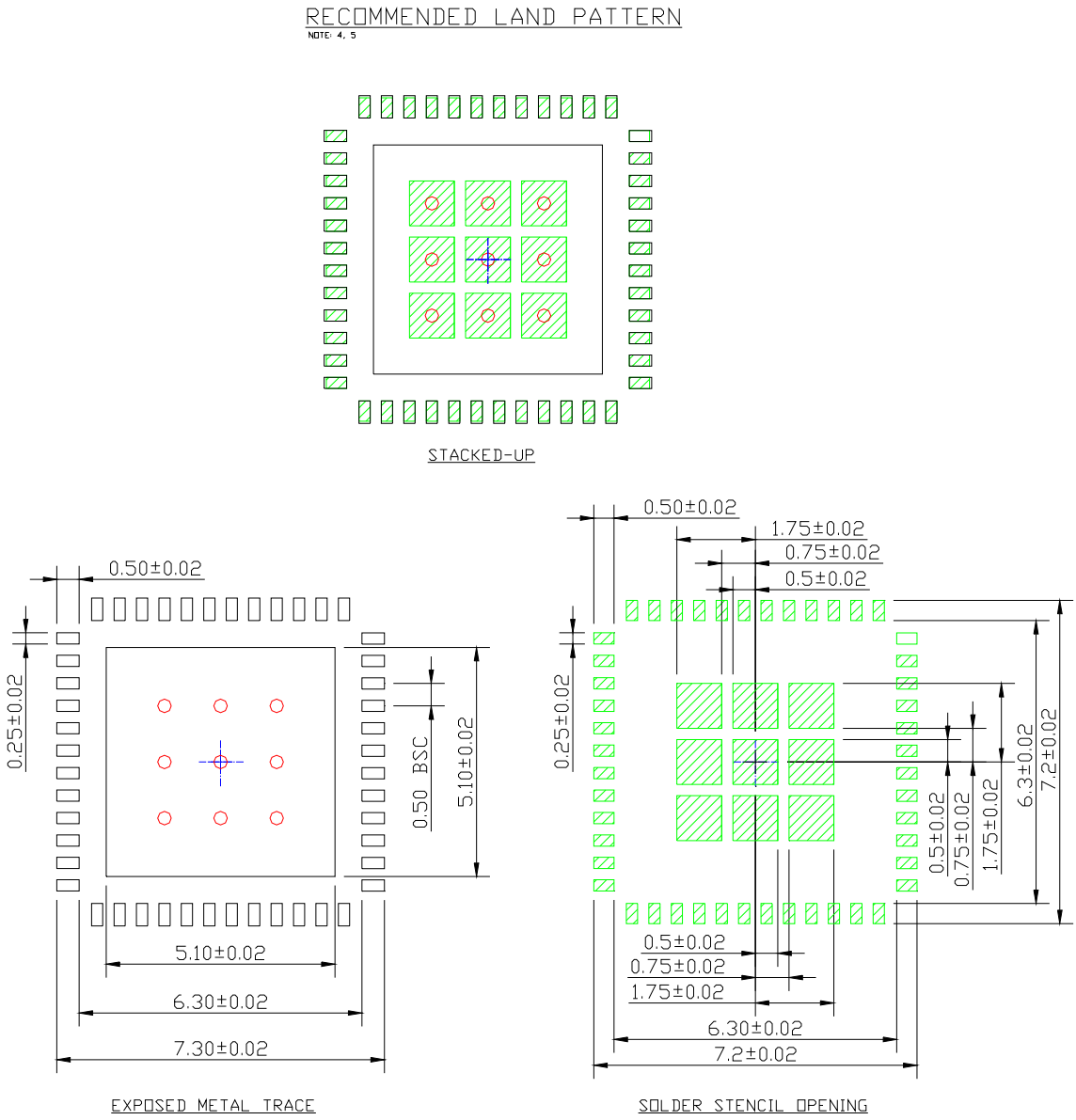


Side View
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. PITCH is 1.00mm.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.00x1.00mm, SPACING IS 0.25mm.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

POD-Land Pattern drawing #: QFN77-48LD-PL-1-C



NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2016)

- Initial release of data sheet.

Revision B (April 2016)

- Added maximum jitter value to Table 1-7.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	xxx	X	X	X	–	XX
Device	Part #	Power Supply	Package	Temperature		Shipping

Device:	SM813:		Flexible Ultra-Low Jitter Clock Synthesizer
Part #:	xxx	=	Factory-Assigned from User Design
Power Supply:	U	=	2.5V/3.3V
Package:	M	=	48-Pin 7 mm x 7 mm QFN
Temperature:	G	=	–40°C to +85°C
Shipping:	Blank TR	= =	Tray Tape & Reel

Package Options

Package Option:	#5, (Note 1)
QFN Package:	48-Pin, 7 mm x 7 mm
Number of Outputs:	8
OE Control:	Yes

Note 1: Use the ClockWorks Configurator web tool via the SM813xxx product page to determine the desired configuration. The desired configuration also determines the part number (xxx variable) that the factory assigns to the design.

Examples:

a) SM813xxxUMG: Flexible Ultra-Low Jitter Clock Synthesizer, Factory-Assigned Part Number, 2.5V/3.3V Power Supply, 48-Pin QFN, –40°C to +85°C Temp. Range, Tray Shipping

b) SM813xxxUMG-TR: Flexible Ultra-Low Jitter Clock Synthesizer, Factory-Assigned Part Number, 2.5V/3.3V Power Supply, 48-Pin QFN, –40°C to +85°C Temp. Range, Tape & Reel Shipping

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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