NPC

NIPPON PRECISION CIRCUITS LTD.

CMOS LSI SM8210S

Signal Processor for Paging Receivers

OVERVIEW

The SM8210S is a signal processor for paging receivers using the POCSAG (Post Office Code Standardization Advisory Group) coding system. The POCSAG coding system conforms to CCIR recommendation 584 concerning standard international wireless calling codes.

The SM8210S can receive messages containing tone, numeric and character data, and supports both 512 and 1200 bps data rates.

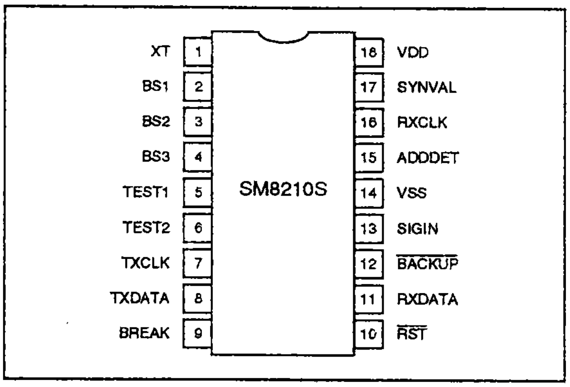
The SM8210S uses an intermittent reception technique that reduces power consumption, extending battery life.

The SM8210S operates from a 3 V supply and is available in 18-pin SOPs.

FEATURES

- POCSAG coding system support
- Battery saving mode
- Six main addresses
- 24 extension addresses
- Tone, numeric and character data capability
- Automatic correction of one- or two-bit burst errors
- 512 and 1200 bps data rates
- 25 to 75% duty cycle data capability when preamble pattern is detected
- Low-power Molygate® CMOS process
- 5 μA (typ) current consumption in preamble mode, and 3 μA (typ) in lock, idle and switch ON modes
- 3 V supply
- 18-pin SOPs

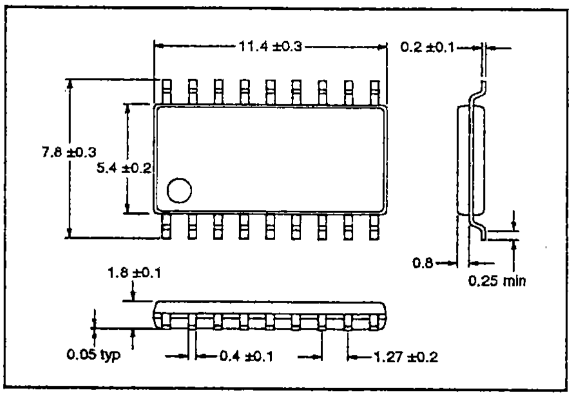
PINOUT



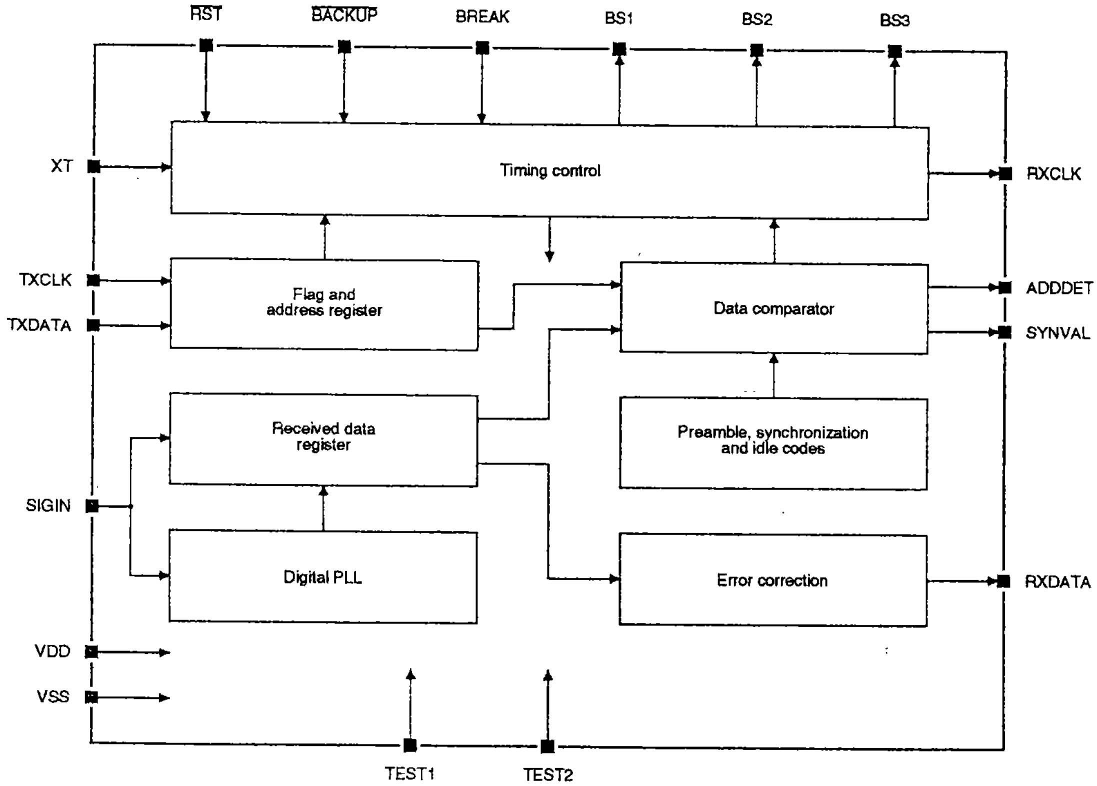
PACKAGE DIMENSIONS

Unit: mm

SOP18



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	XT	External 76.8 kHz clock input
2	BS1	RF circuitry battery control signal output 1
3	BS2	RF circuitry battery control signal output 2
4	BS3	PLL lock-up stabilization signal output
5	TEST1	Test input. This pin should be left open for normal operation.
6	TEST2	Test input. This pin should be left open for normal operation.
7	TXCLK	ID data read clock input
8	TXDATA	ID data input
9	BREAK	Message transfer halt input
10	$\overline{\text{RST}}$	Reset input
11	RXDATA	Receive data output
12	$\overline{\text{BACKUP}}$	Power-save mode control input
13	SIGIN	NRZ signal input
14	VSS	Ground
15	ADDDET	Address received detector output
16	RXCLK	Receive data clock output

Number	Name	Description
17	SYNVAL	Sync word received detector output
18	VDD	3 V supply

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_I	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Operating temperature range	T_{opr}	–20 to 70	deg. C
Storage temperature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{SLD}	260	deg. C
Soldering time	t_{SLD}	10	s

Recommended Operating Conditions

T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	3	V
Supply voltage range	V_{DD}	2.5 to 3.5	V

Electrical Characteristics

V_{DD} = 2.5 to 3.5 V, V_{SS} = 0 V, T_a = –20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	XT = 76.8 kHz. Lock, idle and switch ON modes	–	3.0	6.0	µA
		XT = 76.8 kHz, preamble mode	–	5.0	10.0	
Standby supply current	I_{DDS}	T_a = 25 deg. C	–	–	1.0	µA
LOW-level input voltage	V_{IL}		–	–	$0.2V_{DD}$	V
HIGH-level input voltage	V_{IH}		$0.8V_{DD}$	–	–	V
LOW-level output voltage	V_{OL}	I_{OL} = 20 µA	–	–	0.1	V
HIGH-level output voltage	V_{OH}	I_{OH} = –20 µA	V_{DD} – 0.1	–	–	V
Input leakage current	I_{LI}	V_I = V_{DD} or V_{SS}	–	–	±1.0	µA

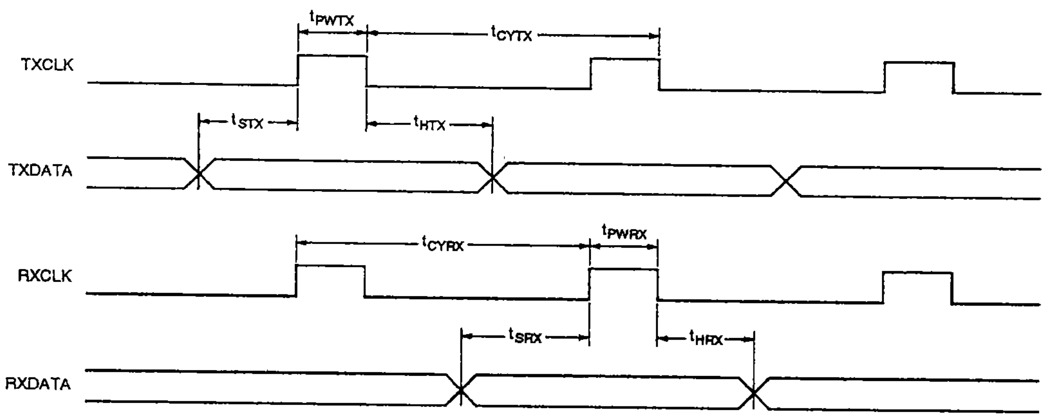
Timing Characteristics

V_{DD} = 2.5 to 3.5 V, V_{SS} = 0 V, T_a = –20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Transmit clock pulsewidth	t_{PWTX}		13	–	100	µs
Transmit clock cycle time	t_{CYTX}		450	–	–	µs
Transmit data setup time	t_{STX}		1.0	–	–	µs
Transmit data hold time	t_{HTX}		1.0	–	–	µs
XT pulse frequency	t_{CYXT}		76.8 –250 ppm	76.8	76.8 +250 ppm	kHz
XT pulse duty cycle	D_{XT}		25	–	75	%
BREAK pulsewidth	t_{PWBR}		13	–	–	µs
Receive clock cycle time. See note.	t_{CYRX}	512 bps	–	1953	–	µs
		1200 bps	–	833	–	
Receive clock pulsewidth. See note.	t_{PWRX}	512 bps	–	124	–	µs
		1200 bps	–	52	–	
Receive data lead time. See note.	t_{SRX}	512 bps	–	1341	–	µs
		1200 bps	–	573	–	
Receive data hold time. See note.	t_{HRX}	512 bps	–	488	–	µs
		1200 bps	–	208	–	

Note

Values vary slightly due to the operation of the internal, digital PLL.



FUNCTIONAL DESCRIPTION

Operating Flow

The overall operation of the SM8210S is outlined in the operating flow chart shown in figures 1, 2 and 3. The main features and functions are discussed below.

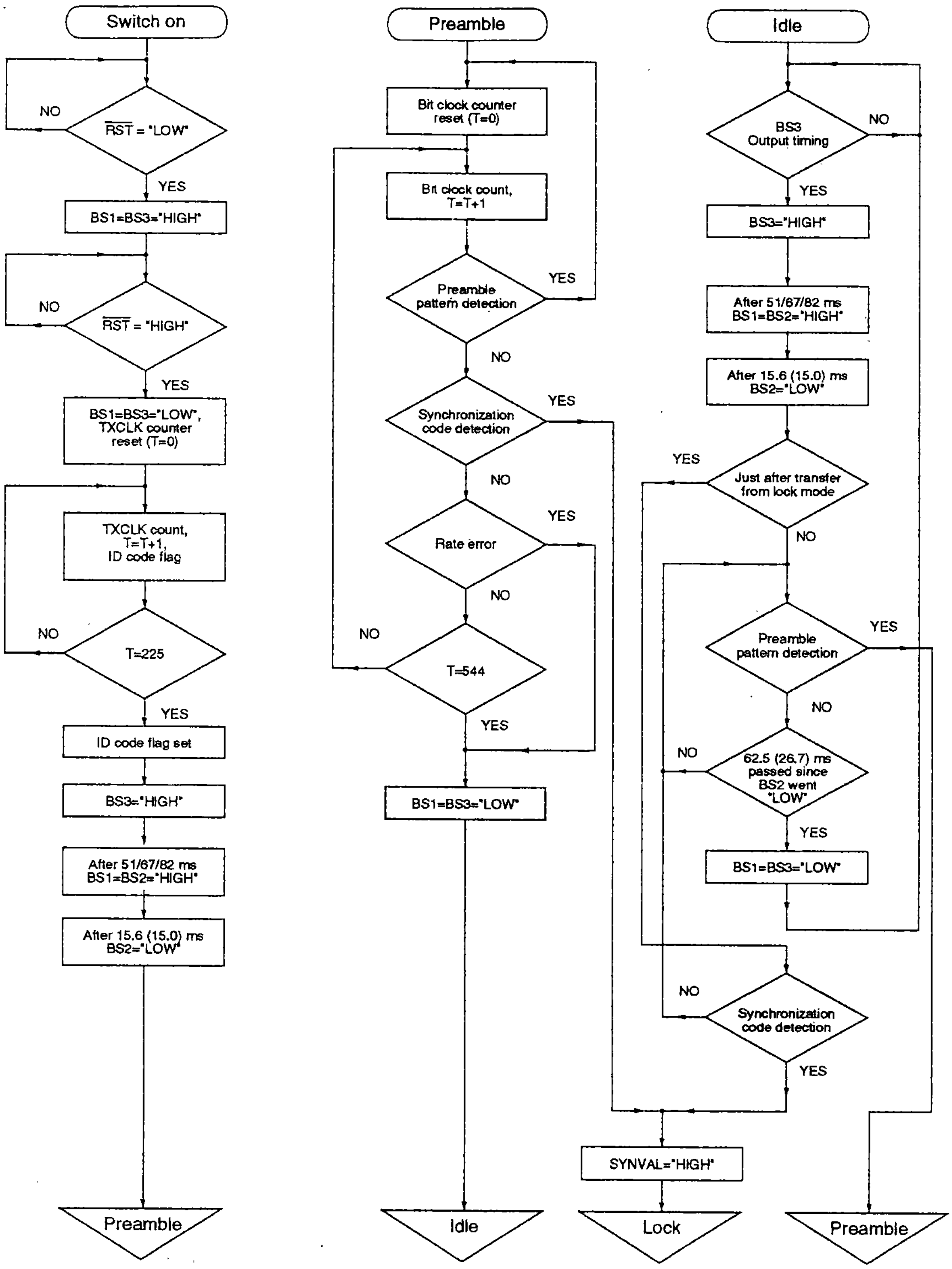


Figure 1. Switch ON, preamble and idle mode flow

Note

Data given refers to a baud rate of 512 bps. Data given in parentheses ( ) refers to a baud rate of 1200 bps.

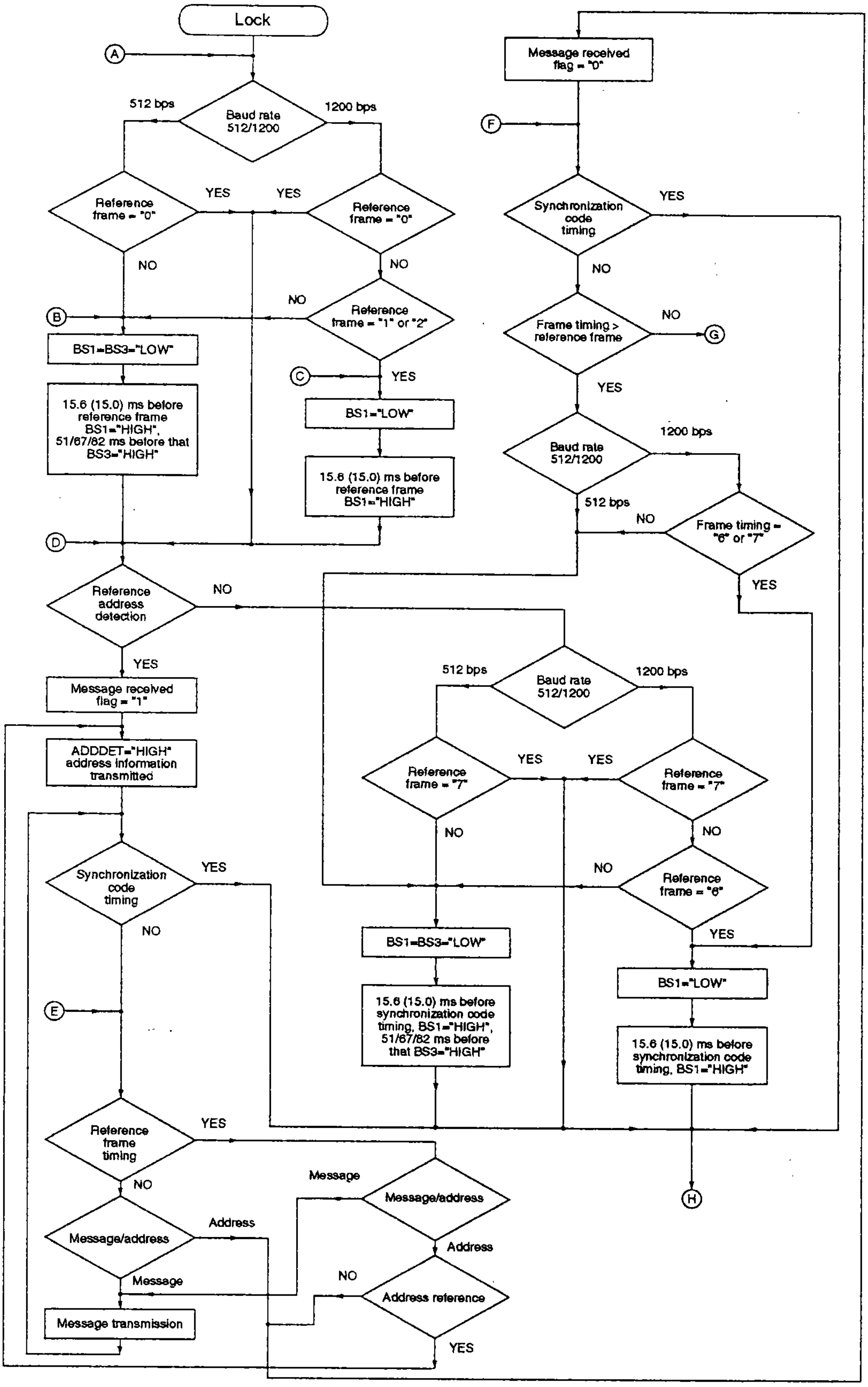


Figure 2. Lock mode flowchart

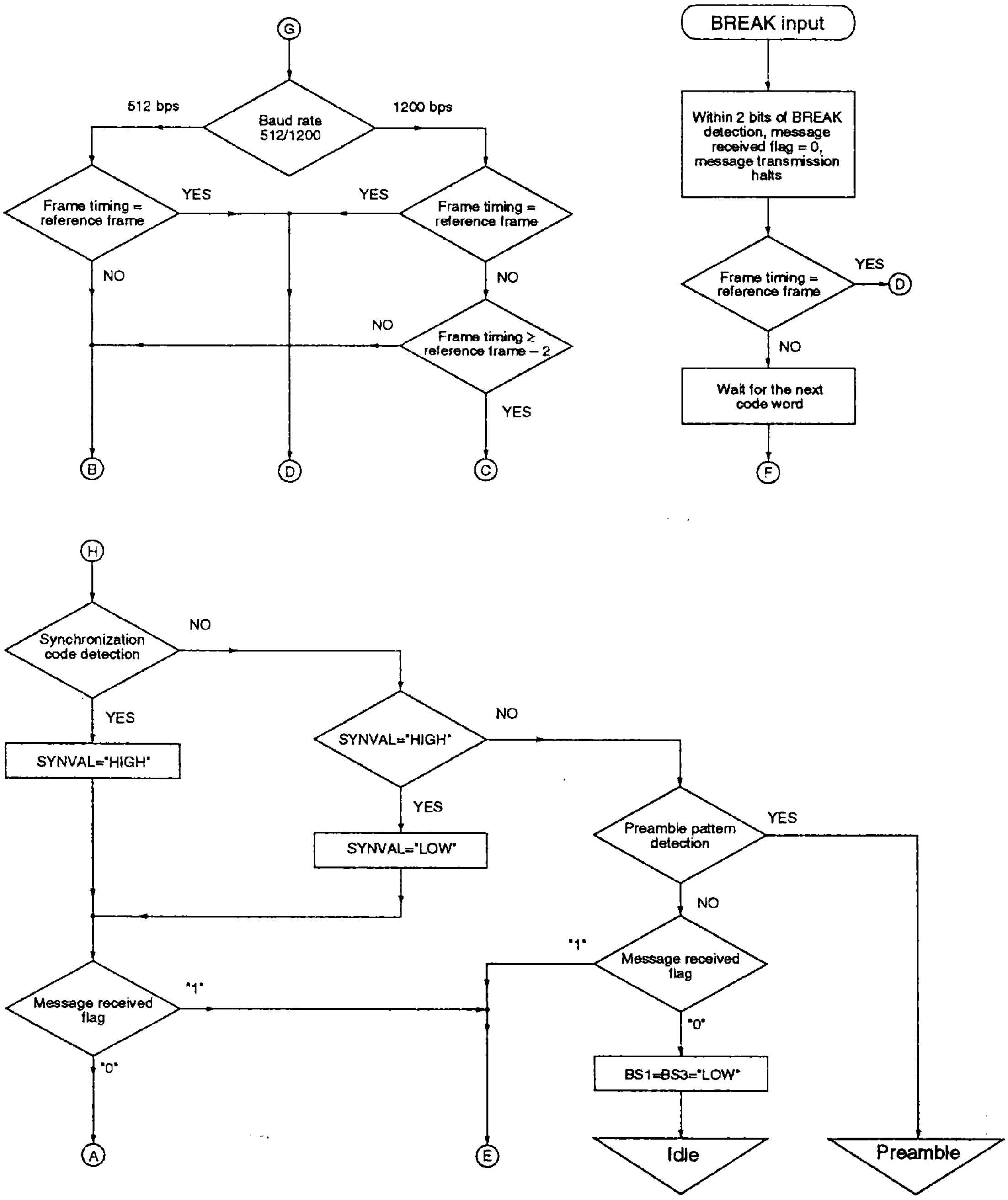


Figure 3. Lockmode flowchart (continued)

Data Format

The format of the received data is as per CCIR RPC No. 1 (POCSAG). The received data comprises preamble and synchronization code words and data frames as shown in figure 4.

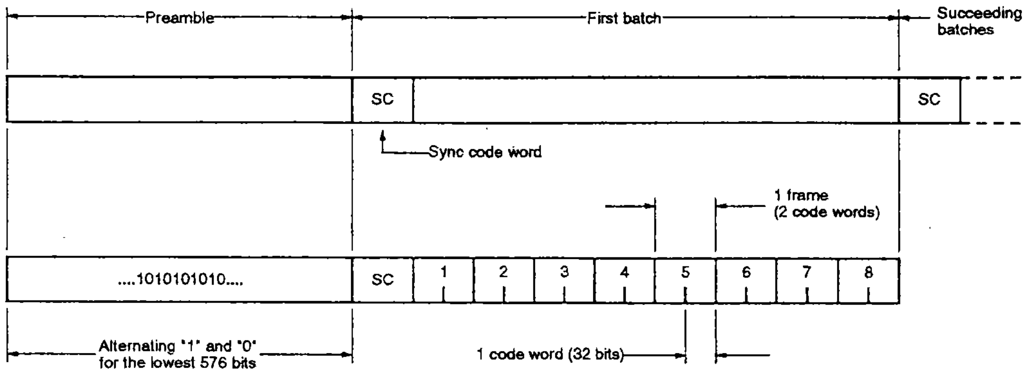


Figure 4. Data format

Synchronization code word

The synchronization code word allows the synchronization of the succeeding data words. It consists of a 31-bit M-type pattern followed by a single even-parity bit as shown in table 1.

Table 1. Synchronization code word

Bit No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Data	0	1	1	1	1	1	0	0	1	1	0	1	0	0	1	0
Bit No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Data	0	0	0	1	0	1	0	1	1	1	0	1	1	0	0	0

Address and message signal code words

Each code word comprises 32 bits, divided into several fields as shown in table 2. The fields comprise the following.

- One bit (msb) to distinguish between the address word and the message word
- An address corresponding to the call number assigned to the subscriber's receiver
- Two function bits
- A message field
- A BCH (31, 21) check code, in the form BCH (n, k) where n is the code length and k is the number of data bits
- An even-parity bit

Table 2. Data frame configuration

Data type	Bit number				
	1 (msb)	2 to 19	20 to 21	22 to 31	32 (lsb)
Address code word	0	Address field	Function bits	Check bits	Even-parity bit
Message code word	1	Message field		Check bits	Even-parity bit

Table 3. Function bits

Function	Bit 20	Bit 21
A call	0	0
B call	0	1

Table 3. Function bits—continued

Function	Bit 20	Bit 21
C call	1	0
D call	1	1

Call number and code conversion

The call number is converted into an address signal (call code) by expanding the 7-digit decimal call number into a 21-bit binary call code. The frame type is defined by the three least-significant bits of the call code, F1 to F3. The call code is then written into the ID-ROM.

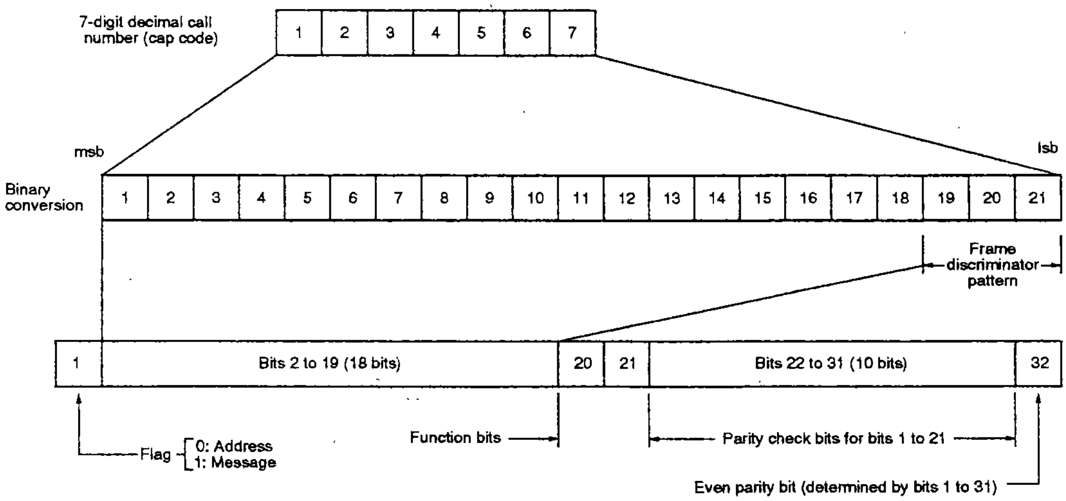


Figure 5. Call number and call code

The identifier flag (bit 1) is set to zero to indicate that this is an address word. Bits 2 to 19 are the 18-bit call code, and bits 20 and 21 are the function bits.

Table 4. Frame type codes

Frame type	Frame code		
	F3	F2	F1
Frame 0	0	0	0
Frame 1	0	0	1
Frame 2	0	1	0
Frame 3	0	1	1
Frame 4	1	0	0
Frame 5	1	0	1
Frame 6	1	1	0
Frame 7	1	1	1

Idle word

An idle word can be inserted into either the address or message word to indicate that the word contains no information. The idle word bit pattern is shown in table 5. Message reception is halted when the receiver detects an idle word. In pager systems that send numeric data, the number of frames varies with the type of message being sent. In this case, an idle signal is transmitted to indicate completion of the message.

Table 5. Idle code word

Bit No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Data	0	1	1	1	1	0	1	0	1	0	0	0	1	0	0	1
Bit No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Data	1	1	0	0	0	0	0	1	1	0	0	1	0	1	1	1

Received signal duty cycle

The preamble signal, an alternating pattern of 0 and 1 bits, is received if the duty cycle is between 25 and 75%.

Battery Saving Operation

Battery consumption is reduced by controlled intermittent receive operation using BS1, BS2 and BS3. The functions of BS1, BS2 and BS3 are determined by the operating mode.

BS1 Main RF control output signal. RF turns ON when BS1 goes HIGH.

BS2 RF discharge output control signal. BS2 goes HIGH with BS1 and then goes LOW again 15.8 ms later (15.0 ms at 1200 bps). In lock mode, BS2 remains LOW.

BS3 PLL start control output signal, when a PLL is used. BS3 goes HIGH before BS1 and then goes LOW with BS1. The BS3 to BS1 lead time is set by a CPU operation using flags PL1 and PL2.

Operating Modes

Switch ON mode

After power ON, the internal registers are reset by taking $\overline{RST}$ LOW. The registers can then be initialized by writing six addresses comprising 18 bits and 7-bit flag data synchronized with TXCLK and TXDATA. The data on TXDATA is transmitted over 32 × 7 + 1 TXCLK cycles. The operating mode changes to preamble mode after 225 TXCLK cycles, setting BS1, BS2 and BS3.

Flag	Function
PL1, PL2	PLL lock-up time select
INV	Input signal invert select
LBO	512 or 1200 bps select
F1, F2, F3	Frame select

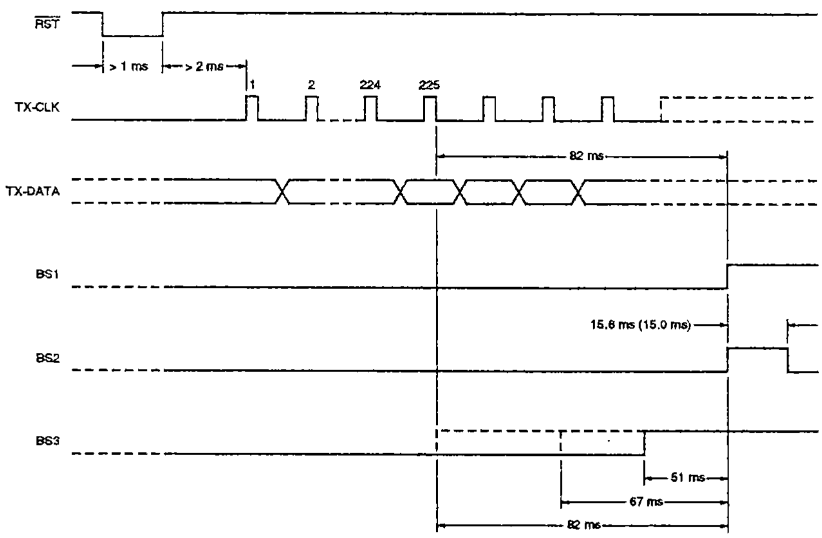


Figure 6. Switch ON mode timing

Preamble mode

Preamble operating mode continues for a length of 544 bits and then changes to idle mode if none of the following are detected.

- A preamble pattern. If detected, preamble mode continues for a further 544 bits.
- A rate error. A rate error occurs if two SIGIN edges occur within a single bit period. If two such errors occur consecutively, the operating mode changes to idle mode immediately.
- A synchronization code. A synchronization code is detected if two bit errors or less occur. If detected, the operating mode changes to lock mode, setting SYNVAL to HIGH.

During preamble mode, BS1 and BS3 remain HIGH.

Idle mode

When $BS1 \cdot \overline{BS2}$ is HIGH during idle mode, the SM8210S checks for the presence of a preamble signal. If detected, the operating mode changes to preamble mode. If not detected, intermittent operation continues.

A preamble signal is detected when the 6-bit pattern 101010 occurs. This detection method ensures that incorrect mode switching does not occur due to weak electric fields or noise. This pattern can also be included in other transmitted signals to facilitate easier mode switching.

When the operating mode changes from lock mode to idle mode, the SM8210S checks for a synchronization code without setting BS2. If a synchronization code is detected, the operating mode returns to lock mode.

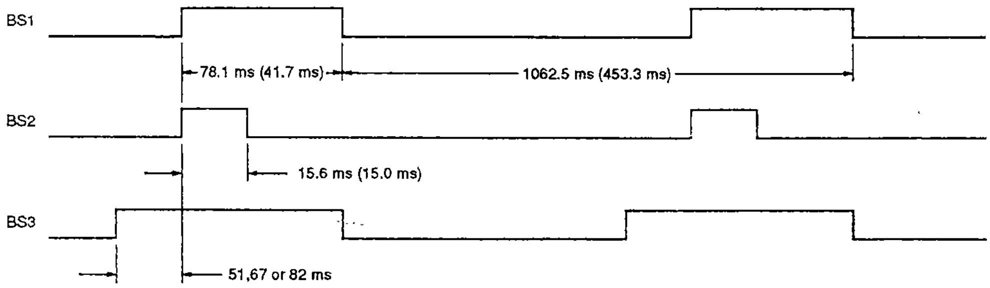


Figure 7. Idle mode timing

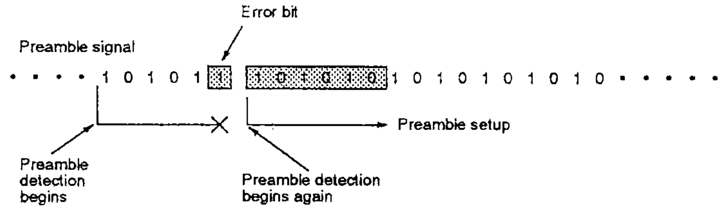


Figure 8. Preamble code sequence

Lock mode

If a synchronization code is detected during preamble mode, the operating mode changes to lock mode and BS1 goes LOW. When the frame specified by the flag data occurs, BS1 goes HIGH and the received data is compared with the 24 addresses. Note that if the frame number is zero, BS1 remains HIGH.

A match occurs if there are two bit errors or less. The comparison is made twice since each frame comprises two code words. BS1 goes LOW if there is no match and the synchronization code detect state is reset. If the synchronization code cannot be detected twice consecutively, the operating mode changes to idle mode and remains in lock mode during message reception.

If the synchronization code is not detected a second time but instead the preamble pattern is detected, the operating mode changes to preamble mode.

If one of the 24 addresses compared matches, ADDDET goes HIGH during the next code word, and the data in that address is sent to the CPU on RXDATA, which is synchronized to RXCLK. If the data following an address is confirmed to be a message, BS1 is held HIGH and the message is then received. After error correction, the received message is sent to the CPU on RXDATA, again synchronized with RXCLK, as a 23-bit word comprising 20-bit data, 2-bit error correction code and 1-bit even parity check. If a message spans two or more batches, then a synchronization code detection is carried out during reception. Message reception terminates when another address or idle code is detected, or when an interrupt occurs on BREAK. When reception terminates, BS1 goes LOW and the SM8210S waits for the synchronization code or an address for the next reference frame.

Mode change summary

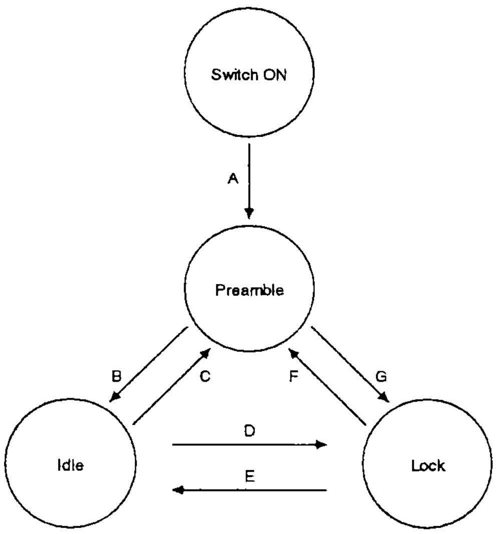


Figure 9. Operating mode switching

Notes

A The ID code, synchronized to TXCLK, is read after $\overline{RST}$ goes LOW.
B A rate error is detected, or neither a preamble pattern nor synchronization code is detected within a fixed time.
C Preamble pattern is detected.
D Synchronization code is detected during the first cycle after changing from lock mode.
E Synchronization code is not detected twice consecutively.
F Preamble pattern is detected instead of a second synchronization code.
G Synchronization code is detected.

Address/Flag Data Transfer

After initialization ($\overline{RST}$ goes LOW), the address/flag data is transferred from the CPU to the SM8210S on TXDATA on the falling edge of each of the 225 TXCLK pulses.

The SM8210S supports six, independent, 18-bit addresses (A, B, C, D, E and F) for handling various group calls. Each address is expanded into four extension addresses by adding two function bits to each address. Also, one 0 bit (most significant bit) to indicate that it is an address, ten parity bits for BCH (31, 21) format and one even-parity bit are added. These addresses are then stored in RAM as twenty-four 32-bit addresses to be compared with the received data.

Data is input into each address, most significant bit first. If less than the six addresses are used, data for the address used last should be copied into the remaining addresses.

The data corresponding to each TXCLK pulse is shown in table 6, PLL lock-up time in table 7, and the baud rate and inverting selection in table 8.

Table 6. ID and flag format

TX clock	Data	TX clock	Data	TX clock	Data	TX clock	Data	TX clock	Data
1	0	46	AA4	91	0	136	AD10	181	0
2	0	47	AA3	92	0	137	AD9	182	0
3	0	48	AA2	93	0	138	AD8	183	0
4	0	49	AA1	94	0	139	AD7	184	0
5	0	50	AA0	95	0	140	AD6	185	0
6	0	51	0	96	0	141	AD5	186	0
7	0	52	0	97	AC17	142	AD4	187	0
8	0	53	0	98	AC16	143	AD3	188	0
9	0	54	0	99	AC15	144	AD2	189	0
10	0	55	0	100	AC14	145	AD1	190	0
11	0	56	0	101	AC13	146	AD0	191	0
12	0	57	0	102	AC12	147	0	192	0
13	0	58	0	103	AC11	148	0	193	AF17
14	0	59	0	104	AC10	149	0	194	AF16

Table 6. ID and flag format—continued

TX clock	Data	TX clock	Data	TX clock	Data	TX clock	Data	TX clock	Data
15	0	60	0	105	AC9	150	0	195	AF15
16	0	61	0	106	AC8	151	0	196	AF14
17	0	62	0	107	AC7	152	0	197	AF13
18	0	63	0	108	AC6	153	0	198	AF12
19	0	64	0	109	AC5	154	0	199	AF11
20	0	65	AB17	110	AC4	155	0	200	AF10
21	1	66	AB16	111	AC3	156	0	201	AF9
22	0	67	AB15	112	AC2	157	0	202	AF8
23	0	68	AB14	113	AC1	158	0	203	AF7
24	0	69	AB13	114	AC0	159	0	204	AF6
25	PL1	70	AB12	115	0	160	0	205	AF5
26	PL2	71	AB11	116	0	161	AE17	206	AF4
27	INV	72	AB10	117	0	162	AE16	207	AF3
28	LB0	73	AB9	118	0	163	AE15	208	AF2
29	F1	74	AB8	119	0	164	AE14	209	AF1
30	F2	75	AB7	120	0	165	AE13	210	AF0
31	F3	76	AB6	121	0	166	AE12	211	0
32	0	77	AB5	122	0	167	AE11	212	0
33	AA17	78	AB4	123	0	168	AE10	213	0
34	AA16	79	AB3	124	0	169	AE9	214	0
35	AA15	80	AB2	125	0	170	AE8	215	0
36	AA14	81	AB1	126	0	171	AE7	216	0
37	AA13	82	AB0	127	0	172	AE6	217	0
38	AA12	83	0	128	0	173	AE5	218	0
39	AA11	84	0	129	AD17	174	AE4	219	0
40	AA10	85	0	130	AD16	175	AE3	220	0
41	AA9	86	0	131	AD15	176	AE2	221	0
42	AA8	87	0	132	AD14	177	AE1	222	0
43	AA7	88	0	133	AD13	178	AE0	223	0
44	AA6	89	0	134	AD12	179	0	224	0
45	AA5	90	0	135	AD11	180	0	225	0

Table 7. PLL lock-up time selection

PLn flag		Lock-up time	Unit
PL1	PL2		
0	0	51	ms
1	0	67	ms
0	1	82	ms

Table 8. Baud rate and signal inversion selection

LBO	INV	Baud rate	Input
0	0	1200 bps	Non-inverting input
0	1	1200 bps	Inverting input
1	0	512 bps	Non-inverting input
1	1	512 bps	Inverting input

Received Data Transfer

In lock mode, if the received data in the frame specified by the frame flags contains two or less bit errors and matches one of the 24 addresses, then ADDDET will go HIGH during the next code word length and the 5-bit data in that address will be sent on TXDATA to the CPU, synchronized with RXCLK.

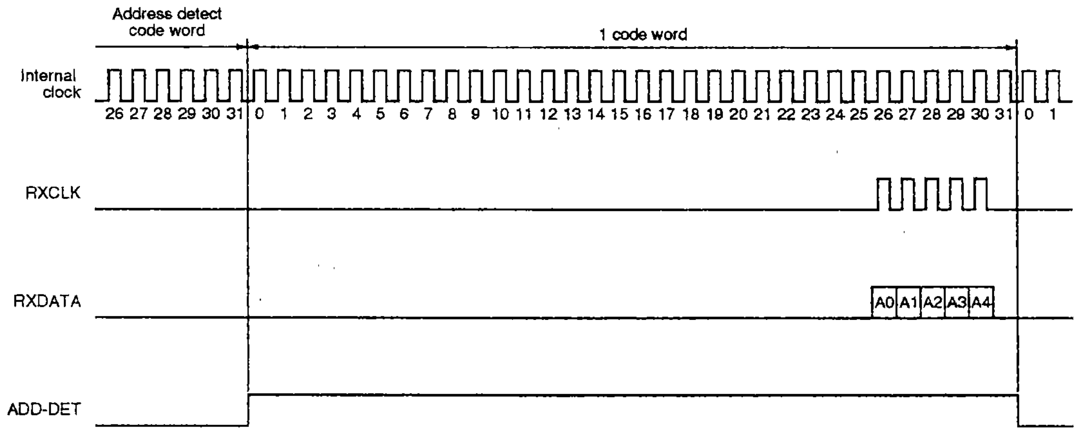


Figure 10. Received address data timing

Table 9. Address flags

A0	A1	A2	A3	A4	Address	Function bit	A0	A1	A2	A3	A4	Address	Function bit
0	0	1	0	0	A	A call	0	0	0	0	1	D	A call
1	0	1	0	0		B call	1	0	0	0	1		B call
0	1	1	0	0		C call	0	1	0	0	1		C call
1	1	1	0	0		D call	1	1	0	0	1		D call
0	0	0	1	0	B	A call	0	0	1	0	1	E	A call
1	0	0	1	0		B call	1	0	1	0	1		B call
0	1	0	1	0		C call	0	1	1	0	1		C call
1	1	0	1	0		D call	1	1	1	0	1		D call
0	0	1	1	0	C	A call	0	0	0	1	1	F	A call
1	0	1	1	0		B call	1	0	0	1	1		B call
0	1	1	1	0		C call	0	1	0	1	1		C call
1	1	1	1	0		D call	1	1	0	1	1		D call

When an address is detected, the 32-bit data for the next code word is received. An error check is made using BCH (31, 21) format, and single-bit and two consecutive bit errors are corrected. Random 2-bit errors and 3-bit or more errors are not corrected. After correction, if the most significant bit is a 1, the data is a message and is sent to the CPU together with an error check flag. If the most significant bit is a 0, the data is an address or idle code, and data reception and data transfer to the CPU are stopped.

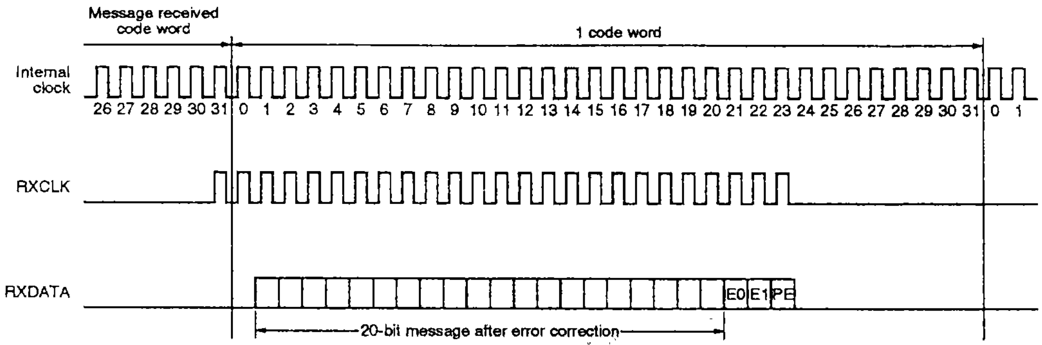


Figure 11. Received message transfer timing

Table 10. Error flags

Error count	Error flags	
	E0	E1
None	0	0
One error	1	0
Two consecutive bits	0	1
Two or more random bits, or three or more consecutive bits	1	1

Table 11. Parity flag

Parity check	Flag
	PE
No error	0
Error before BCH correction	1

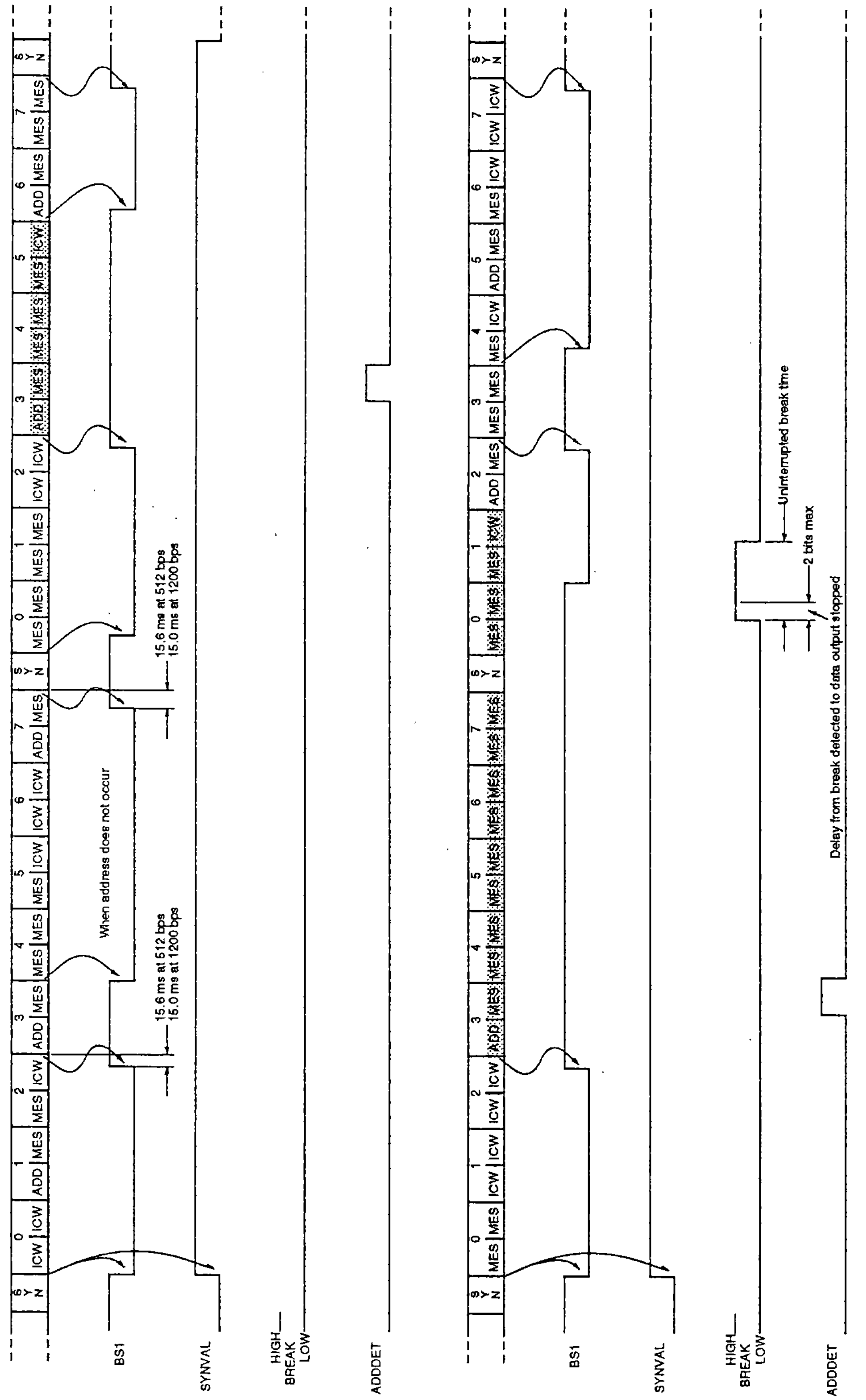


Figure 12. Interface timing

CPU Interfaces

Synchronization word detection

When a synchronization code is detected, if there are two or less error bits, SYNVAL goes HIGH during the next 544-bit cycle.

Address detection

In lock mode, if the data received in the frame matches an address with two or less bit errors, then ADDDET remains HIGH during the next code word. If consecutive matching addresses are detected, ADDDET is HIGH for two code words.

Receive data interrupt

The CPU halts data transmission from the SM8210S when BREAK goes HIGH. The SM8210S then stops receiving data and changes to the synchronization code detect state.

Extended Reset

If $\overline{RST}$ is held LOW for more than 1 or 2 ms, then BS1 and BS3 go HIGH and stay HIGH until 1 or 2 ms after $\overline{RST}$ goes HIGH again. This period is used to check the RF circuit operation. After $\overline{RST}$ goes HIGH, the ID code input state is active. See figure 6.

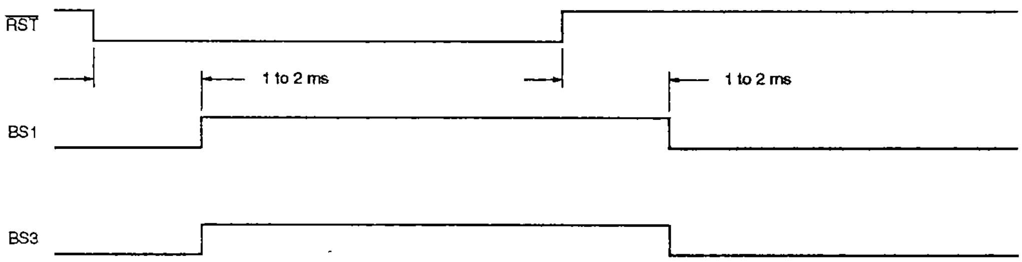


Figure 13. Reset timing

Power Saving Control

When $\overline{BACKUP}$ goes LOW, internal operation halts and all outputs become high impedance. To recover, it is necessary to set the ID code and initialize the device.

Transmitting data

If $\overline{BACKUP}$ goes LOW while transmitting data on TXDATA, TXCLK should not be halted until the ID code has been read. Similarly, the XT clock should not be halted until at least one bit period (150 cycles at 512 bps or 64 cycles at 1200 bps) after reading the ID code.

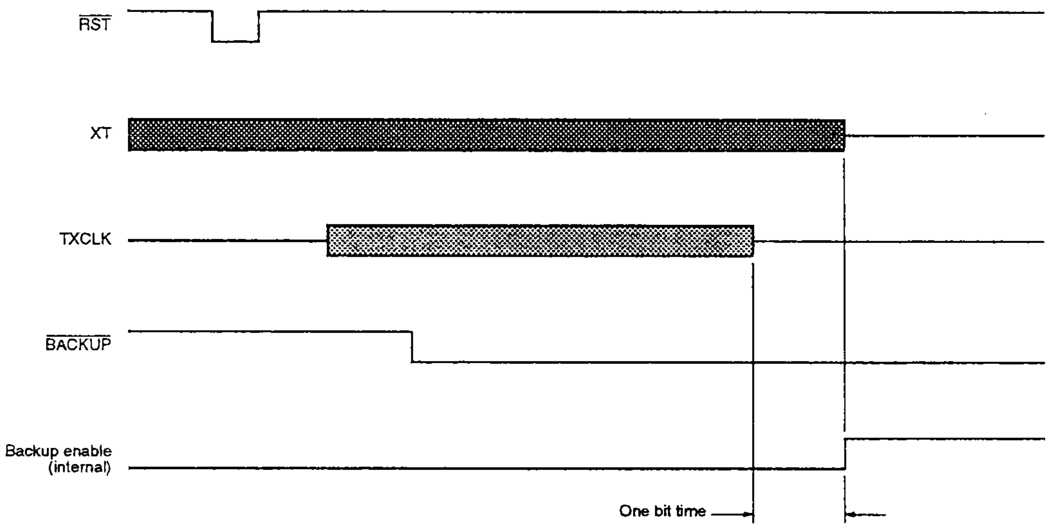
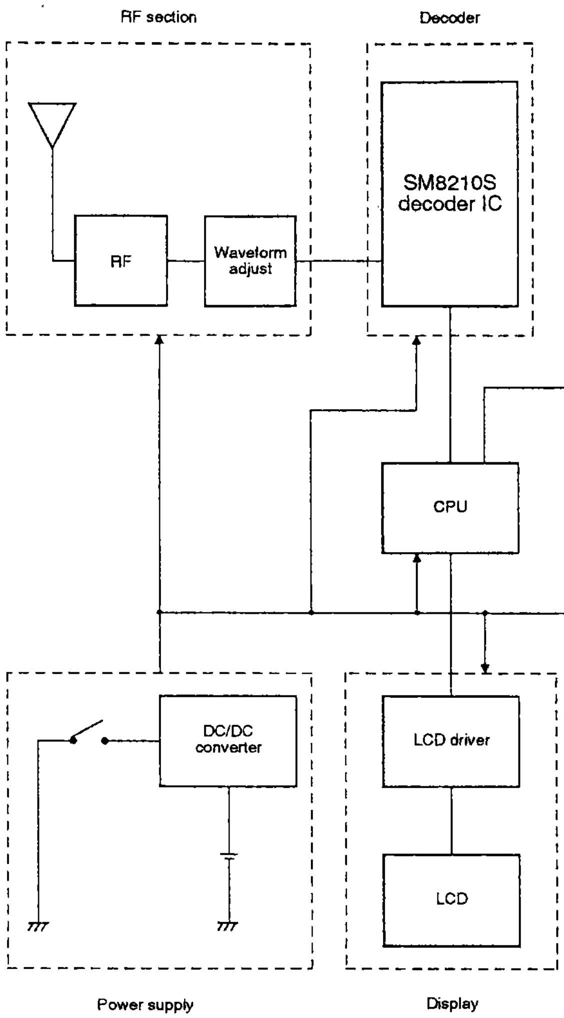


Figure 14. $\overline{BACKUP}$ during data transmission

Under other conditions

If $\overline{BACKUP}$ goes LOW under any conditions, excluding during data transmission, the XT clock should continue for a minimum period of 65 bits.

TYPICAL APPLICATION



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NC9210A 1992.06