NIPPON PRECISION CIRCUITS INC.

SM8701BM

DVD Player Clock Generator

OVERVIEW

The SM8701BM is a 27 MHz master clock, 5-system output clock generator for DVD players. It has 2 built-in PLLs that, with the addition of a single crystal oscillator element, can generate 256fs, 384fs and 768fs clocks plus independent fixed-frequency 27 MHz and 33.8688 MHz output clocks. Supported sampling frequencies (fs) include the standard 32, 44.1 or 48 kHz, or double-frequency 64, 88.2 or 96 kHz.

FEATURES

- 27 MHz master clock (internal PLL reference clock)
- Generated clocks
  - 27 MHz output
  - 33.8688 MHz output
  - 256fs output
  - 384fs output
  - 768fs output
- Sampling frequency fs
  - 32/64 kHz
  - 44.1/88.2 kHz
  - 48/96 kHz
- Low jitter output
- 3-wire serial or parallel control
- Supply voltage: $V_{DD} = V_{DDP} = 5.0V$
  $V_{DDO} = V_{DD3} = 3.3V$
- 20-pin SSOP package

APPLICATIONS

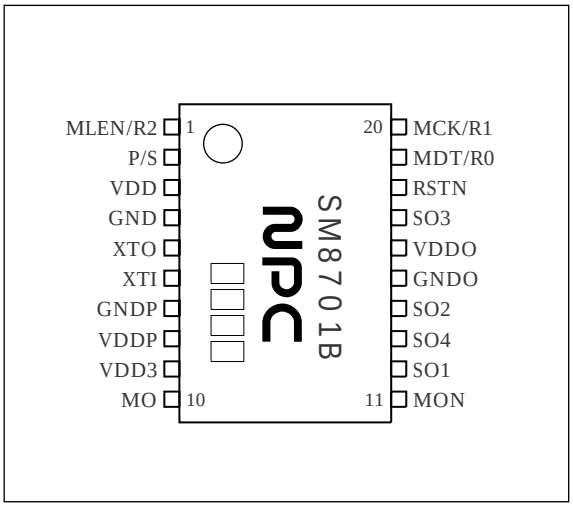
- DVD players

ORDERING INFORMATION

Device	Package
SM8701BM	20-pin SSOP

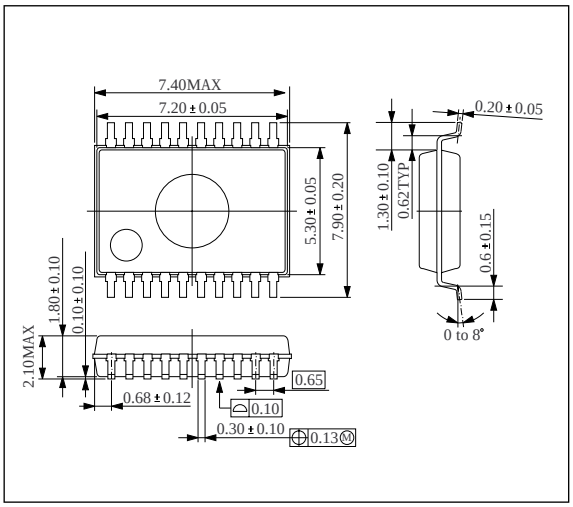
PINOUT

(Top View)

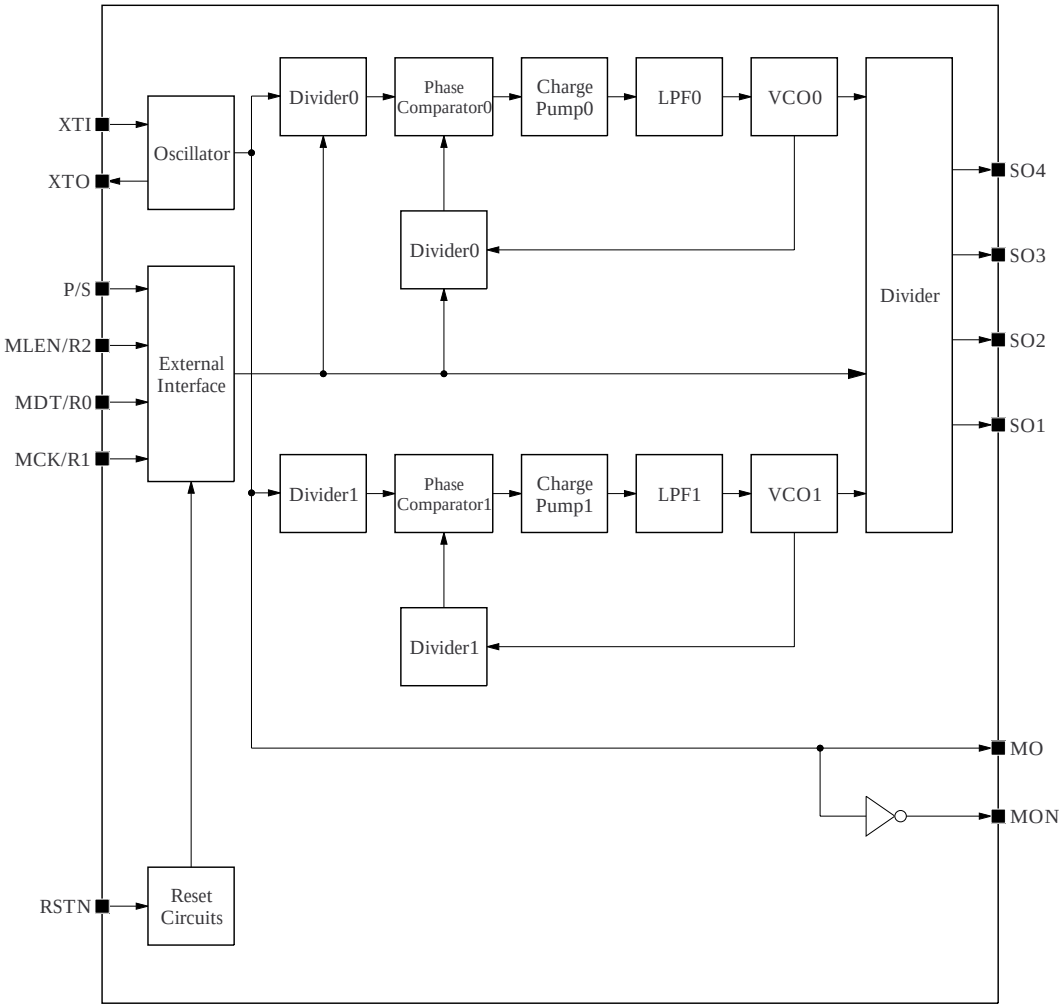


PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	MLEN/R2	Ip[1]	Control signal input. In serial mode: latch enable signal In parallel mode: sampling rate select signal
2	P/S	Ip[1]	Mode select signal. LOW: serial mode, HIGH: parallel mode
3	VDD	–	5 V supply (Digital block)
4	GND	–	Ground (Digital block)
5	XTO	O	Reference signal crystal oscillator element connection
6	XTI	I	Reference signal crystal oscillator element connection or external clock input
7	GNDP	–	Ground (PLL block)
8	VDDP	–	5 V supply (PLL block)
9	VDD3	–	3.3 V supply (output buffer)
10	MO	O	27 MHz fixed-frequency output
11	MON	O	27 MHz fixed-frequency output (inverted)
12	SO1	O	33.8688 MHz fixed-frequency output
13	SO4	O	768fs output
14	SO2	O	256fs output
15	GNDO	–	Ground (output buffer)
16	VDDO	–	3.3 V supply (output buffer)
17	SO3	O	384fs output
18	RSTN	Ip[2]	LOW-level reset input
19	MDT/R0	Ip[1]	Control signal input. In serial mode: control data input signal In parallel mode: sampling frequency select signal
20	MCK/R1	Ip[1]	Control signal input. In serial mode: clock signal In parallel mode: sampling frequency select signal

1. Schmitt trigger input with pull-down resistor
2. Schmitt trigger input with pull-up resistor

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}, V_{DDP}, V_{DDO}, V_{DD3}		–0.3 to 6.5	V
Supply voltage deviation	$V_{DD} - V_{DDP}$, $V_{DDO} - V_{DD3}$, GND – GNDP, GND – GNDO, GNDP – GNDO		±0.1	V
Input voltage range	V_{IN}	Digital inputs	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	Digital outputs	–0.3 to V_{DDO}, V_{DD3} + 0.3	V
Power dissipation	P_D		300	mW
Storage temperature range	T_{stg}		–55 to 125	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	Rating	Unit
Supply voltage ranges	V_{DDO}, V_{DD3}		2.7 to 3.6	V
	V_{DD}, V_{DDP}		4.5 to 5.5	V
Operating temperature range	T_{opr}		–40 to 85	°C

DC Electrical Characteristics

External clock, T_a = –40 to 85 °C, $V_{DD} = V_{DDP}$ = 4.5 to 5.5 V, $V_{DDO} = V_{DD3}$ = 2.7 to 3.6 V unless otherwise stated

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	All supplies. $V_{DD} = V_{DDP}$ = 5.0V, $V_{DDO} = V_{DD3}$ = 3.3 V, T_a = 25 °C, fs = 48 kHz, using XTI external 27 MHz master clock, no load on clock outputs (MO, MON, SO1 to SO4)	–	32	45	mA
HIGH-level input voltage	V_{IH1}	P/S, MLEN/R2, MCK/R1, MDT/R0, RSTN	2.0	–	–	V
LOW-level input voltage	V_{IL1}	P/S, MLEN/R2, MCK/R1, MDT/R0, RSTN	–	–	0.8	V
HIGH-level input voltage	V_{IH2}	XTI	$0.7 \times V_{DD}$	–	–	V
LOW-level input voltage	V_{IL2}	XTI	–	–	$0.3 \times V_{DD}$	V
HIGH-level input current[1]	I_{IH1}	$V_{IN} = V_{DD}$	–	–	150	µA
LOW-level input current[1]	I_{IL1}	V_{IN} = 0 V	–	–	–1	µA
HIGH-level input current[2]	I_{IH2}	$V_{IN} = V_{DD}$	–	–	1	µA
LOW-level input current[2]	I_{IL2}	V_{IN} = 0 V	–	–	–150	µA
HIGH-level input current	I_{IH3}	XTI, $V_{IN} = V_{DD}$	–	–	40	µA
LOW-level input current	I_{IL3}	XTI, V_{IN} = 0 V	–	–	–40	µA
HIGH-level output voltage	V_{OH}	All outputs. I_{OH} = –2 mA	$V_{DDO} - 0.4$	–	–	V
LOW-level output voltage	V_{OL}	All outputs. I_{OL} = 4 mA	–	–	0.4	V

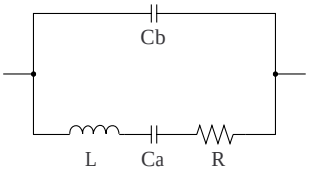
1. P/S, MLEN/R2, MCK/R1, MDT/R0. Schmitt trigger input, internal pull-down.
2. RSTN. Schmitt trigger input, internal pull-up.

PLL AC Electrical Characteristics

External clock, T_a = –40 to 85 °C, $V_{DD} = V_{DDP}$ = 4.5 to 5.5 V, $V_{DDO} = V_{DD3}$ = 2.7 to 3.6 V unless otherwise stated

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI external input clock frequency	f_M	DUTY: 50 ± 5%	–	27.0000	–	MHz
Output clock rise time	t_R	All outputs, 0.2 to 0.8V_{DDO} or V_{DD3}, C_L = 20 pF	–	2.5	–	ns
Output clock fall time	t_F	All outputs, 0.8 to 0.2V_{DDO} or V_{DD3}, C_L = 20 pF	–	2.5	–	ns
MO, MON output clock jitter[1]	JITTER	Standard tolerance Crystal oscillator element	–	150	–	ps
SO1, SO2 (Standard), SO3, SO4 output clock jitter[1]			–	150	–	ps
SO2 (Double) output clock jitter[1]			–	450	–	ps
MO, MON output clock duty[1]	DUTY	Crystal oscillator element, C_L = 20 pF	45	50	55	%
SO1, SO2 (Standard), SO3, SO4 output clock duty[1]		C_L = 20 pF	40	50	60	%
SO2 (Double) output clock duty[1]		C_L = 20 pF	23.3	33.3	43.3	%
Settling time	t_S	All outputs	–	–	40	ms
Power-up time[2]	t_P	All outputs	–	–	50	ms
RSTN external reset LOW-level pulsewidth	t_{RSTL}	1.4 V to 1.4 V	100	–	–	ns

1. 1.4V to 1.4V. Ta=20°C. The characteristics of output clock jitter and output clock duty depends on crystal oscillator.
   NPC's standard crystal oscillator: R = 10.5 Ω, L = 5.38 mH, Ca = 6.74 fF, Cb = 1.85 pF
   measurement apparatus: HP4195
   Load capacitance: C1 = 7 pF, C2 = 11 pF



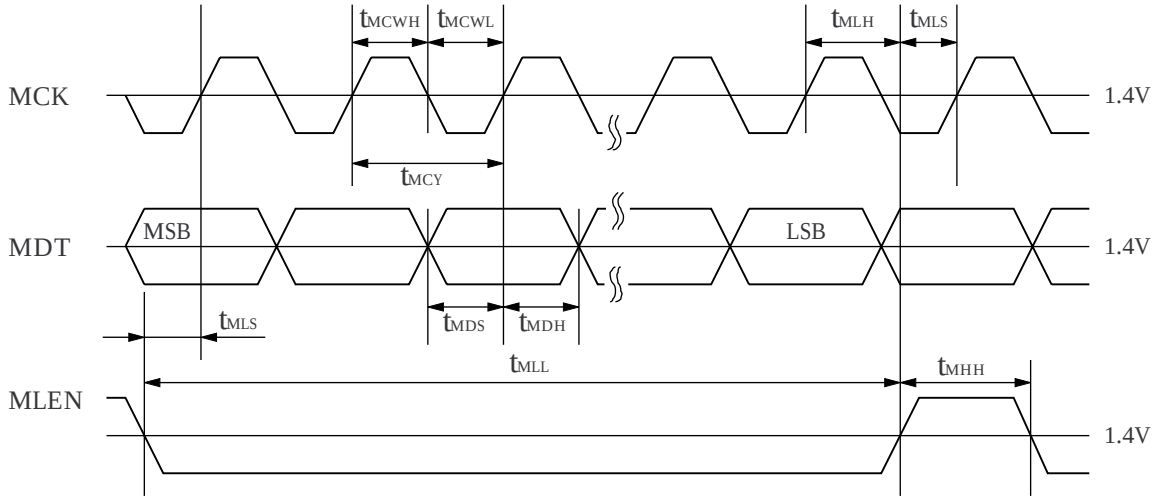
2. Time from OFF condition to stable frequency output.

Serial Interface AC Characteristics

External clock, T_a = –40 to 85 °C, $V_{DD} = V_{DDP}$ = 4.5 to 5.5 V, $V_{DDO} = V_{DD3}$ = 2.7 to 3.6 V unless otherwise stated

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
MCK HIGH-level pulsewidth	t_{MCWH}		40	–	–	ns
MCK LOW-level pulsewidth	t_{MCWL}		40	–	–	ns
MCK pulse cycle time	t_{MCY}		100	–	–	ns
MDT setup time	t_{MDS}		40	–	–	ns
MDT hold time	t_{MDH}		40	–	–	ns
MLEN setup time[1]	t_{MLS}		40	–	–	ns
MLEN hold time[2]	t_{MLH}		40	–	–	ns
MLEN HIGH-level pulsewidth	t_{MHH}		200	–	–	ns
MLEN LOW-level pulsewidth	t_{MLL}		$16 \times t_{MCY}$	–	–	ns

1. Time from the MLEN falling edge to the next MCK rising edge. If the MCK clock stops after the LSB, the MLEN rise timing is optional.
2. Time from MCK rising edge corresponding to the LSB to the MLEN rising edge.



FUNCTIONAL DESCRIPTION

27 MHz Master Clock

The 27 MHz master clock is generated either by connecting a crystal oscillator element between XTI (pin 6) and XTO (pin 5), as shown in figure 1, or by connecting an external 27 MHz clock to XTI, as shown in figure 2. Input 27MHz master clock on XTI when using an external clock. Crystal oscillator element must be fundamental.

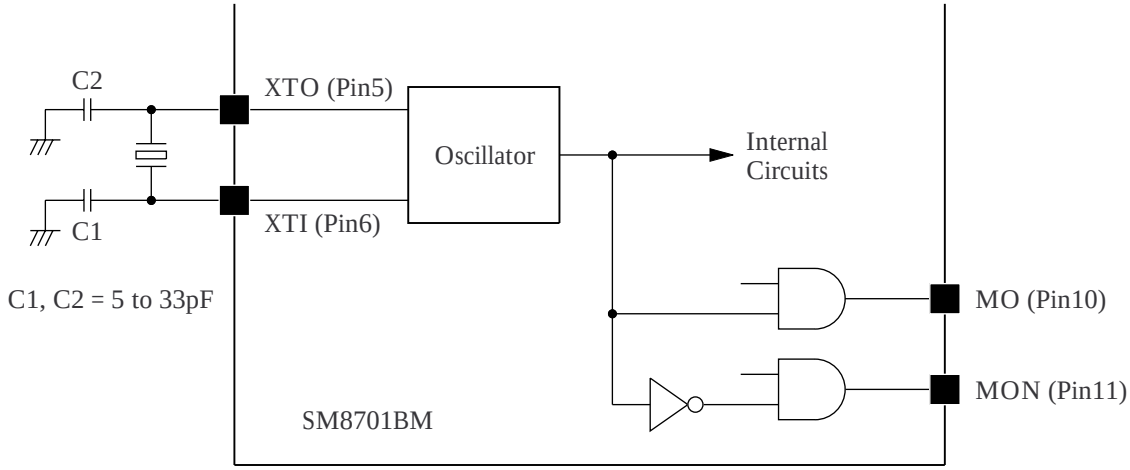


Figure 1. Crystal oscillator connection

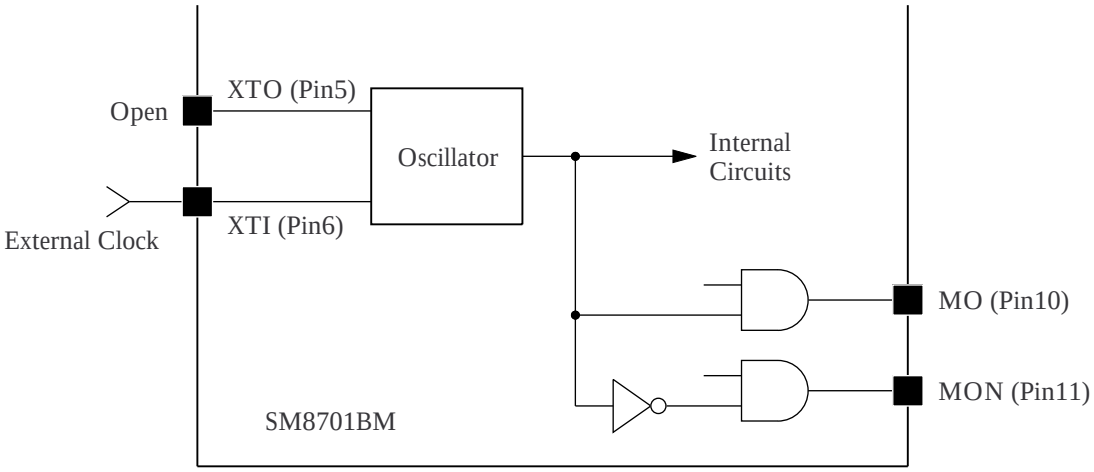


Figure 2. External clock input

Sampling Frequency and Output Clock Frequency

The SM8701BM generates several output clocks from the 27 MHz master clock, with frequencies of 256fs (SO2), 384fs (SO3) and 768fs (SO4), where fs is the sampling frequency selected by external control inputs. SO1 outputs 33.8688 MHz clock. The supported sampling frequencies and the output clock frequencies are shown in table 1.

Table 1. Sampling frequency and output clock frequency

Sampling rate	Sampling frequency fs	Output clock frequency (MHz)			
		SO1	SO2	SO3	SO4
Standard	32 kHz	33.8688	8.192	12.288	24.576
	44.1 kHz	33.8688	11.2896	16.9344	33.8688
	48 kHz	33.8688	12.288	18.432	36.864
Double	64 kHz	33.8688	16.384	24.576	24.576
	88.2 kHz	33.8688	22.5792	33.8688	33.8688
	96 kHz	33.8688	24.576	36.864	36.864

Reset

The SM8701BM supports an external reset using RSTN (pin 18). At reset, the mode register takes its default value, and the output clocks have default frequencies.

When RSTN goes HIGH, an internal reset continues for a period of 1024 cycles of the 27 MHz master clock. The timing is shown in figure 3.

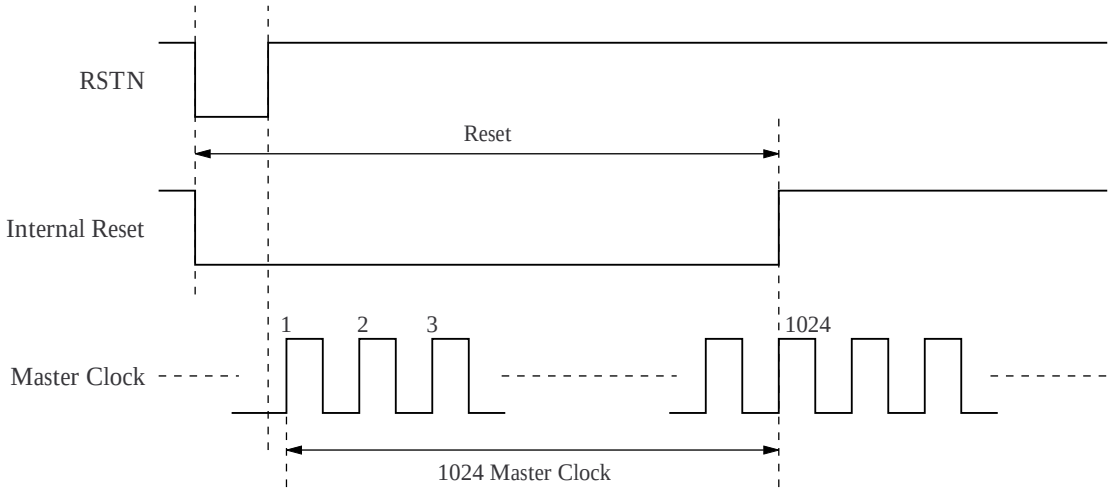


Figure 3. External reset timing

Operation Control

The SM8701BM functions are controlled by inputs MLEN/R2 (pin 1), MDT/R0 (pin 19) and MCK/R1 (pin 20). The operating mode is selected by input P/S (pin 2)—serial control when P/S is LOW, and parallel control when P/S is HIGH. Table 2 shows the relationship between functions and mode.

Table 2. Control functions

Function	Controllable	
	Serial	Parallel
Sampling frequency group: 48/44.1/32 kHz	Yes	Yes
Sampling rate: standard/double	Yes	Yes
Clock output: enable/disable	Yes	No

Serial control (P/S = LOW)

When P/S is LOW, the control interface is serial control mode. The serial control data is set by 16-bit MDT data in sync with the MCK clock and the MLEN enable signal clock at the serial control mode. The format is shown in figure 4.

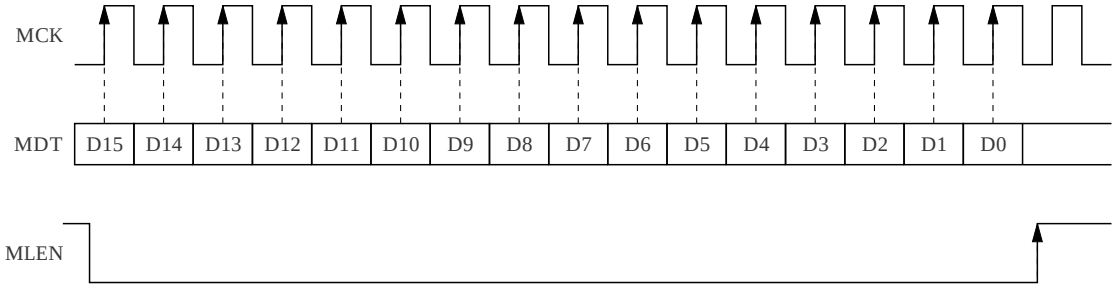
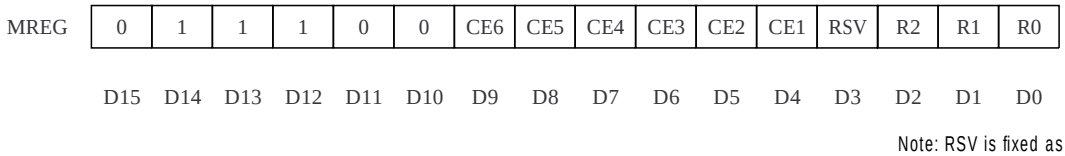


Figure 4. Serial control format

The 16-bit mode register (MREG) is shown in figure 5, and the name and function of each bit is described in tables 3 to 5. In serial control mode, mode register bits D15 to D10 must be set to 011100. D3 is fixed as LOW.



Note: RSV is fixed as LOW.

Figure 5. Mode register

Table 3. Mode register control bit functions

Bit	Name	Function
D9	CE6	MON output enable/disable
D8	CE5	MO output enable/disable
D7	CE4	SO4 output enable/disable
D6	CE3	SO3 output enable/disable
D5	CE2	SO2 output enable/disable
D4	CE1	SO1 output enable/disable
D3	RSV	Fixed as LOW
D2/D1/D0	R2/R1/R0	Sampling frequency select

Table 4. CE6 to CE1 clock output control setting

CE6 to CE1	Clock output
LOW	Disable (LOW-level output)
HIGH	Enable (default)

Table 5. Sampling frequency select (R2, R1, R0)

R2	R1	R0	Sampling rate	Sampling frequency group	Sampling frequency
LOW	LOW	LOW	Standard	48 kHz	48 kHz (default)
LOW	LOW	HIGH	Standard	44.1 kHz	44.1 kHz
LOW	HIGH	LOW	Standard	32 kHz	32 kHz
LOW	HIGH	HIGH	Prohibited (test mode)		
HIGH	LOW	LOW	Double	48 kHz	96 kHz
HIGH	LOW	HIGH	Double	44.1 kHz	88.2 kHz
HIGH	HIGH	LOW	Double	32 kHz	64 kHz
HIGH	HIGH	HIGH	Prohibited (test mode)		

When the sampling frequency is changed, a settling time of 40 ms (max) is required to make the output frequency stable. The SO2 to SO4 output response when the frequency is changed is shown in figure 6. SO1 fixed on 33.8688 MHz.

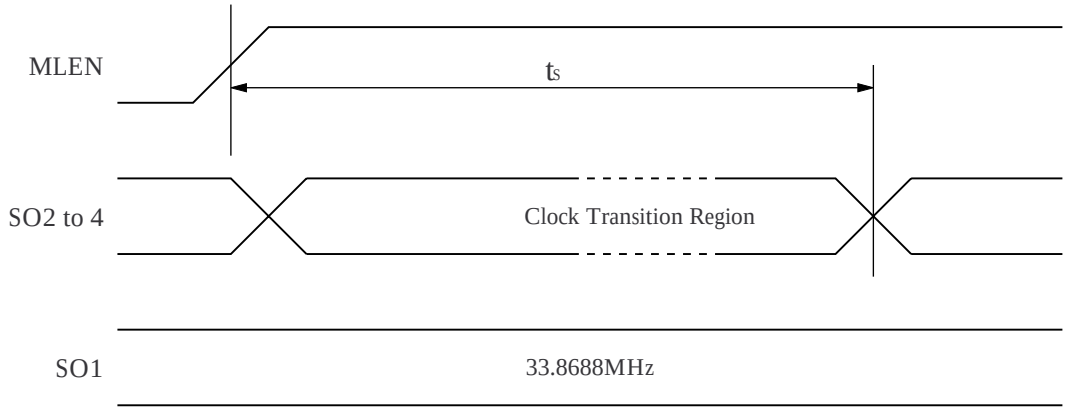


Figure 6. System clock transient timing

Parallel control (P/S = HIGH)

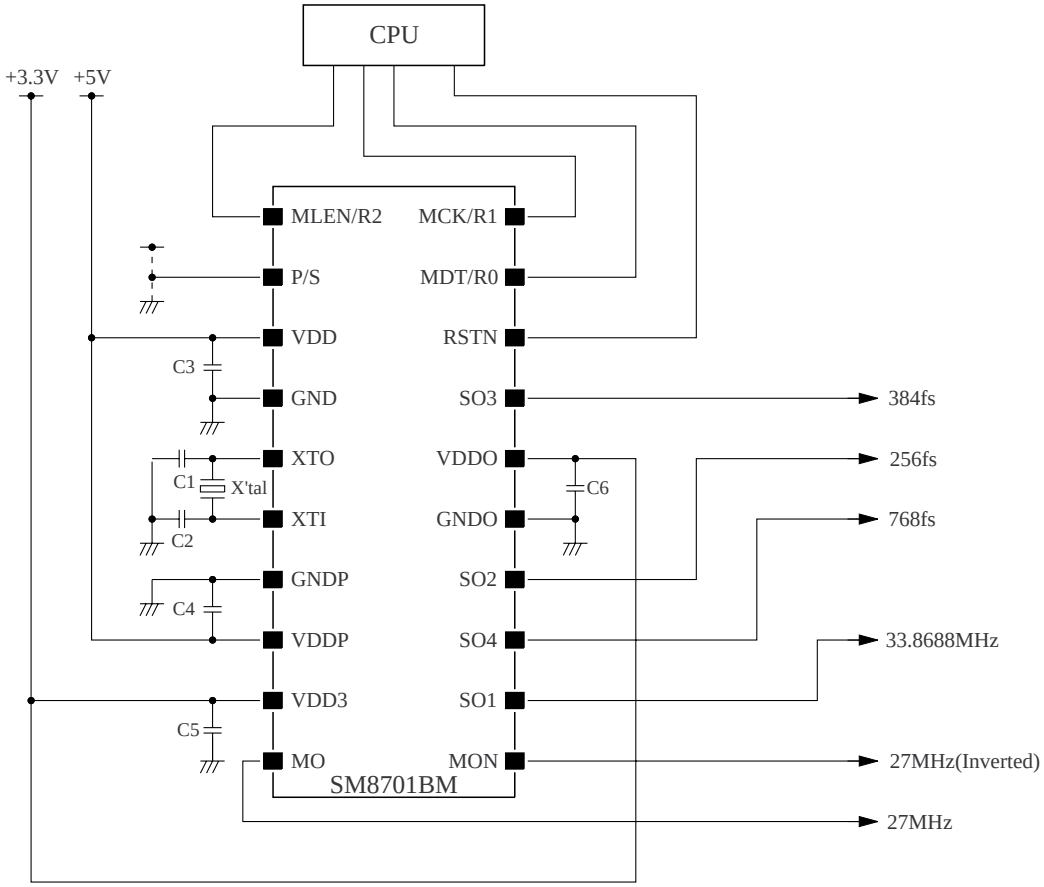
When P/S is HIGH, the control interface is parallel control mode. The parallel control pins R2 (pin 1), R1 (pin 20) and R0 (pin 19) and functions are shown in table 6.

Table 6. Sampling frequency select (R2, R1, R0)

R2	R1	R0	Sampling rate	Sampling frequency group	Sampling frequency
LOW	LOW	LOW	Standard	48 kHz	48 kHz (default)
LOW	LOW	HIGH	Standard	44.1 kHz	44.1 kHz
LOW	HIGH	LOW	Standard	32 kHz	32 kHz
LOW	HIGH	HIGH	Prohibited (test mode)		
HIGH	LOW	LOW	Double	48 kHz	96 kHz
HIGH	LOW	HIGH	Double	44.1 kHz	88.2 kHz
HIGH	HIGH	LOW	Double	32 kHz	64 kHz
HIGH	HIGH	HIGH	Prohibited (test mode)		

Note that in parallel control mode, clock output enable/disable controls are not available. Also note that the reset function does not affect the sampling frequency group or sampling rate select settings (it is determined by R2, R1, R0 condition).

TYPICAL APPLICATION



- Connect the decoupling capacitors (approximately 0.1µF and 1000pF) in parallel, as close to power supply pins as possible.
- In order to minimize noise, it is useful to make ground as solid pattern.
- Master clock stability affects the other outputs stability. In the usage of crystal oscillator, load capacitor and crystal oscillator should be placed as close to the SM8701BM as possible, and wired shortly. Select crystal oscillators and load capacitance carefully, depending on the condition, as those combination will have influence on the frequency accuracy(C1, C2).
- Supply pattern including decoupling capacitors needs careful attention to make the IC's performance better, since the SM8701BM outputs several high frequency clocks. Pattern capacitance from output pins should not to be large for prevention of the noise. Connecting output pins to buffers is useful if it is necessary.
- Power supply and ground pins.
  - VDD :5V Power supply for digital block (CPU I/F*, XT1, XT2).
  - GND : Ground for digital block (CPU I/F*, XT1, XT2, output block except SO3).
  - VDDP :5V Power supply for PLL block.
  - GNDP : Ground for PLL block.
  - VDDO :3.3V Power supply for SO3.
  - GNDO : Ground for SO3.
  - VDD3 :3.3V Power supply for output block (except SO3).

*: CPU I/F: MDT/R0, MCK/R1, MLEN/R2, RSTN, P/S

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