NIPPON PRECISION CIRCUITS INC.

SM8707 series

Clock Generator with Dual PLLs

OVERVIEW

The SM8707 series are dual-PLL clock generator ICs, using a 27MHz master clock, that generate independent audio clock, video clock, and signal processor clock outputs needed in DVD player/recorder applications. Each PLL loop filter and crystal oscillator circuit are built-in and require no external components, resulting in high-precision clocks. The lineup includes devices that support both 44.1/48kHz audio sampling frequencies (fs), switchable using a control pin. The sampling frequency can be switched during operation without generating any output spike noise.

FEATURES

- Supply voltage: 3.0 to 3.6V
- Low current consumption: 35mA typ.
  (V_{DD} = 3.3V, all outputs with no load)
- 27MHz master clock
  (internal PLL reference clock)
- PLL loop filter built-in
- Crystal oscillator circuit built-in
- Sampling frequency fs: 44.1/48kHz
- 16-pin VSOP package (Pb free)
- Generated clocks (Refer to "Output Frequency Listing" on page 18 for details.)

	SM8707D	SM8707E	SM8707F	SM8707G	SM8707H	SM8707K	SM8707L
Video system output	27.0000MHz	27.0000MHz	27.0000MHz	27.0000MHz	27.0000MHz	–	27.0000MHz
Audio system output	512fs 768fs[1] 384fs[1]	512fs	768fs	–	512fs	768fs	768fs
Signal processor system output	16.9344MHz 33.8688MHz	33.8688MHz	16.9344MHz 33.8688MHz	33.8688MHz	16.9344MHz 33.8688MHz 36.8640MHz	18.4320MHz 24.5760MHz 33.8688MHz 36.8640MHz	24.5760MHz 33.8688MHz

1. 384fs (fs = 44.1kHz)/768fs (fs = 48kHz)

- Low jitter output (1-sigma output load capacitance typical values)

	SM8707D	SM8707E	SM8707F	SM8707G	SM8707H	SM8707K	SM8707L
Video system output	20ps	20ps	20ps	20ps	20ps	–	20ps
Audio and Signal processor system output	70ps	55ps	40ps	40ps	70ps	60ps	60ps

APPLICATIONS

- DVD players/recorders
- DVD car navigation system

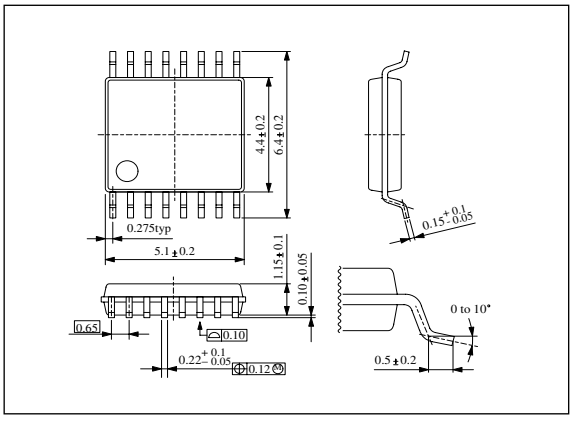
ORDERING INFORMATION

Device	Package
SM8707DV	16-pin VSOP
SM8707EV	
SM8707FV	
SM8707GV	
SM8707HV	
SM8707KV	
SM8707LV	

PACKAGE DIMENSIONS

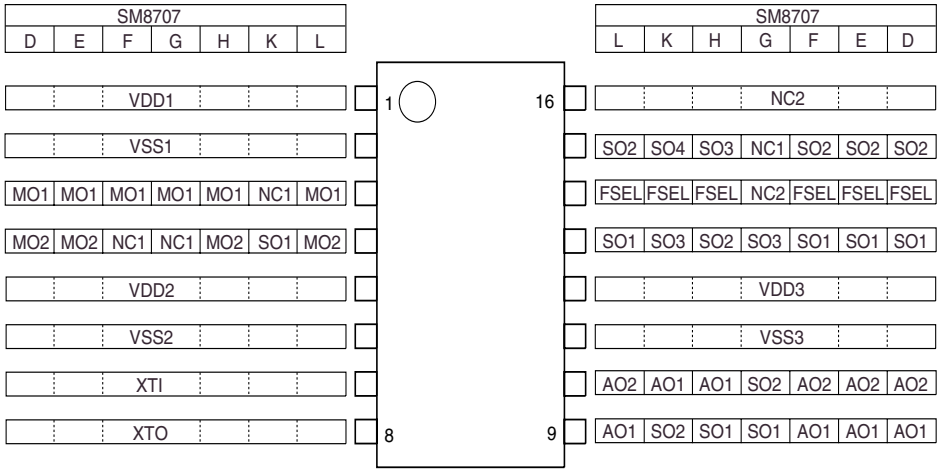
(Unit: mm)

Weight: 0.07g



PINOUT

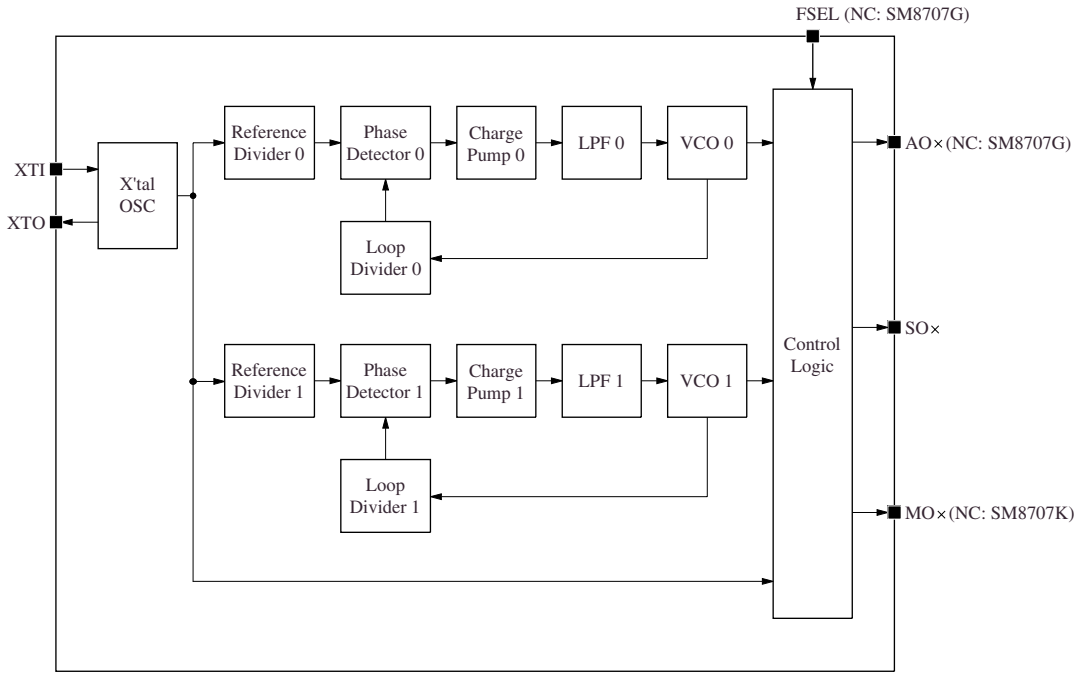
(Top view)



PIN DESCRIPTION

Name	I/O	Description
MO×	O	Video system output
AO×	O	Audio system output
SO×	O	Signal processor system output
FSEL	I	Sampling frequency select
XTI	I	Crystal oscillator connection or external clock input
XTO	O	Crystal oscillator connection
VDD1	–	Supply for digital block
VSS1	–	Ground for digital block
VDD2	–	Supply for analog block
VSS2	–	Ground for analog block
VDD3	–	Supply for digital block
VSS3	–	Ground for digital block
NC1	O	No connection output (leave pin open circuit)
NC2	I	No connection (leave pin open circuit or connect to VDD)

BLOCK DIAGRAM



Note: Unless otherwise noted, VDD applies to VDD1, VDD2, and VDD3. Similarly, VSS applies to VSS1, VSS2, and VSS3.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD1} , V_{DD2} , V_{DD3}		– 0.3 to + 6.5	V
Supply voltage deviation	$V_{DD1} - V_{DD2}$, $V_{DD1} - V_{DD3}$, $V_{DD2} - V_{DD3}$		± 0.1	V
Input voltage range	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D		165	mW
Storage temperature range	T_{stg}		– 55 to + 125	°C

Recommended Operating Conditions

$V_{SS} = V_{SS1} = V_{SS2} = V_{SS3} = 0V$ unless otherwise noted.

Note 1: The supply voltage is defined relative to $V_{SS} = 0V$.

Note 2: The supply voltages applied on VDD1, VDD2, and VDD3 should be derived from a common supply source.

Note 3: If the supply voltages on VDD1, VDD2, and VDD3 are from different sources, they should be applied simultaneously. The SM8707 may be damaged if the supply voltage timing is different.

SM8707D

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges	V_{DD1} , V_{DD2} , V_{DD3}	(Note 1, 2, 3)	+ 3.0	–	+ 3.6	V
Output load capacitance 1	C_{L1}	MO1, MO2, SO1, SO2 outputs	–	–	25	pF
Output load capacitance 2	C_{L2}	AO1, AO2 outputs	–	–	15	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 40	–	+ 85	°C

SM8707E

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges	V_{DD1} , V_{DD2} , V_{DD3}	(Note 1, 2, 3)	+ 3.0	–	+ 3.6	V
Output load capacitance 1	C_{L1}	MO1 output	–	–	40	pF
Output load capacitance 2	C_{L2}	MO2 output	–	–	25	pF
Output load capacitance 3	C_{L3}	SO1, SO2, AO1, AO2 outputs	–	–	15	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 10	–	+ 75	°C

SM8707F

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges	V_{DD1} , V_{DD2} , V_{DD3}	(Note 1, 2, 3)	+ 3.0	–	+ 3.6	V
Output load capacitance 1	C_{L1}	MO1, SO1, SO2 outputs	–	–	25	pF
Output load capacitance 2	C_{L2}	AO1, AO2 outputs	–	–	15	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 40	–	+ 85	°C

SM8707G

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges	V_{DD1} , V_{DD2} , V_{DD3}	(Note 1, 2, 3)	+ 3.0	–	+ 3.6	V
Output load capacitance 1	C_{L1}	MO1 output	–	–	40	pF
Output load capacitance 2	C_{L2}	SO3 output	–	–	25	pF
Output load capacitance 3	C_{L3}	SO1, SO2 outputs	–	–	15	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 10	–	+ 75	°C

SM8707H

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges	V_{DD1} , V_{DD2} , V_{DD3}	(Note 1, 2, 3)	+ 3.0	–	+ 3.6	V
Output load capacitance 1	C_{L1}	MO1, MO2, SO2, SO3 outputs	–	–	25	pF
Output load capacitance 2	C_{L2}	AO1, SO1 outputs	–	–	15	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 40	–	+ 85	°C

SM8707K

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges	V_{DD1} , V_{DD2} , V_{DD3}	(Note 1, 2, 3)	+ 3.0	–	+ 3.6	V
Output load capacitance	C_L	Outputs	–	–	25	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 40	–	+ 85	°C

SM8707L

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage ranges	V_{DD1} , V_{DD2} , V_{DD3}	(Note 1, 2, 3)	+ 3.0	–	+ 3.6	V
Output load capacitance	C_L	Outputs excluding XTO	–	–	15	pF
Master clock frequency	f_{XTAL}	When using crystal oscillator	–	27.0000	–	MHz
Operating temperature range	T_{opr}		– 40	–	+ 85	°C

DC Electrical Characteristics

- SM8707D/F/H/K/L
  f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 40 to + 85 °C unless otherwise noted.
- SM8707E/G
  f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 10 to + 75 °C unless otherwise noted.

Parameter	Symbol	Pins	Condition		Rating			Unit
					min	typ	max	
Current consumption	I_{DD}	VDD	V_{DD} = 3.3V, Ta = 25°C, fs = 48kHz, Crystal oscillator connected, no load on all outputs	Excluding SM8707G	–	35	45	mA
				SM8707G	–	20	27	
Input voltage	V_{IH}	FSEL, XTI	V_{DD} = 3.3V		0.8 V_{DD}	–	–	V
	V_{IL}				–	–	0.2 V_{DD}	
Input current	I_{IH1}	FSEL[1]	V_{IN} = V_{DD}		–	–	1	µA
	I_{IL1}		V_{IN} = 0V		– 100	–	–	
	I_{IH2}	XTI	V_{IN} = V_{DD}		–	–	40	
	I_{IL2}		V_{IN} = 0V		– 40	–	–	
Output voltage	V_{OH}	All outputs excluding XTO	I_{OH} = – 2mA		V_{DD} – 0.4	–	–	V
	V_{OL}		I_{OL} = 2mA		–	–	0.4	

1. FSEL pin has Schmitt-trigger input and built-in pull-up resistor (SM8707G: NC pin).

AC Electrical Characteristics

SM8707D

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 40 to + 85 °C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI	Applies to external clock input use only	–	27.0000	–	MHz
Output clock rise time[2]	t_r	MO1, MO2, SO1, SO2	C_L = 25 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
		AO1, AO2	C_L = 15pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
Output clock fall time[2]	t_f	MO1, MO2, SO1, SO2	C_L = 25pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
		AO1, AO2	C_L = 15pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
Output clock jitter[3]	t_{jitter} (1-sigma)	MO1, MO2	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	20	–	ps
		SO1, SO2		–	70	–	
		AO1, AO2	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	70	–	
Output clock duty cycle[2]	Dt	MO1, MO2, SO1, SO2	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	%
		AO1, AO2	Ta = 25°C, C_L =15 pF, V_O = 0.5V_{DD}	45	50	55	
Settling time[2]	t_S	All outputs excluding XTO		–	–	1	µs
Power-up time[2, 4]	t_P	All outputs excluding XTO		–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

SM8707E

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 10 to + 75 °C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI	Applies to external clock input use only	–	27.0000	–	MHz
Output clock rise time[2]	t_r	MO1	C_L = 40 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
		MO2	C_L = 25 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
		SO1, SO2, AO1, AO2	C_L = 15pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
Output clock fall time[2]	t_f	MO1	C_L = 40pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
		MO2	C_L = 25pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
		SO1, SO2, AO1, AO2	C_L = 15pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
Output clock jitter[3]	t_{jitter} (1-sigma)	MO1	Ta = 25°C, C_L = 40pF, V_O = 0.5V_{DD}	–	20	–	ps
		MO2	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	20	–	
		SO1, SO2, AO1, AO2	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	55	–	
Output clock duty cycle[2]	Dt	MO1	Ta = 25°C, C_L = 40pF, V_O = 0.5V_{DD}	45	50	55	%
		MO2	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	
		SO1, SO2, AO1, AO2	Ta = 25°C, C_L =15 pF, V_O = 0.5V_{DD}	45	50	55	
Settling time[2]	t_S	AO1, AO2		–	–	1	µs
Power-up time[2, 4]	t_P	All outputs excluding XTO		–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

SM8707F

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 40 to + 85 °C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI	Applies to external clock input use only	–	27.0000	–	MHz
Output clock rise time[2]	t_r	MO1, SO1, SO2	C_L = 25 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
		AO1, AO2	C_L = 15pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
Output clock fall time[2]	t_f	MO1, SO1, SO2	C_L = 25pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
		AO1, AO2	C_L = 15pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
Output clock jitter[3]	t_{jitter} (1-sigma)	MO1	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	20	–	ps
		SO1, SO2		–	40	–	
		AO1, AO2	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	40	–	
Output clock duty cycle[2]	Dt	MO1, SO1, SO2	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	%
		AO1, AO2	Ta = 25°C, C_L =15 pF, V_O = 0.5V_{DD}	45	50	55	
Settling time[2]	t_S	All outputs excluding XTO		–	–	1	µs
Power-up time[2, 4]	t_P	All outputs excluding XTO		–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

SM8707G

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 10 to + 75 °C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI	Applies to external clock input use only	–	27.0000	–	MHz
Output clock rise time[2]	t_r	MO1	C_L = 40 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
		SO3	C_L = 25 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
		SO1, SO2	C_L = 15pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
Output clock fall time[2]	t_f	MO1	C_L = 40pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
		SO3	C_L = 25pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
		SO1, SO2	C_L = 15pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
Output clock jitter[3]	t_{jitter} (1-sigma)	MO1	Ta = 25°C, C_L = 40pF, V_O = 0.5V_{DD}	–	20	–	ps
		SO3	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	40	–	
		SO1, SO2	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	40	–	
Output clock duty cycle[2]	Dt	MO1	Ta = 25°C, C_L = 40pF, V_O = 0.5V_{DD}	45	50	55	%
		SO3	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	
		SO1, SO2	Ta = 25°C, C_L =15 pF, V_O = 0.5V_{DD}	45	50	55	
Power-up time[2, 4]	t_P	All outputs excluding XTO		–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

SM8707H

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 40 to + 85 °C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI	Applies to external clock input use only	–	27.0000	–	MHz
Output clock rise time[2]	t_r	MO1, MO2, SO2, SO3	C_L = 25 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
		SO1, AO1	C_L = 15pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	
Output clock fall time[2]	t_f	MO1, MO2, SO2, SO3	C_L = 25pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
		SO1, AO1	C_L = 15pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	
Output clock jitter[3]	t_{jitter} (1-sigma)	MO1, MO2	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	20	–	ps
		SO2, SO3		–	70	–	
		SO1, AO1	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	70	–	
Output clock duty cycle[2]	Dt	MO1, MO2, SO2, SO3	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	%
		SO1, AO1	Ta = 25°C, C_L =15 pF, V_O = 0.5V_{DD}	45	50	55	
Settling time[2]	t_S	All outputs excluding XTO		–	–	1	µs
Power-up time[2, 4]	t_P	All outputs excluding XTO		–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

SM8707K

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 40 to + 85 °C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI	Applies to external clock input use only	–	27.0000	–	MHz
Frequency deviation[1]	D_f	SO1, SO2, SO3, SO4, AO1	Applies to external clock input use only, When frequency deviation of master clock is 0ppm	–15	–	+15	ppm
Output clock rise time[2]	t_r	SO1, SO2, SO3, SO4, AO1	C_L = 25 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
Output clock fall time[2]	t_f	SO1, SO2, SO3, SO4, AO1	C_L = 25pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
Output clock jitter[3]	t_{jitter} (1-sigma)	SO1, SO2, SO3, SO4, AO1	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	60	–	ps
Output clock duty cycle[2]	Dt	SO1, SO2, SO3, SO4, AO1	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	%
Settling time[2]	t_S	All outputs excluding XTO		–	–	1	µs
Power-up time[2, 4]	t_P	All outputs excluding XTO		–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

SM8707L

f_{XTAL} = 27.0000MHz, V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = – 40 to + 85 °C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
External input clock frequency[1]	f_{XTI}	XTI	Applies to external clock input use only	–	27.0000	–	MHz
Output clock rise time[2]	t_r	MO1, MO2, SO1, SO2, AO1, AO2	C_L = 15 pF, transition between V_{OL} = 0.2V_{DD} and V_{OH} = 0.8V_{DD}	–	2.0	–	ns
Output clock fall time[2]	t_f	MO1, MO2, SO1, SO2, AO1, AO2	C_L = 15pF, transition between V_{OH} = 0.8V_{DD} and V_{OL} = 0.2V_{DD}	–	2.0	–	ns
Output clock jitter[3]	t_{jitter} (1-sigma)	MO1, MO2	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	20	–	ps
		SO1, SO2, AO1, AO2		–	60	–	ps
Output clock duty cycle[2]	Dt	MO1, MO2, SO1, SO2, AO1, AO2	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	45	50	55	%
Settling time[2]	t_S	All outputs excluding XTO		–	–	1	µs
Power-up time[2, 4]	t_P	All outputs excluding XTO		–	1	5	ms

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

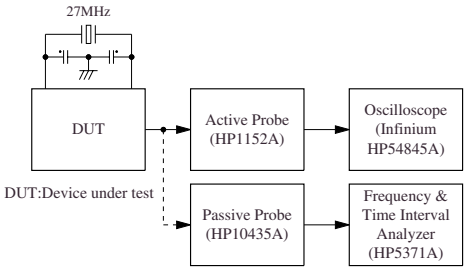


Figure 1. Measurement circuit 1

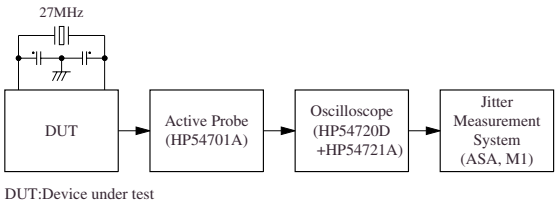


Figure 2. Measurement circuit 2

FUNCTIONAL DESCRIPTION

27MHz Master Clock

The SM8707 series 27MHz master clock circuit is configured, as shown in Figure 3 and 4, with the crystal oscillator element connected between XTI (pin 7) and XTO (pin 8).

Alternatively, the 27MHz master clock can be supplied from an external master clock input on XTI, as shown in Figure 5 and 6.

If an external input clock on XTI is used, it is recommended that the frequency be 27.0000MHz, with 50% duty, and 3.3V voltage amplitude level.

Furthermore, when using an external clock input, the input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.

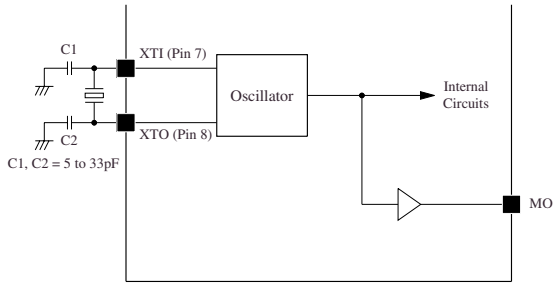


Figure 3. Crystal oscillator connection (excluding SM8707K)

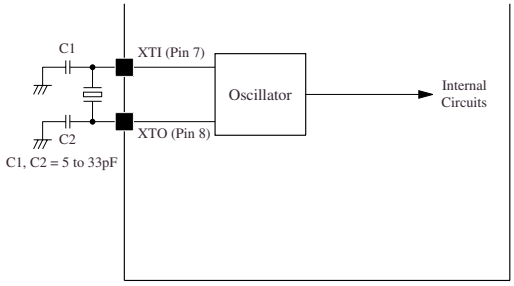


Figure 4. Crystal oscillator connection (SM8707K)

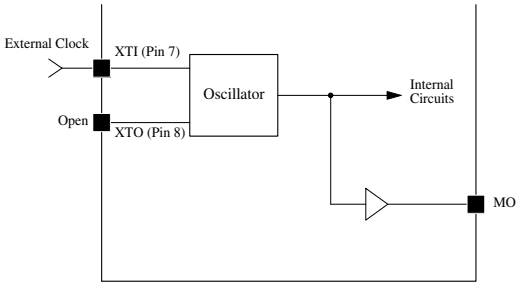


Figure 5. External clock input (excluding SM8707K)

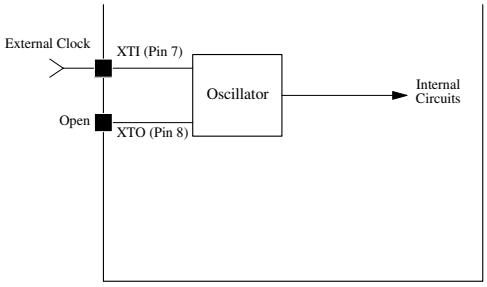


Figure 6. External clock input (SM8707K)

Sampling Frequency and Output Clock Frequency

SM8707D

The SM8707D sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is HIGH, and 48kHz when FSEL is LOW. The audio output (AO1) is a 384fs frequency clock when FSEL is HIGH (fs = 44.1kHz), and 768fs frequency clock when FSEL is LOW (fs = 48kHz) where fs is determined by the setting on FSEL. The audio output (AO2) is a 512fs frequency clock. In addition, the signal processor output (SO1 and SO2) is a 16.9344MHz, 33.8688MHz frequency clock derived from the master clock. And the video output (MO1 and MO2) is a 27MHz frequency clock, identical to the master clock.

The SM8707D possible output clock frequencies are shown in Table 1.

Table 1. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

FSEL (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]					
		AO1 (Pin 9)	AO2 (Pin 10)	SO1 (Pin 13)	SO2 (Pin 15)	MO1 (Pin 3)	MO2 (Pin 4)
HIGH	44.1	16.9344 (384fs)	22.5792 (512fs)	16.9344	33.8688	27.0000	27.0000
LOW	48	36.8640 (768fs)	24.5760 (512fs)	16.9344	33.8688	27.0000	27.0000

SM8707E

The SM8707E sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is LOW, and 48kHz when FSEL is HIGH. The audio output (AO1 and AO2) is a 512fs frequency clock, where fs is determined by the setting on FSEL. In addition, the signal processor output (SO1 and SO2) is a 33.8688MHz frequency clock derived from the master clock. And the video output (MO1 and MO2) is a 27MHz frequency clock, identical to the master clock.

The SM8707E possible output clock frequencies are shown in Table 2.

Table 2. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

FSEL (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]					
		AO1 (Pin 9)	AO2 (Pin 10)	SO1 (Pin 13)	SO2 (Pin 15)	MO1 (Pin 3)	MO2 (Pin 4)
HIGH	48	24.5760 (512fs)	24.5760 (512fs)	33.8688	33.8688	27.0000	27.0000
LOW	44.1	22.5792 (512fs)	22.5792 (512fs)	33.8688	33.8688	27.0000	27.0000

SM8707F

The SM8707F sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is HIGH, and 48kHz when FSEL is LOW. The audio outputs (AO1 and AO2) are equivalent to 768fs, where fs is determined by the setting on FSEL. In addition, the signal processor outputs (SO1 and SO2) are 16.9344MHz and 33.8688MHz clocks, respectively, derived from the master clock. The video output (MO1) is a 27MHz clock, identical to the master clock.

The SM8707F supported clock frequencies are shown in Table 3.

Table 3. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

FSEL (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]				
		AO1 (Pin 9)	AO2 (Pin 10)	SO1 (Pin 13)	SO2 (Pin 15)	MO1 (Pin 3)
HIGH	44.1	33.8688 (768fs)	33.8688 (768fs)	16.9344	33.8688	27.0000
LOW	48	36.8640 (768fs)	36.8640 (768fs)	16.9344	33.8688	27.0000

SM8707G

The SM8707G signal processor outputs (SO1, SO2 and SO3) are all 33.8688MHz clocks, derived from the master clock. The video output (MO1) is a 27MHz clock, identical to the master clock.

The SM8707G supported clock frequencies are shown in Table 4.

Table 4. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

Output clock frequency [MHz]			
SO1 (Pin 9)	SO2 (Pin 10)	SO3 (Pin 13)	MO1 (Pin 3)
33.8688	33.8688	33.8688	27.0000

SM8707H

The SM8707H sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is HIGH, and 48kHz when FSEL is LOW. The audio output (AO1) is equivalent to 512fs, where fs is determined by the setting on FSEL. In addition, the signal processor outputs (SO1, SO2 and SO3) are 36.8640MHz, 16.9344MHz and 33.8688MHz clocks, respectively, derived from the master clock. The video outputs (MO1 and MO2) are 27MHz clocks, identical to the master clock.

The SM8707H supported clock frequencies are shown in Table 5.

Table 5. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

FSEL (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]					
		AO1 (Pin 10)	SO1 (Pin 9)	SO2 (Pin 13)	SO3 (Pin 15)	MO1 (Pin 3)	MO2 (Pin 4)
HIGH	44.1	22.5792 (512fs)	36.8640	16.9344	33.8688	27.0000	27.0000
LOW	48	24.5760 (512fs)	36.8640	16.9344	33.8688	27.0000	27.0000

SM8707K

The SM8707K sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is HIGH, and 48kHz when FSEL is LOW. The audio output (AO1) is equivalent to 768fs, where fs is determined by the setting on FSEL. In addition, the signal processor output (SO1, SO2, SO3 and SO4) is 24.5760MHz, 18.4320MHz, 36.8640MHz and 33.8688MHz clocks, respectively, derived from the master clock. Also, the audio output AO1 36.8688MHz clock is synchronized with the signal processor output SO4 clock, and audio output AO1 36.8640MHz clock is synchronized with the signal processor output SO3 clock.

The SM8707K supported clock frequencies are shown in Table 6.

Table 6. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

FSEL (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]				
		AO1 (Pin 10)	SO1 (Pin 4)	SO2 (Pin 9)	SO3 (Pin 13)	SO4 (Pin 15)
HIGH	44.1	33.8688 (768fs)	24.5760	18.4320	36.8640	33.8688
LOW	48	36.8640 (768fs)	24.5760	18.4320	36.8640	33.8688

SM8707L

The SM8707L sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is LOW, and 48kHz when FSEL is HIGH. The audio output (AO1 and AO2) is a 768fs frequency clock, where fs is determined by the setting on FSEL. In addition, the signal processor output (SO1 and SO2) is 24.5760MHz and 33.8688MHz frequency clock derived from the master clock. And the video output (MO1 and MO2) is a 27MHz frequency clock, identical to the master clock.

The SM8707L supported clock frequencies are shown in Table 7.

Table 7. Sampling frequency and output clock frequency (27.0000MHz master clock frequency)

FSEL (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]					
		AO1 (Pin 9)	AO2 (Pin 10)	SO1 (Pin 13)	SO2 (Pin 15)	MO1 (Pin 3)	MO2 (Pin 4)
HIGH	44.1	33.8688 (768fs)	33.8688 (768fs)	24.5760	33.8688	27.0000	27.0000
LOW	48	36.8640 (768fs)	36.8640 (768fs)	24.5760	33.8688	27.0000	27.0000

Spike Noise Prevention Function

All device versions, excluding the SM8707G which has no FSEL input, have a spike noise prevention circuit that prevents any spike noise generation in the audio output clocks when the sampling frequency is switched using FSEL.

The state of the AO× output before and after FSEL is switched is shown in Figure 7.

When FSEL is switched, either from LOW to HIGH or HIGH to LOW, the spike noise prevention circuit stops the AO× clock output by a maximum of 1µs, and then the output clock changes to reflect the current FSEL setting.

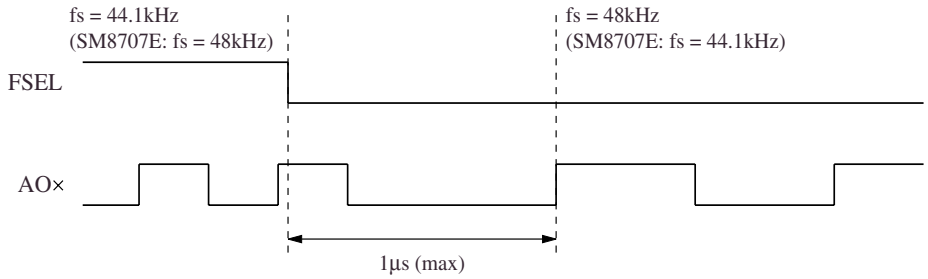


Figure 7. Spike noise prevention circuit timing at sampling frequency switching

Sampling Frequency Switching Settling Time

The clock output response when the sampling frequency is switched using FSEL is shown in Figure 8. Note that all device versions, excluding the SM8707G which has no FSEL input, have a spike noise prevention circuit which stops the output AO× clocks for a fixed interval, which means the settling time is a maximum 1µs when the sampling frequency is switched.

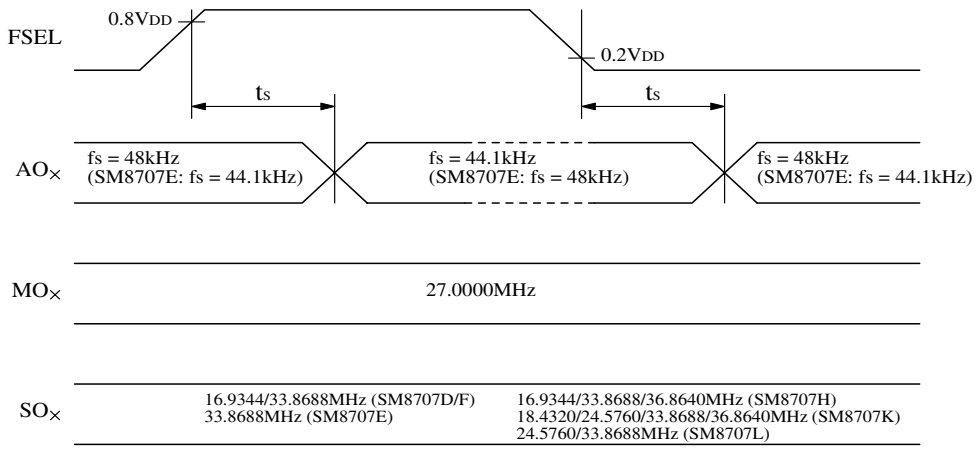


Figure 8. Output signal switching timing

SM8707 series OUTPUT FREQUENCY LISTING

Version	FSEL polarity (Pin 14)	Sampling frequency fs [kHz]	Output clock frequency [MHz]					
			Pin 3	Pin 4	Pin 9	Pin 10	Pin 13	Pin 15
SM8707D	H	44.1	27.0000	27.0000	16.9344 (384fs)	22.5792 (512fs)	16.9344	33.8688
	L	48.0	27.0000	27.0000	36.8640 (768fs)	24.5760 (512fs)	16.9344	33.8688
	Output load capacitance [pF]		25	25	15	15	25	25
	Pin name		MO1	MO2	AO1	AO2	SO1	SO2
SM8707E	H	48.0	27.0000	27.0000	24.5760 (512fs)	24.5760 (512fs)	33.8688	33.8688
	L	44.1	27.0000	27.0000	22.5792 (512fs)	22.5792 (512fs)	33.8688	33.8688
	Output load capacitance [pF]		40	25	15	15	15	15
	Pin name		MO1	MO2	AO1	AO2	SO1	SO2
SM8707F	H	44.1	27.0000	–	33.8688 (768fs)	33.8688 (768fs)	16.9344	33.8688
	L	48.0	27.0000		36.8640 (768fs)	36.8640 (768fs)	16.9344	33.8688
	Output load capacitance [pF]		25	–	15	15	25	25
	Pin name		MO1	NC1	AO1	AO2	SO1	SO2
SM8707G	–	–	27.0000	–	33.8688	33.8688	33.8688	–
	Output load capacitance [pF]		40	–	15	15	25	–
	Pin name		MO1	NC1	SO1	SO2	SO3	NC1
SM8707H	H	44.1	27.0000	27.0000	36.8640	22.5792 (512fs)	16.9344	33.8688
	L	48.0	27.0000	27.0000	36.8640	24.5760 (512fs)	16.9344	33.8688
	Output load capacitance [pF]		25	25	15	15	25	25
	Pin name		MO1	MO2	SO1	AO1	SO2	SO3
SM8707K	H	44.1	–	24.5760	18.4320	33.8688 (768fs)	36.8640	33.8688
	L	48.0		24.5760	18.4320	36.8640 (768fs)	36.8640	33.8688
	Output load capacitance [pF]		–	25	25	25	25	25
	Pin name		NC1	SO1	SO2	AO1	SO3	SO4
SM8707L	H	44.1	27.0000	27.0000	33.8688 (768fs)	33.8688 (768fs)	24.5760	33.8688
	L	48.0	27.0000	27.0000	36.8640 (768fs)	36.8640 (768fs)	24.5760	33.8688
	Output load capacitance [pF]		15	15	15	15	15	15
	Pin name		MO1	MO2	AO1	AO2	SO1	SO2

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