NIPPON PRECISION CIRCUITS INC.

SM8761 series

Spread Spectrum Clock Generator

OVERVIEW

The SM8761 series are compact clock generator ICs that have a spread spectrum (SS) function to reduce undesirable EMI radiation. They have a built-in crystal oscillator circuit, PLL, and loop filter. They accept an input clock signal, generated using an external crystal or direct external clock input, and output an SS-modulated clock signal. In addition, versions are available for center spread and down spread modulation mode, and all have a mode control pin to select the SS modulation function.

FEATURES

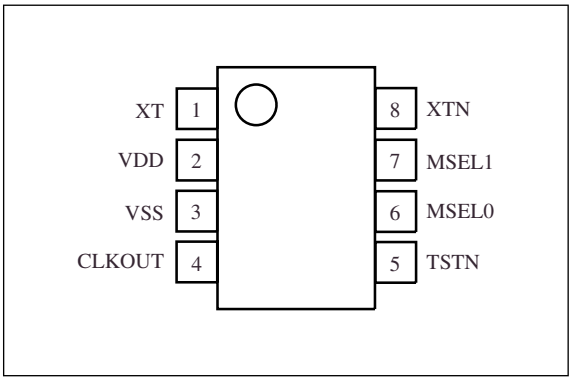
- Spread spectrum clock output to reduce EMI
- Correspond to wide range of output frequency
- Low jitter
- Operating supply voltage: 3.3 ± 0.3V
- Multiplication: 1-time multiplication
- Package: 8-pin SOP

		SM8761AA	SM8761AB
Spectrum modulation mode		Down spread	Center spread
Spectrum modulation rate*1		– 1.0% to – 3.8%	± 0.75% to ± 2.25%
Input frequency	Crystal element connection	20MHz to 40MHz	12MHz to 32MHz
	External input clock	20MHz to 108MHz	12MHz to 32MHz
Output frequency		20MHz to 108MHz	12MHz to 32MHz
Multiplication		1-time multiplication	1-time multiplication
Jitter (Cycle-to-Cycle)		200ps (typ) @33MHz	200ps (typ) @16MHz
		120ps (typ) @75MHz	

*1. The modulation rate that can be selected varies with the input frequency.

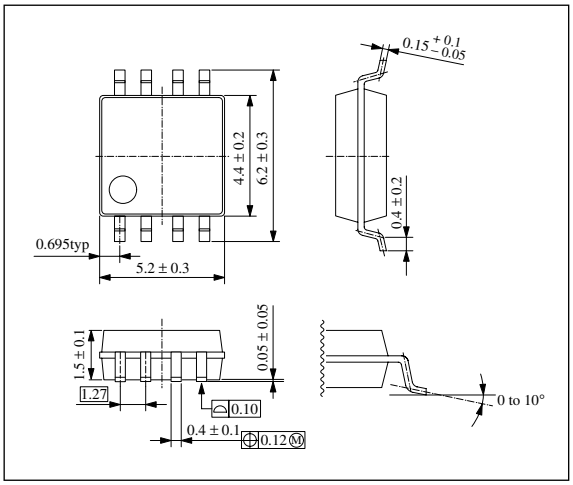
PINOUT

(Top view)



PACKAGE DIMENSIONS

(Unit: mm)



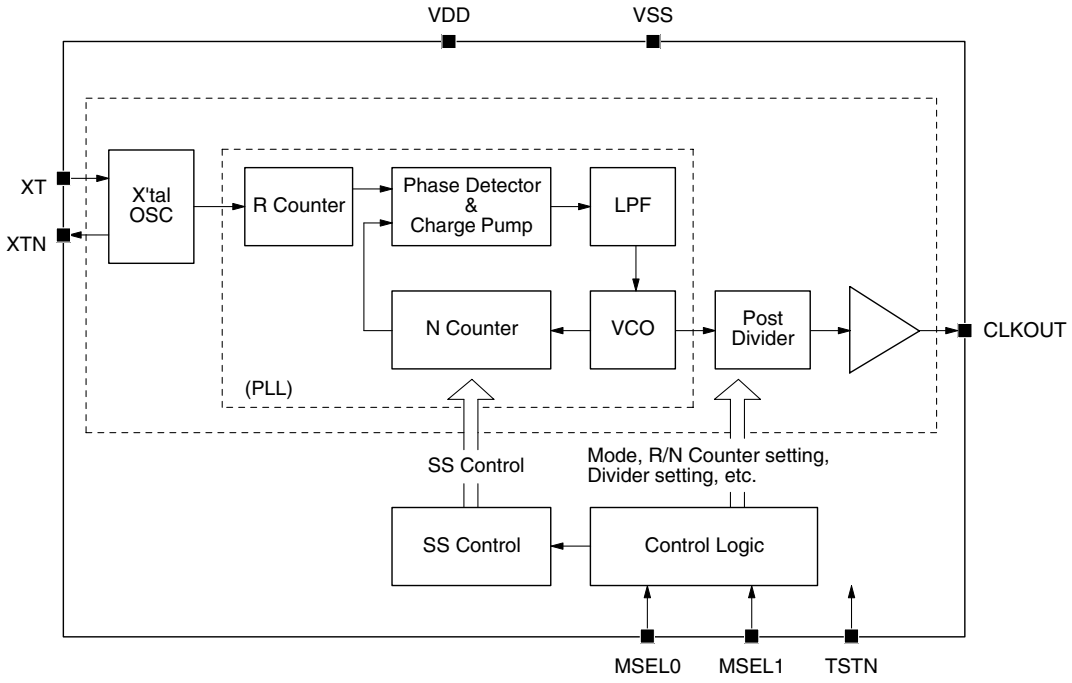
APPLICATIONS

- Printer (laser/inkjet)
- Photocopiers, scanners
- LCD/PDP displays
- Projectors
- Miscellaneous electronic equipment

ORDERING INFORMATION

Device	Package
SM8761AAS	8-pin SOP
SM8761ABS	

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O*1	Function
1	XT	I	Crystal oscillator element connection or external clock input
2	VDD	PWR	Supply voltage
3	VSS	GND	Ground
4	CLKOUT	O	SS clock output
5	TSTN	Ip	Test (Tie HIGH or leave open circuit)
6	MSEL0	I	SS modulation rate setting
7	MSEL1	I	SS modulation rate setting
8	XTN	O	Crystal oscillator element connection

*1. Built-in pull-up resistor

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to +6.5	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	300	mW
Storage temperature range	T_{STG}	–55 to +125	°C

Recommended Operating Conditions

SM8761AA

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage range	V_{DD}		+3.0	–	+3.6	V
Output load capacitance	C_L	CLKOUT output pin	–	–	15	pF
Master clock frequency	f_{IN}	Crystal oscillator element connection	20	–	40	MHz
		External clock input	20	–	108	
Operating temperature range	T_{OPR}		–20	–	+80	°C

SM8761AB

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage range	V_{DD}		+3.0	–	+3.6	V
Output load capacitance	C_L	CLKOUT output pin	–	–	15	pF
Master clock frequency	f_{IN}	Crystal oscillator element connection	12	–	32	MHz
		External clock input	12	–	32	
Operating temperature range	T_{OPR}		–20	–	+80	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

SM8761AA

V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V, Ta = –20 to +80°C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
Current consumption	I_{DD}	VDD	V_{DD} = 3.3V, Ta = 25°C, external input clock, fin = 33MHz, all outputs unloaded	–	11	16	mA
			V_{DD} = 3.3V, Ta = 25°C, external input clock, fin = 75MHz, all outputs unloaded	–	16	24	
Input voltage	V_{IH1}	MSEL0, MSEL1	V_{DD} = 3.3V	0.85V_{DD}	–	–	V
	V_{IM1}			0.45V_{DD}	0.50V_{DD}	0.55V_{DD}	
	V_{IL1}			–	–	0.15V_{DD}	
	V_{IH2}	TSTN	V_{DD} = 3.3V	0.85V_{DD}	–	–	
	V_{IL2}			–	–	0.15V_{DD}	
	V_{IH3}	XT	V_{DD} = 3.3V	0.80V_{DD}	–	–	
	V_{IL3}			–	–	0.20V_{DD}	
Input current	I_{IH1}	MSEL0, MSEL1	V_{IN} = V_{DD}	–	–	1	µA
	I_{IL1}		V_{IN} = 0V	–1	–	–	
	I_{IH2}	TSTN	V_{IN} = V_{DD}, built-in pull-up resistor	–	–	1	
	I_{IL2}		V_{IN} = 0V, built-in pull-up resistor	–100	–	–	
	I_{IH3}	XT	V_{IN} = V_{DD}	–	–	40	
	I_{IL3}		V_{IN} = 0V	–40	–	–	
Output voltage	V_{OH}	CLKOUT	I_{OH} = –2mA	V_{DD} – 0.4	–	–	V
	V_{OL}		I_{OL} = 2mA	–	–	0.4	

SM8761AB

V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V, Ta = −20 to +80°C unless otherwise noted.

Parameter	Symbol	Pins	Condition	Rating			Unit
				min	typ	max	
Current consumption	I_{DD}	VDD	V_{DD} = 3.3V, Ta = 25°C, external input clock, fin = 12MHz, all outputs unloaded	–	5	8	mA
			V_{DD} = 3.3V, Ta = 25°C, external input clock, fin = 24MHz, all outputs unloaded	–	6	10	
Input voltage	V_{IH1}	MSEL0, MSEL1	V_{DD} = 3.3V	0.85V_{DD}	–	–	V
	V_{IM1}			0.45V_{DD}	0.50V_{DD}	0.55V_{DD}	
	V_{IL1}			–	–	0.15V_{DD}	
	V_{IH2}	TSTN	V_{DD} = 3.3V	0.85V_{DD}	–	–	
	V_{IL2}			–	–	0.15V_{DD}	
	V_{IH3}	XT	V_{DD} = 3.3V	0.80V_{DD}	–	–	
	V_{IL3}			–	–	0.20V_{DD}	
Input current	I_{IH1}	MSEL0, MSEL1	V_{IN} = V_{DD}	–	–	1	µA
	I_{IL1}		V_{IN} = 0V	–1	–	–	
	I_{IH2}	TSTN	V_{IN} = V_{DD}, built-in pull-up resistor	–	–	1	
	I_{IL2}		V_{IN} = 0V, built-in pull-up resistor	–100	–	–	
	I_{IH3}	XT	V_{IN} = V_{DD}	–	–	40	
	I_{IL3}		V_{IN} = 0V	–40	–	–	
Output voltage	V_{OH}	CLKOUT	I_{OH} = −2mA	V_{DD} − 0.4	–	–	V
	V_{OL}		I_{OL} = 2mA	–	–	0.4	

AC Characteristics

SM8761AA

V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V, Ta = –20 to +80°C unless otherwise noted.

Parameter	Symbol	Pins	Condition		Rating min	Rating typ	Rating max	Unit
Clock frequency	f_{in}	XT	Crystal connection		20	–	40	MHz
			External clock input*1		20	–	108	
Output clock rise time*2	t_r	CLKOUT	C_L = 15pF, V_{OL} = 0.2V_{DD} to V_{OH} = 0.8V_{DD} transition time		–	2.0	–	ns
Output clock fall time*2	t_f	CLKOUT	C_L = 15pF, V_{OH} = 0.8V_{DD} to V_{OL} = 0.2V_{DD} transition time		–	2.0	–	ns
Output clock jitter*2	t_{jitter}	CLKOUT	Cycle-to-cycle jitter, Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	fin = 33MHz	–	200	–	ps
				fin = 75MHz	–	120	–	
Output clock duty cycle*2	Dt	CLKOUT	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}		45	50	55	%
Power-up time*2,*3	t_p	CLKOUT			–	1	5	ms

*1. When using an external clock input, it is recommended that the clock on XT have 50% duty and V_{DD} level signal amplitude. Note that the input signal voltage must not exceed the absolute maximum rating, otherwise it may cause the device to breakdown.
*2. Measured using the circuit in Figure 1 on the NPC standard evaluation board.
*3. The power-up time is the time from when the supply reaches 3.0V after the supply is turned ON until each output clock reaches its designated frequency to within ± 0.1%.

SM8761AB

V_{DD} = 3.3 ± 0.3V, V_{SS} = 0V, Ta = –20 to +80°C unless otherwise noted.

Parameter	Symbol	Pins	Condition		Rating min	Rating typ	Rating max	Unit
Clock frequency	f_{in}	XT	Crystal connection		12	–	32	MHz
			External clock input*1		12	–	32	
Output clock rise time*2	t_r	CLKOUT	C_L = 15pF, V_{OL} = 0.2V_{DD} to V_{OH} = 0.8V_{DD} transition time		–	2.0	–	ns
Output clock fall time*2	t_f	CLKOUT	C_L = 15pF, V_{OH} = 0.8V_{DD} to V_{OL} = 0.2V_{DD} transition time		–	2.0	–	ns
Output clock jitter*2	t_{jitter}	CLKOUT	Cycle-to-cycle jitter, Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	fin = 12MHz	–	450	–	ps
				fin = 16MHz	–	200	–	
				fin = 20MHz	–	300	–	
				fin = 27MHz	–	180	–	
Output clock duty cycle*2	Dt	CLKOUT	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}		45	50	55	%
Power-up time*2,*3	t_p	CLKOUT			–	1	5	ms

*1. When using an external clock input, it is recommended that the clock on XT have 50% duty and V_{DD} level signal amplitude. Note that the input signal voltage must not exceed the absolute maximum rating, otherwise it may cause the device to breakdown.
*2. Measured using the circuit in Figure 1 on the NPC standard evaluation board.
*3. The power-up time is the time from when the supply reaches 3.0V after the supply is turned ON until each output clock reaches its designated frequency to within ± 0.1%.

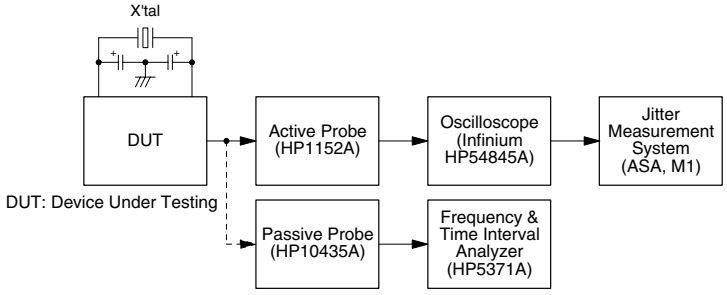


Figure 1. Measurement circuit

FUNCTIONAL DESCRIPTION

Master Clock

The SM8761 series master clock can be generated by the crystal oscillator formed by connecting a crystal between XT (pin 1) and XTN (pin 8) as shown in Figure 2. Alternatively, an external master clock can be input directly on XT (pin 1) as shown in Figure 3. If an external clock is input on XT, it is recommended that the clock have 50% duty and V_{DD} level voltage amplitude. Note that the input clock amplitude voltage must not exceed the absolute maximum rating, otherwise it may cause the SM8761 series to breakdown.

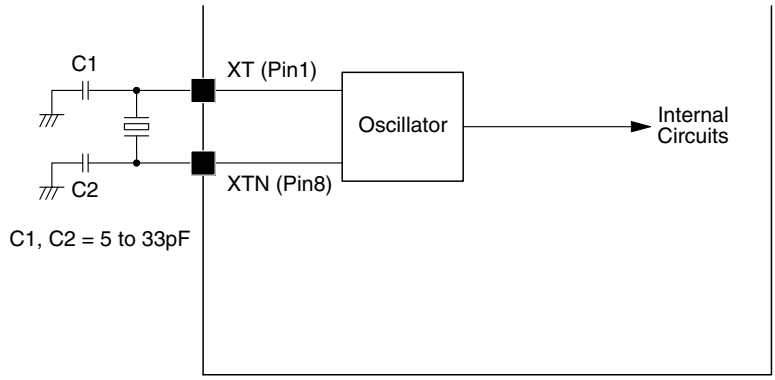


Figure 2. Crystal element connection

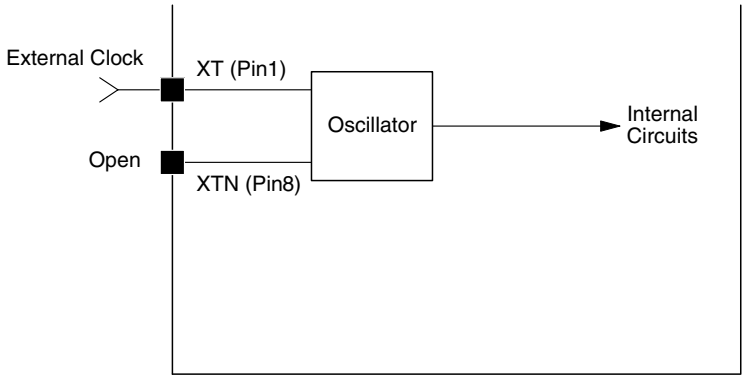


Figure 3. External clock input

Function Controls

The SM8761 series power-down and SS modulation ON/OFF functions are controlled using the MSEL0 and MSEL1 input pins as shown in Table 1.

SM8761AA

MSEL1 (Pin 7)	MSEL0 (Pin 6)	Input/Output frequency range [MHz]	SS mode	SS modulation*1 [%]
L	L	20 to 54 (Low range)	Down spread	–2.3
L	M			–3.2
L	H			–2.8
M	L			–1.9
M	M			–3.8
M	H	50 to 108 (High range)	Down spread	–2.5
H	L			–1.9
H	M			–1.0
H	H			–1.2

*1. The modulation rates in the table above are reference values at 30MHz to 40MHz (Low range) and 70MHz to 80MHz (High range). The modulation rate varies with the input/output frequency.

Note. Signal level “H” represents V_{DD} level, “L” represents V_{SS} level, and “M” represents $1/2V_{DD}$.

SM8761AB

MSEL1 (Pin 7)	MSEL0 (Pin 6)	Input/Output frequency range [MHz]	SS mode	SS modulation*1 [%]
L	L	12 to 18 (Low range)	Center spread	± 1.25
L	M			± 0.75
L	H			± 1.75
M	L			± 2.25
M	M	(reserved)*2		
M	H	18 to 32 (High range)	Center spread	± 2.25
H	L			± 1.25
H	M			± 0.75
H	H			± 1.75

*1. The modulation rates in the table above are reference values at 12MHz (Low range) and 24MHz (High range). The modulation rate varies with the input/output frequency.

*2. If MSEL1 (pin 7) and MSEL0 (pin 6) are both simultaneously "M" level, then SM8761AB operation cannot be guaranteed.

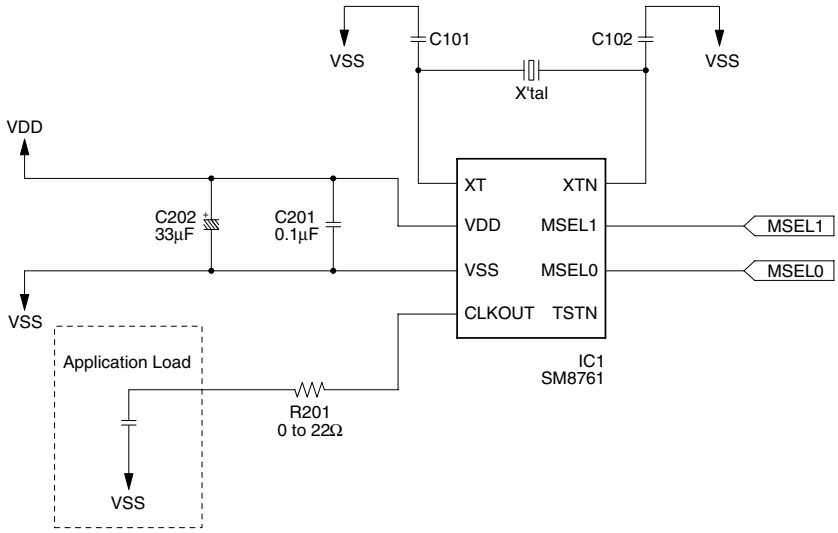
Note. Signal level “H” represents V_{DD} level, “L” represents V_{SS} level, and “M” represents $1/2V_{DD}$.

Typical Connection Circuit

A typical connection circuit diagram is shown in Figure 4.

1) The SM8761 series oscillator circuit between XT and XTN has a built-in feedback resistor (approximately 250kΩ).
2) The oscillator circuit capacitances C101 and C102 connected to XTN and XT, to match the crystal load capacitor.
3) If using an external clock input on XT, then connections to XT and XTN should be as shown in figure 3.
4) R201 is impedance matching resistor for board pattern.
5) C201 and C202 are bypass capacitors inserted between the supply voltage lines.

C201 is a 0.1µF (approximately) multi-layer ceramic capacitor connected directly alongside the SM8761 series.
C202 is a 33µF (approximately) electrolytic capacitor.

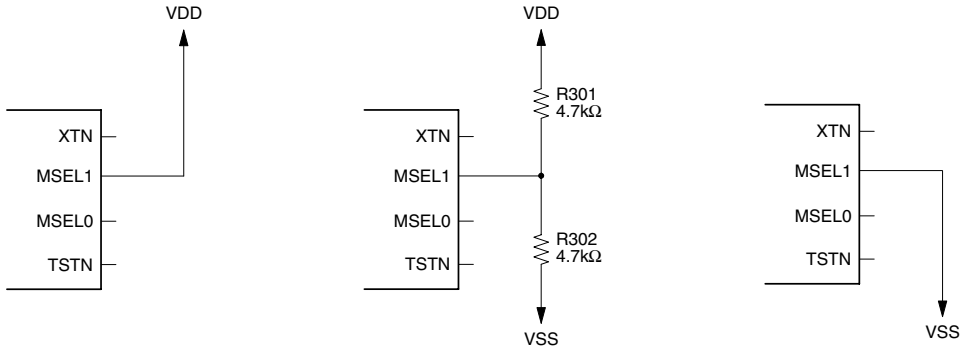


Note. This is a sample connection diagram only, and its use is not a guarantee of SM8761 series device characteristics.

Figure 4. Typical connection circuit

MSEL1 and MSEL0 Connection Method

MSEL1 and MSEL0 both support a $1/2V_{DD}$ "M" level for 3-value ("H", "M", "L") DC voltage input control. Typical connection circuits for each input level shown in figure 5. "H" level is input by connection to VDD, and "L" level by connection to VSS. "M" level is input by connection to the center tap of two identical resistances in series between VDD and VSS. The recommended resistance is 4.7kΩ.

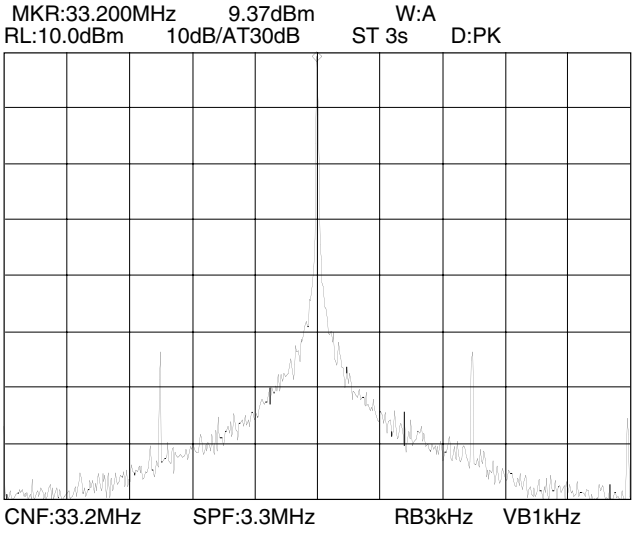


(a)"H" level (b)"M" level (c)"L" level

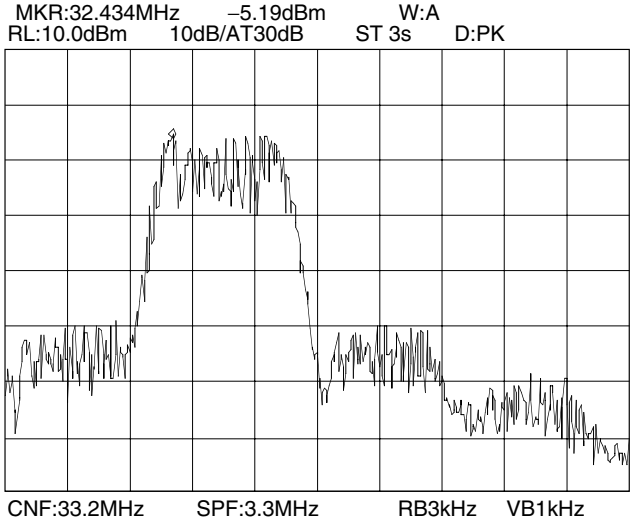
Figure 5. MSEL1 and MSEL0 typical connections

CLKOUT Output Spectrum Sample (SM8761AA)

A sample SM8761AA CLKOUT output spectrum is shown in Figure 6.



(a) NPC test mode: SS OFF, fin = 33.2MHz



(b) MSEL1 = "L"/ MSEL0 = “H”: down spread –2.8%, fin = 33.2MHz

Figure 6. Output spectrum sample

Note. The output spectrum sample in figure (a) is for NPC test mode with the SS function OFF.

Note. These spectrum diagrams were obtained using the NPC evaluation board. These spectrum diagrams are not guaranteed SM8761 series device characteristics.

Please pay your attention to the following points at time of using the products shown in this document.

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