

### DESCRIPTION

SMC4240DM is the dual N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance. This device is ideal for load switch applications.

### PART NUMBER INFORMATION

**SMC 4240D M - TR G**  
 a      b      c      d      e

- a : Company name.
- b : Product Serial number.
- c : Package code                    M:SOP-8
- d : Handling code                    TR:Tape&Reel
- e : Green produce code            G:RoHS Compliant

### FEATURES

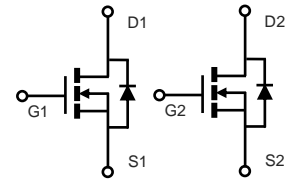
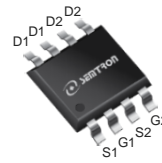
**$V_{DS}=40V, I_D=8A$**

$R_{DS(ON)}=15m\Omega(Typ.)@V_{GS}=10V$   
 $R_{DS(ON)}=18m\Omega(Typ.)@V_{GS}=4.5V$

- ◆ 100% EAS Guaranteed
- ◆ Improved dv/dt capability
- ◆ High power and current handling capability

### APPLICATIONS

- ◆ Power Management
- ◆ DC/DC Power System
- ◆ Load Switch



SOP-8

### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^{\circ}C$ Unless otherwise noted )

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-Source Voltage	40	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current ( $V_{GS}=10V$ )	$T_A=25^{\circ}C$	8
		$T_A=70^{\circ}C$	6.5
$I_{DM}$	Pulsed Drain Current <sup>B</sup>	32	A
$I_{AS}$	Avalanche Current <sup>B</sup>	30	A
EAS	Single Pulse Avalanche energy $L=0.1mH$ <sup>B</sup>	45	mJ
$P_D$	Power Dissipation <sup>A</sup>	$T_A=25^{\circ}C$	2
		$T_A=70^{\circ}C$	1.3
$T_J$	Operation Junction Temperature	-55/150	$^{\circ}C$
$T_{STG}$	Storage Temperature Range	-55/150	$^{\circ}C$

### THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>A</sup>	$t \leq 10s$	62	$^{\circ}C/W$
	Thermal Resistance Junction to Ambient <sup>AC</sup>	Steady-State	90	

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C Unless otherwise noted )

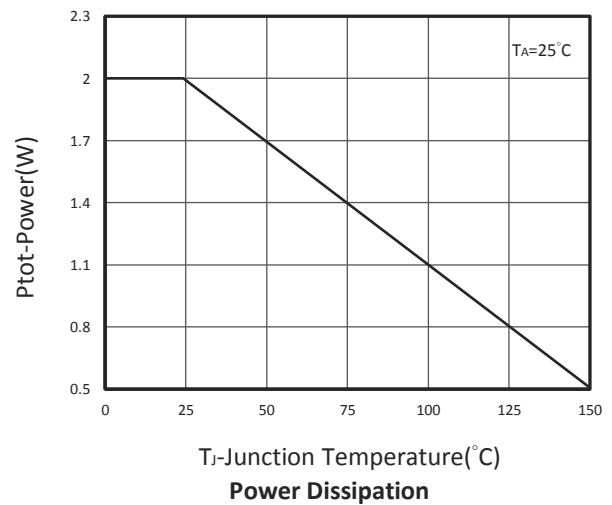
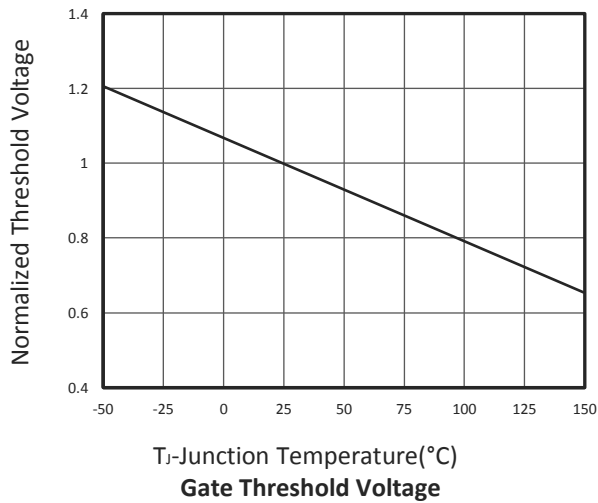
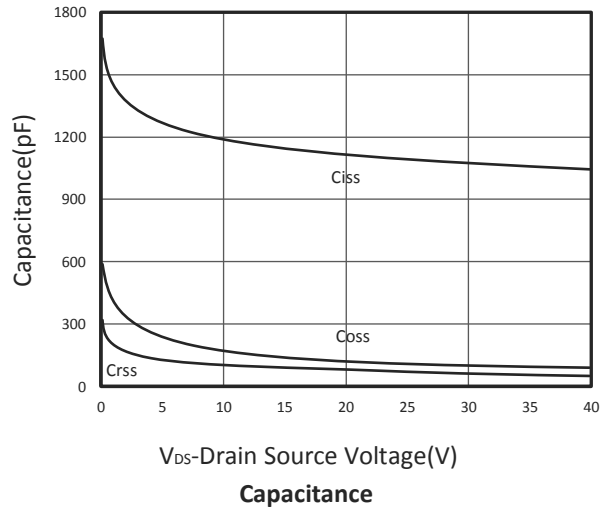
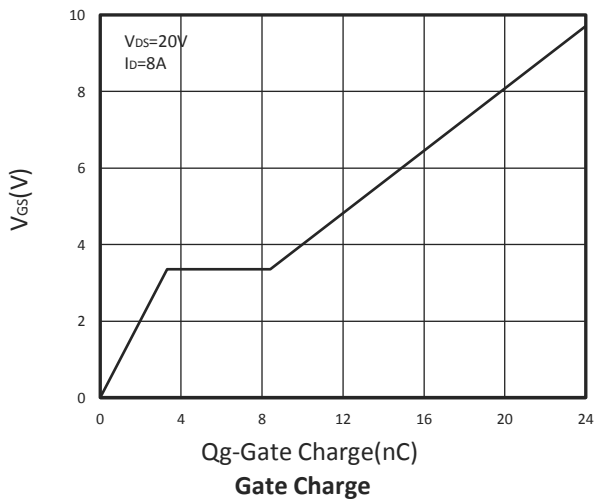
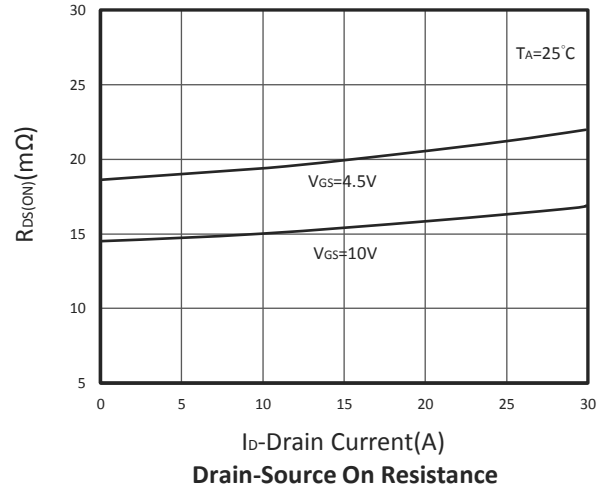
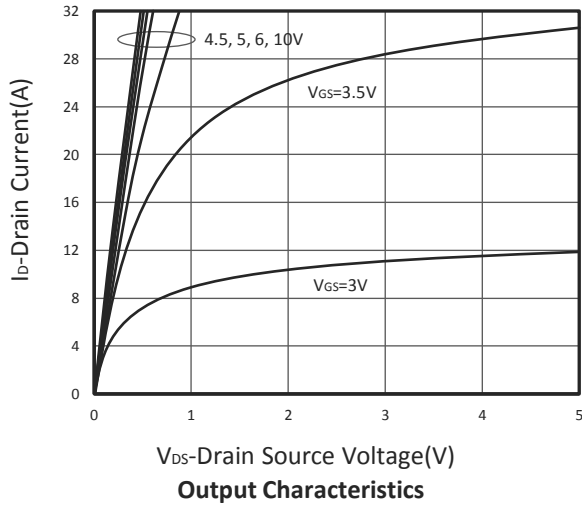
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.7	2.5	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C			1	μA
		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =75°C			10	
R <sub>DS(ON)</sub>	Drain-source On-Resistance <sup>D</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =8A V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A		15 18	18 22	mΩ
G <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =8A		33		S
<b>Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage <sup>D</sup>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V			1	V
I <sub>S</sub>	Diode Continuous Forward Current				8	A
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =8A, di/dt=100A/μs		10		ns
Q <sub>rr</sub>	Reverse Recovery Charge			3.5		nC
<b>Dynamic and Switching Parameters<sup>E</sup></b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =20V, V <sub>GS</sub> =10V, I <sub>D</sub> =8A		24.8	30.1	nC
Q <sub>g</sub>	Total Gate Charge (4.5V)			11.8	13.9	
Q <sub>gs</sub>	Gate-Source Charge			3.6	4.3	
Q <sub>gd</sub>	Gate-Drain Charge			4.7	6.6	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHz		1110	1430	pF
C <sub>oss</sub>	Output Capacitance			108	141	
C <sub>rss</sub>	Reverse Transfer Capacitance			82	115	
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, F=1MHz		2.5		
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =20V, V <sub>GEN</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =1A		7.8	16	nS
t <sub>r</sub>				3	6	
t <sub>d(off)</sub>	Turn-Off Time			28	49	
t <sub>f</sub>				3.1	5.9	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

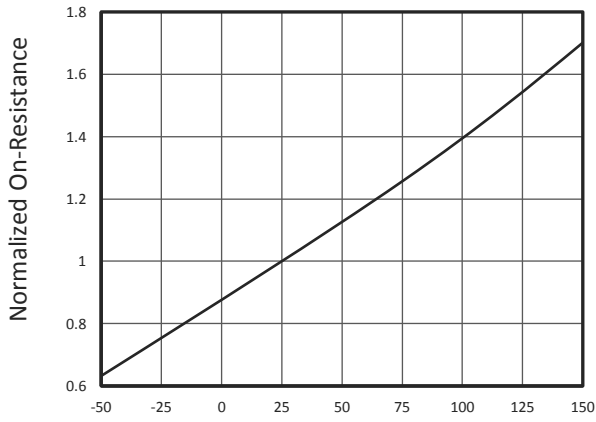
- A. Surface mounted on FR4 board using 1 in<sup>2</sup> pad size.
- B. Pulsed width limited by maximum junction temperature, T<sub>J(MAX)</sub>=150°C (initial temperature T<sub>J</sub>=25°C).
- C. Using ≤ 10s junction-to-ambient thermal resistance is base on T<sub>J(MAX)</sub>=150°C.
- D. Pulse test width ≤300μs and duty cycle ≤ 2%.
- E. Guaranteed by design, not subject to production testing.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

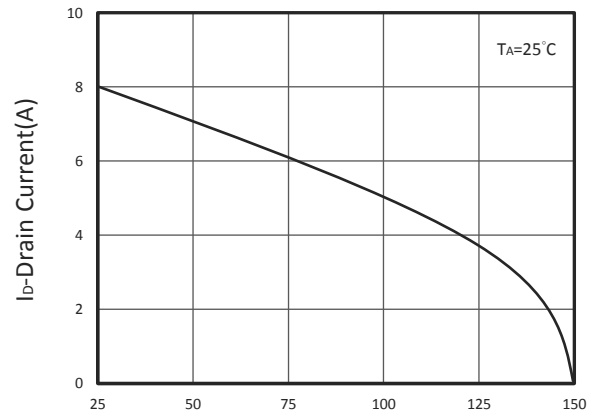
**TYPICAL CHARACTERISTICS**



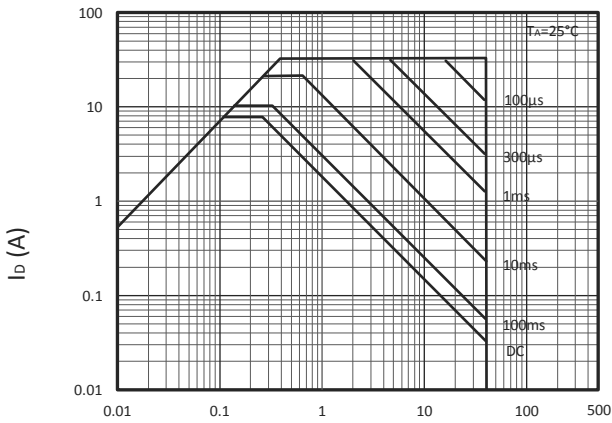
## TYPICAL CHARACTERISTICS



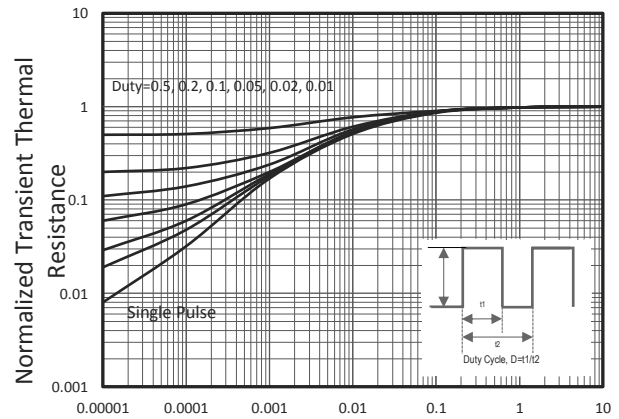
T<sub>J</sub>-Junction Temperature(°C)  
Drain-Source On Resistance



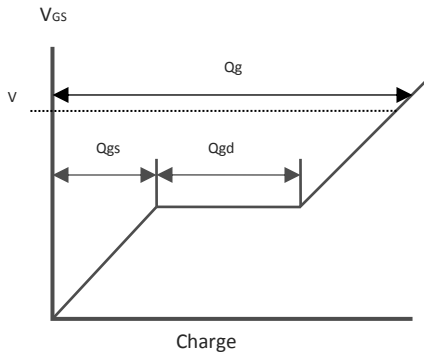
T<sub>J</sub>-Junction Temperature(°C)  
Drain Current vs T<sub>J</sub>



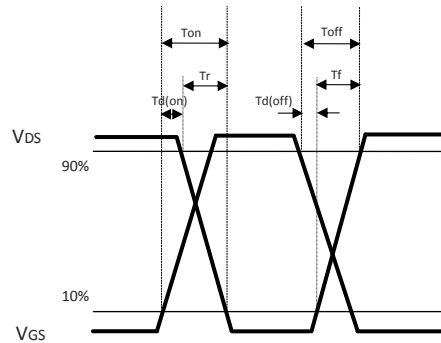
V<sub>DS</sub> Voltage (V)  
Maximum Safe Operation Area



Square Wave Pulse Duration(Sec)  
Thermal Transient Impedance

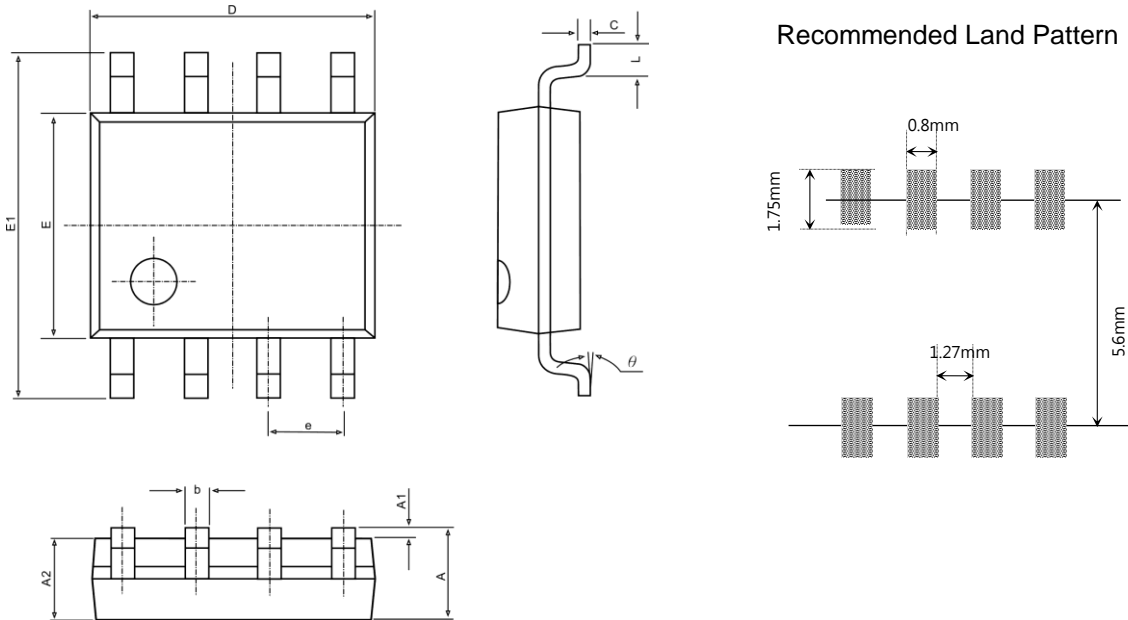


Gate Chrg Waveform



Switching Time Waveform

## ■ SOP-8 PACKAGE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.390	0.490	0.015	0.019
c	0.200	0.250	0.008	0.010
D	4.800	5.100	0.189	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC		0.050 BSC	
L	0.500	0.800	0.020	0.031
θ	0°	8°	0°	8°