

## 30V N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SMC4734 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density and trench DMOS technology.

It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

These devices are well suited for high efficiency fast switching applications.

*SMC4734PD-TRG ROHS Compliant This is Halogen Free*

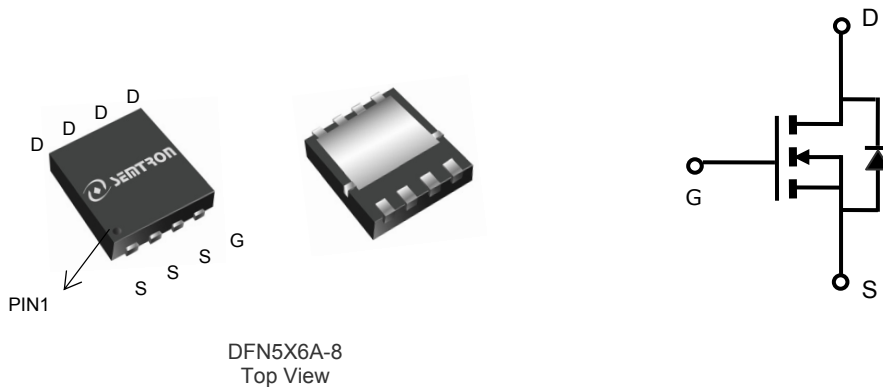
### FEATURE

- ◆ 30V / 70A
- ◆  $R_{DS(ON)} = 4.5m\Omega(typ.)@V_{GS} = 10V$
- ◆  $R_{DS(ON)} = 5.5m\Omega(typ.)@V_{GS} = 4.5V$
- ◆ Low gate charge
- ◆ Improved dv/dt capability
- ◆ High power and current handling capability
- ◆ 100% EAS Guaranteed

### APPLICATIONS

- ◆ High Frequency DC/DC converters
- ◆ Portable Equipment and Battery Powered Systems.
- ◆ Load Switch.

### PIN CONFIGURATION



### PART NUMBER INFORMATION

<p><b>SMC 4734 PD - TR G</b></p> <p>a      b      c      d      e</p>	<p>a : Company name.</p> <p>b : Product Serial number.</p> <p>c : Package code</p> <p>d : Handling code</p> <p>e : Green produce code</p>
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## ORDERING INFORMATION

Part Number	Package Code	Handling Code	Shipping
SMC4734PD-TRG	PD : DFN5X6A-8	TR : Tape&Reel	2.5K/Reel

- ※ Year Code : 0 ~ 9, 2010 : 0
- ※ Week Code : A(1~2) ~ Z(53~54)
- ※ DFN5X6A-8 : Only available in tape and reel packaging.

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ Unless otherwise noted )

Symbol	Parameter	Typical	Unit
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>A</sup>	$T_C=25^\circ\text{C}$	20
		$T_C=100^\circ\text{C}$	15
$I_{DM}$	Pulsed Drain Current <sup>A</sup>	$T_C=25^\circ\text{C}$	70
$E_{AS}$	Single Pulse Avalanche energy $L=0.1\text{mH}$ <sup>B</sup>	65	mJ
$I_{AS}$	Avalanche Current <sup>B</sup>	46	A
$P_D$	Power Dissipation <sup>F</sup>	$T_C=25^\circ\text{C}$	56
		$T_C=100^\circ\text{C}$	42
$P_D$	Power Dissipation <sup>A</sup> Surface-mounted	$T_C=25^\circ\text{C}$	2.2
		$T_C=100^\circ\text{C}$	1.5
$T_J$	Operation Junction Temperature	-55/150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55/150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient <sup>C</sup> Steady-State	60	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction to Lead <sup>C</sup> Steady-State	2.2	$^\circ\text{C}/\text{W}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

A. Surface-mounted on FR-4 board using 1 sq-in pad, 1 oz Cu.

B. The EAS data shows Max. rating . The test condition is  $V_{DD}=25\text{V}$ ,  $V_{GS}=10\text{V}$ ,  $L=0.1\text{mH}$ ,  $I_{AS}=20\text{A}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$ .

C. UIS tested and pulse width limited by maximum junction temperature  $150^\circ\text{C}$  (initial temperature  $T_J=25^\circ\text{C}$ ).

F. The power dissipation  $P_D$  is based on  $T_J(\text{MAX})=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper.

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ Unless otherwise noted )

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Static Parameters</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage <sup>D</sup>	$V_{GS} = 0V, I_D = 250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage <sup>D</sup>	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	1.5	2.0	V
$I_{GSS}$	Gate Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 120V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24V, V_{GS} = 0V$ $T_J = 25^\circ\text{C}$			1	$\mu A$
		$V_{DS} = 24V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$			10	
$R_{DS(ON)}$	Drain-source On-Resistance <sup>D</sup>	$V_{GS} = 10V, I_D = 20A$		4.5	6	m $\Omega$
		$V_{GS} = 4.5V, I_D = 15A$		5.5	7	
$G_{fs}$	Forward Transconductance <sup>D</sup>	$V_{DS} = 10V, I_D = 20A$		41		S
<b>Source-Drain Diode</b>						
$V_{SD}$	Diode Forward Voltage <sup>B</sup>	$I_S = 1A, V_{GS} = 0V$		0.7	1.0	V
$I_S$	Continuous Source Current				78	A
<b>Dynamic Parameters</b>						
$Q_g(4.5V)$	Total Gate Charge	$V_{DS} = 15V, V_{GS} = 4.5V$ $I_D = 15A$		22		nC
$Q_{gs}$	Gate-Source Charge			7.8		
$Q_{gd}$	Gate-Drain Charge			7.2		
$C_{iss}$	Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V$ $f = 1\text{MHz}$		2212		pF
$C_{oss}$	Output Capacitance			252		
$C_{rss}$	Reverse Transfer Capacitance			203		
$R_G$	Gate Resistance	$V_{GS} = 0V, V_{DS} = 0V,$ $F = 1\text{MHz}$		1.6	2.2	$\Omega$
$t_{d(on)}$	Turn-On Time <sup>E</sup>	$V_{DD} = 15V, V_{GEN} = 10V,$ $R_G = 3.3\Omega, I_D = 15A$		8.2		nS
$t_r$				17		
$t_{d(off)}$	Turn-Off Time <sup>E</sup>			39		
$t_f$				11.2		

Note:

D. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$

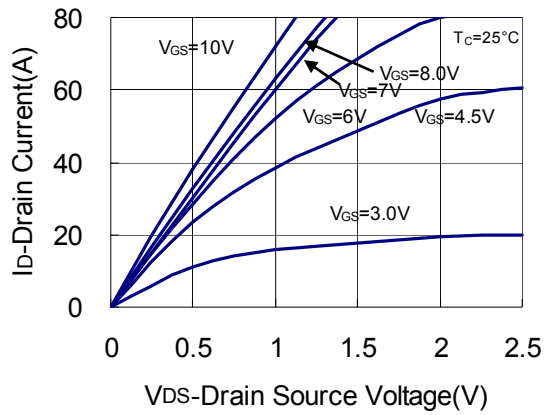
E. Pulsed width limited by maximum junction temperature.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date

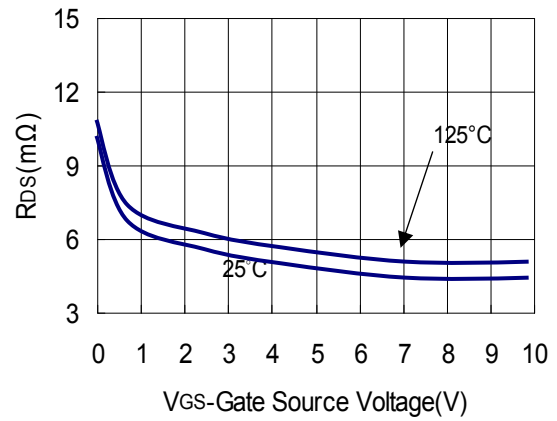
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## TYPICAL CHARACTERISTICS

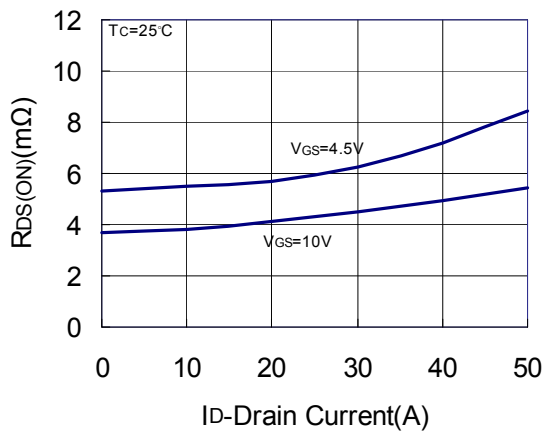
### Output Characteristics



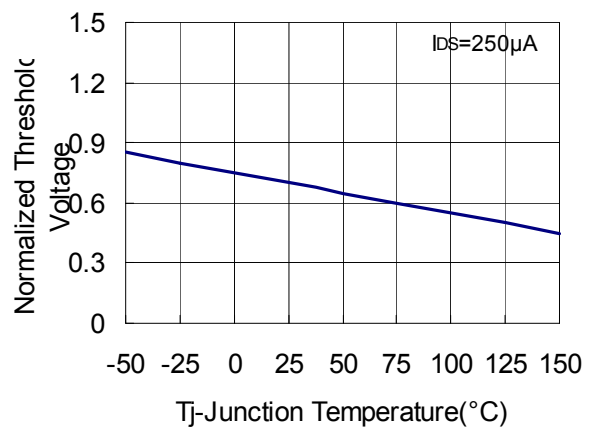
### Drain-Source On Resistance



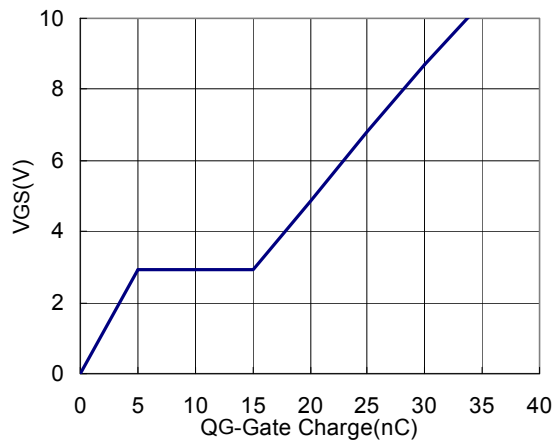
### Transfer Characteristics



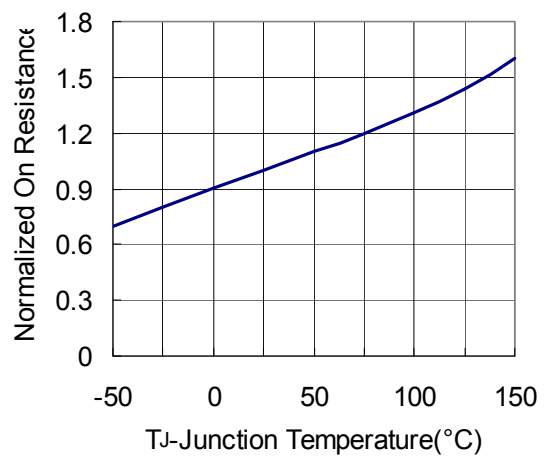
### Gate Threshold Voltage



### Gate Charge

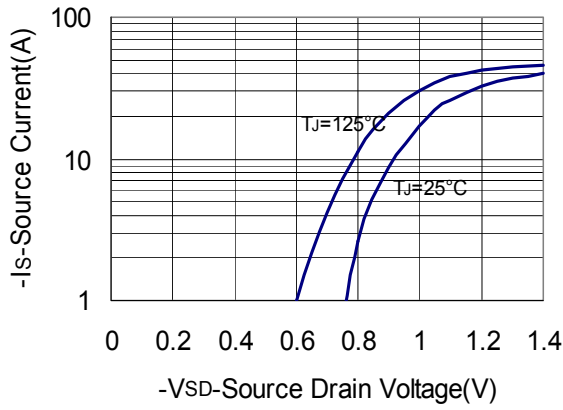


### Drain Source On Resistance

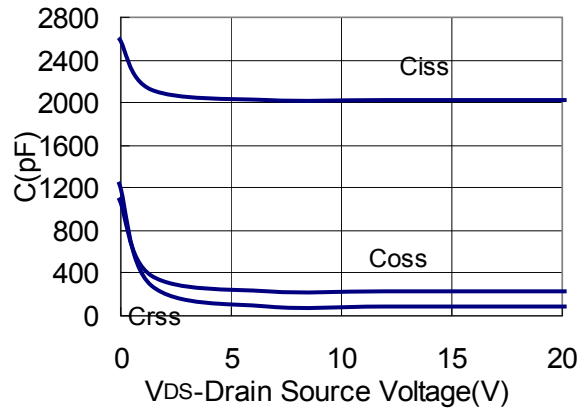


## TYPICAL CHARACTERISTICS

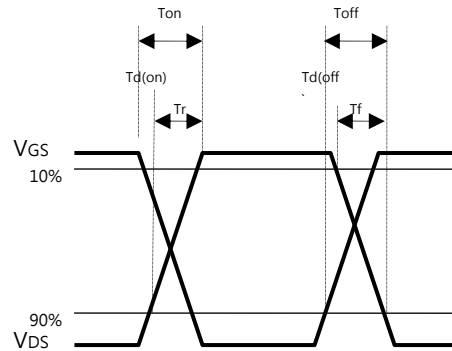
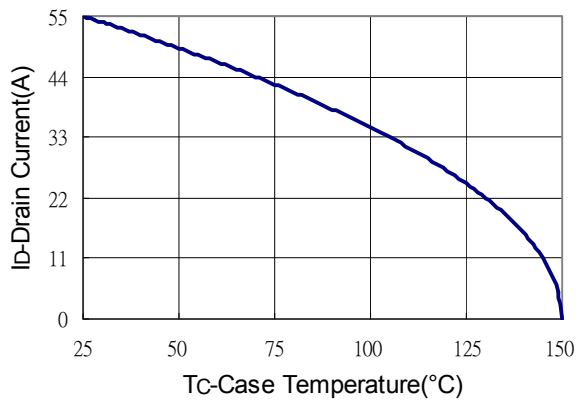
Source Drain Diode Forward



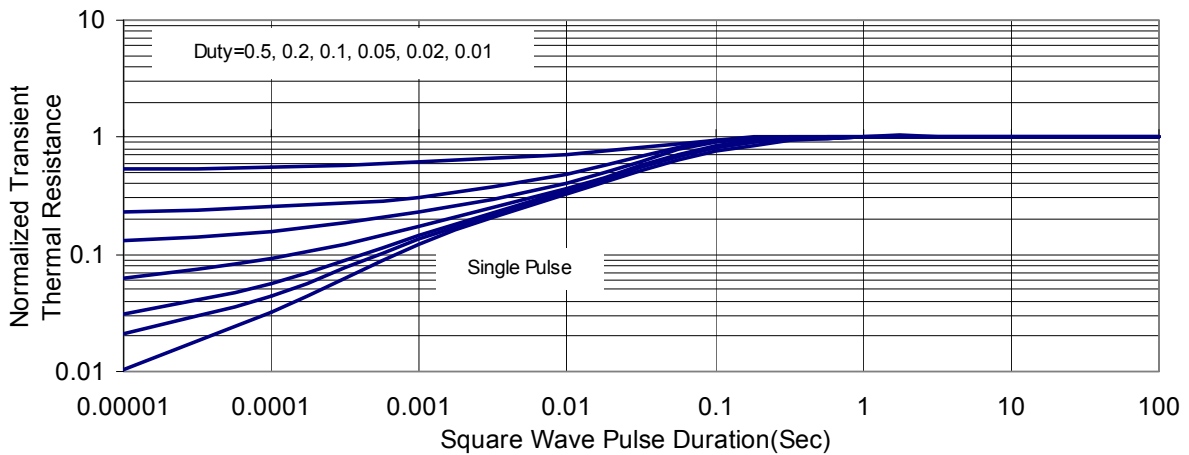
Capacitance



Drain Current



Thermal Transient Impedance



## DFN5X6A-8 PACKAGE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
D2	4.824	4.976	0.190	0.196
E1	3.375	3.575	0.133	0.141
E2	5.674	5.826	0.223	0.229
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
k	1.190	1.390	0.047	0.055
L	0.559	0.325	0.011	0.013
L1	0.424	0.725	0.027	0.029
H	0.574	0.325	0.011	0.013
$\Theta$	10°	12°	10°	12°

