

30V N-Channel Enhancement Mode MOSFET

■ DESCRIPTION

The SMC4866 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density and trench DMOS technology.

It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

These devices are well suited for high efficiency fast switching applications.

SMC4866PDC-TRG ROHS Compliant This is Halogen Free

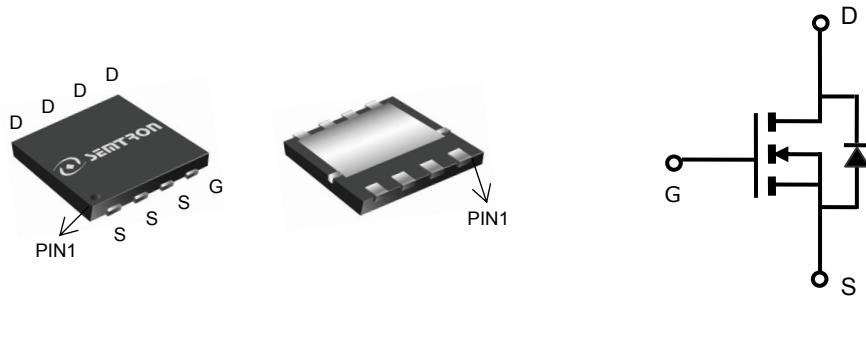
■ FEATURE

- ◆ 30V / 35A
- ◆ $R_{DS(ON)} = 7.5m\Omega$ (typ.)@ $V_{GS} = 10V$
- ◆ $R_{DS(ON)} = 9.5m\Omega$ (typ.)@ $V_{GS} = 4.5V$
- ◆ Fast switch
- ◆ Low gate charge
- ◆ Improved dv/dt capability
- ◆ High power and current handling capability
- ◆ 100% EAS Guaranteed

■ APPLICATIONS

- ◆ High Frequency DC/DC converters
- ◆ Portable Equipment and Battery Powered Systems.

■ PIN CONFIGURATION



DFN3.3X3.3A-8
Top View

■ PART NUMBER INFORMATION

SMC 4866 PDC - TR G a b c d e	a : Company name. b : Product Serial number. c : Package code d : Handling code e : Green produce code
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■ ORDERING INFORMATION

Part Number	Package Code	Handling Code	Shipping
SMC4866PDC-TRG	PDC : DFN3.3X3.3A-8	TR : Tape&Reel	3K/Reel

※ Year Code : 0 ~ 9, 2010 : 0

※ Week Code : A(1~2) ~ Z(53~54)

※ DFN3.3X3.3A-8 : Only available in tape and reel packaging.

■ ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ^A	$T_c=25^\circ\text{C}$	18
		$T_c=100^\circ\text{C}$	11
I_{DM}	Pulsed Drain Current ^A	$T_c=25^\circ\text{C}$	A
E_{AS}	Single Pulse Avalanche energy $L=0.1\text{mH}$ ^B	20	mJ
I_{AS}	Avalanche Current ^B	30	A
P_D	Power Dissipation ^F	$T_c=25^\circ\text{C}$	27
		$T_c=100^\circ\text{C}$	11
P_D	Power Dissipation ^A Surface-mounted	$T_c=25^\circ\text{C}$	2.0
		$T_c=100^\circ\text{C}$	1.2
T_J	Operation Junction Temperature	-55/150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55/150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient ^C Steady-State	60	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction to Lead ^C Steady-State	3.5	$^\circ\text{C}/\text{W}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

A. Surface-mounted on FR-4 board using 1 sq-in pad, 1 oz Cu.

 B. The EAS data shows Max. rating . The test condition is $V_{DD}=25\text{V}$, $V_{GS}=10\text{V}$, $L=0.1\text{mH}$, $I_{AS}=30\text{A}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.

 C. UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_j=25^\circ\text{C}$).

 F. The power dissipation PD is based on $T_J(\text{MAX})=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper.

ELECTRICAL CHARACTERISTICS($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
Static Parameters							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage ^D	$V_{GS}=0V, I_D=250\mu A$	30			V	
$V_{GS(th)}$	Gate Threshold Voltage ^D	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.5	V	
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V$ $T_J=25^\circ C$			1	μA	
		$V_{DS}=24V, V_{GS}=0V$ $T_J=125^\circ C$			10		
$R_{DS(ON)}$	Drain-source On-Resistance ^D	$V_{GS}=10V, I_D=18A$ $V_{GS}=4.5V, I_D=11A$		7.5 9.5	9 13	$m\Omega$	
G_f	Forward Transconductance ^D	$V_{DS}=10V, I_D=8A$		18		S	
Source-Drain Diode							
V_{SD}	Diode Forward Voltage ^B	$I_S=1A, V_{GS}=0V$		0.7	1.0	V	
I_S	Continuous Source Current				20	A	
Dynamic Parameters							
$Q_g(4.5V)$	Total Gate Charge	$V_{DS}=15V, V_{GS}=4.5V$ $I_D=15A$		10.2		nC	
Q_{gs}	Gate-Source Charge			2.1			
Q_{gd}	Gate-Drain Charge			4.0			
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V$ $f=1MHz$		1142		pF	
C_{oss}	Output Capacitance			192			
C_{rss}	Reverse Transfer Capacitance			90			
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$		2.0	3.0	Ω	
$t_{d(on)}$	Turn-On Time ^E	$V_{DD}=15V, V_{GEN}=10V,$ $R_G=3.3\Omega,$		6.2		nS	
t_r				68			
$t_{d(off)}$	Turn-Off Time ^E			22			
t_f				8.1			

Note:

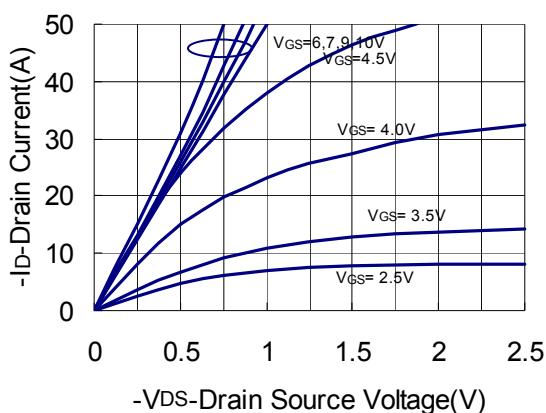
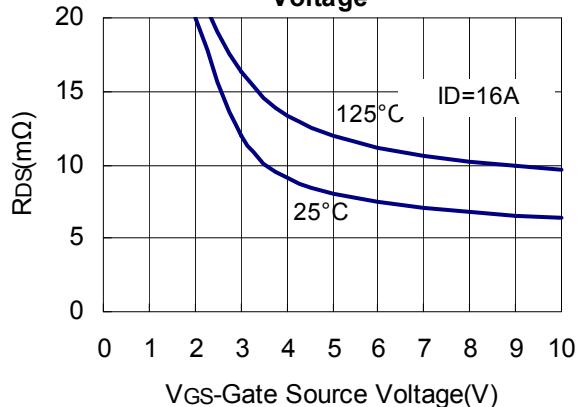
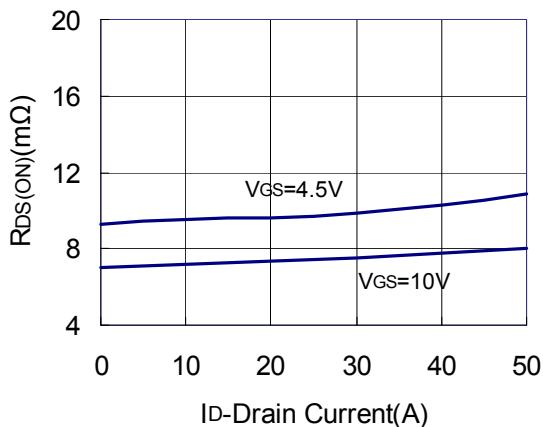
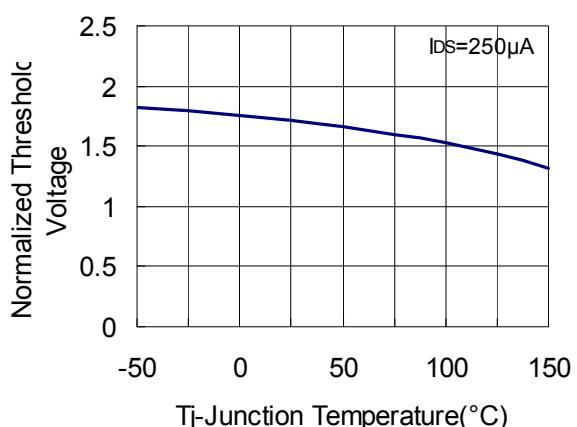
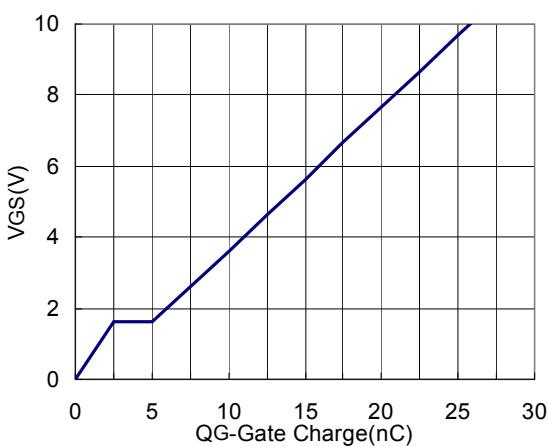
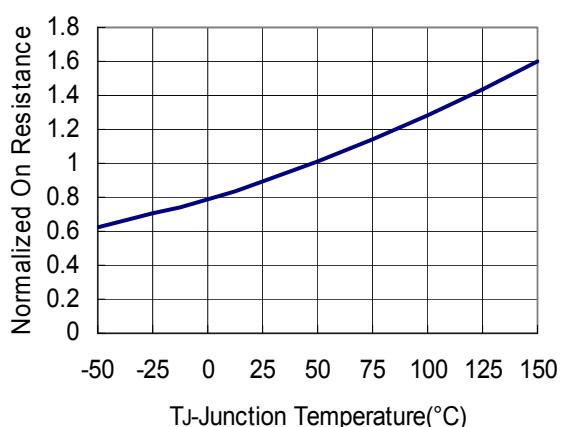
D. The data tested by pulsed , pulse width $\leq 300\mu S$, duty cycle $\leq 2\%$

E. Pulsed width limited by maximum junction temperature.

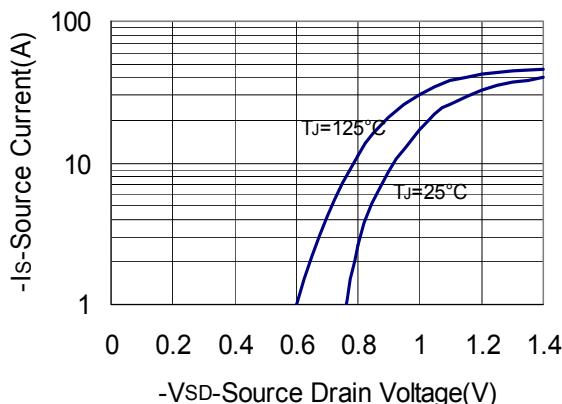
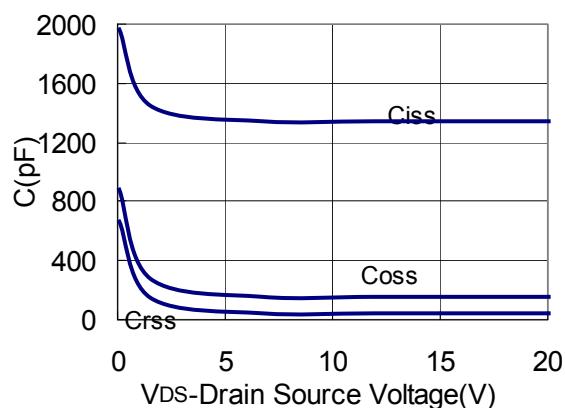
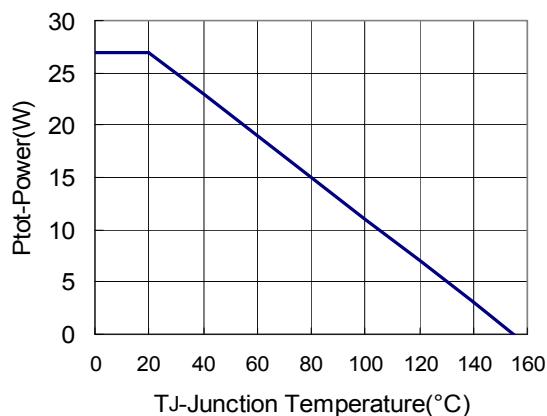
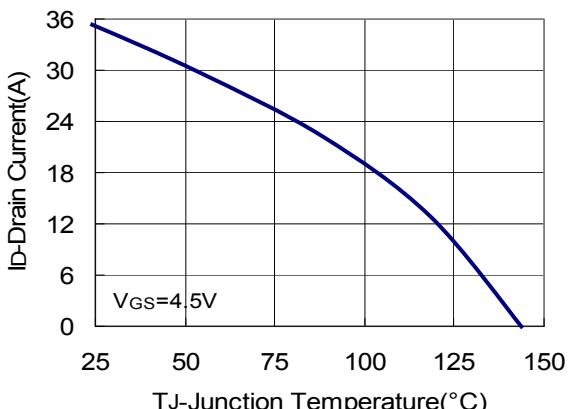
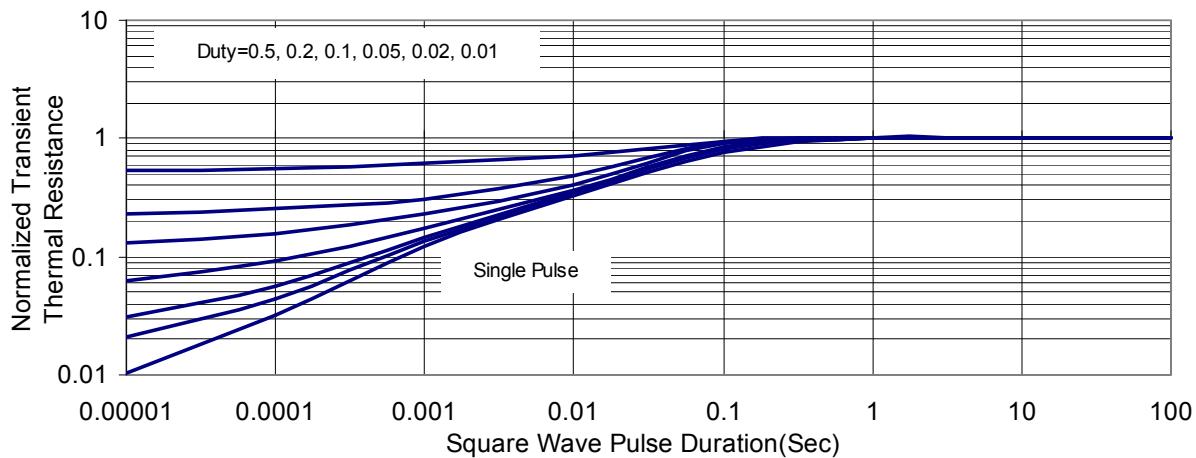
The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date

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TYPICAL CHARACTERISTICS

Output Characteristics

On Resistance VS Gate Source Voltage

Transfer Characteristics

Gate Threshold Voltage

Gate Charge

Normalized RDS(On) V.S. TJ


■ TYPICAL CHARACTERISTICS

Source Drain Diode Forward

Capacitance

Power Dissipation

Drain Current

Thermal Transient Impedance


■ DFN3.3X3.3A-8 PACKAGE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.65	0.85	0.026	0.033
A1	0.152REF.		0.006REF.	
A2	0~0.05		0~0.02	
D	2.900	3.100	0.114	0.122
D1	2.540	2.740	0.100	0.011
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.365	1.765	0.054	0.069
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.260	0.460	0.010	0.018
L1	0.017	0.465	0.006	0.018
L2	0~0.1		0~0.004	
L3	0~0.1		0~0.004	
H	0.3	0.5	0.012	0.02
Θ	9°	13°	9°	13°

