

-30V Dual P-Channel Fast Switching MOSFETs

Dual P-Channel Fast Switching MOSFETs

DESCRIPTION

The SMC4953A is the Dual P-Channel logic enhancement mode power field effect transistor is produced using high cell density, advanced trench technology to provide excellent $R_{DS(ON)}$. This device is suitable for use as a load switch or in PWM and gate charge for most of the synchronous buck converter applications.

SMC4953AM-TRG ROHS Compliant This is Halogen Free

FEATURE

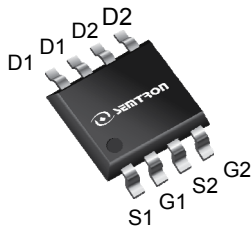
- ◆ **-30V/-5.3A, $R_{DS(ON)}=46m\Omega(typ.)@V_{GS}=-10V$**
- ◆ **-30V/-3.6A, $R_{DS(ON)}=75m\Omega(typ.)@V_{GS}=-4.5V$**
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability

APPLICATIONS

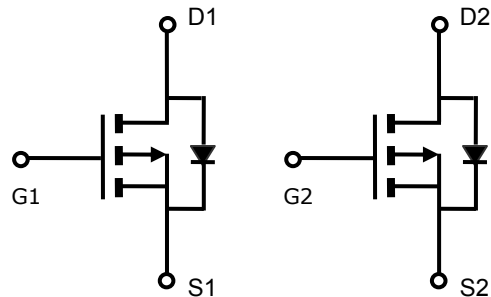
- ◆ Power Management in Note book
- ◆ Portable Equipment
- ◆ DSC
- ◆ LCD Display inverter
- ◆ Battery Powered System
- ◆ DC/DC Converter
- ◆ Load Switch



PIN CONFIGURATION



SOP-8
Top View



PART NUMBER INFORMATION

<p>SMC 4953A M - TR G</p> <p>a b c d e</p>	<p>a : Company name. b : Product Serial number. c : Package code d : Handling code e : Green produce code</p>
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ORDERING INFORMATION

Part Number	Package Code	Handling Code	Shipping
SMC4953AM-TRG	M : SOP-8	TR : Tape&Reel	2.5K/Reel

※ Year Code : 00 ~ 90, 2010 : 00
 ※ Week Code : 01 ~ 54
 ※ SOP-8 : Only available in tape and reel packaging.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V _{DSS}	Drain-Source Voltage	-30	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Continuous Drain Current, V _{GS} =10V ^A	T _A =25°C	-5.3
		T _A =70°C	-4.0
I _{DM}	Pulsed Drain Current ^B	-12	A
E _{AS}	Single Pulse Avalanche energy L=0.1mH ^C	38	mJ
I _{AS}	Avalanche Current	15	A
P _D	Power Dissipation	T _A =25°C	2.0
		T _A =70°C	1.4
T _J	Operation Junction Temperature	-55/150	°C
T _{STG}	Storage Temperature Range	-55/150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

THERMAL DATA

Symbol	Parameter	Min	Typ	Max	Unit
R _{θJA}	Thermal Resistance-Junction to Ambient ^A Steady-State			85	°C/W
R _{θJC}	Thermal Resistance Junction to Lead ^A Steady-State			60	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0		-2.0	V
I_{GSS}	Gate Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$ $T_J = 25^\circ\text{C}$			-1	μA
		$V_{DS} = -24V, V_{GS} = 0V$ $T_J = 55^\circ\text{C}$			-5	
$R_{DS(ON)}$	Drain-source On-Resistance ^B	$V_{GS} = -10V, I_D = -5.3A$ $V_{GS} = -4.5V, I_D = -3.6A$		46 75	55 85	m Ω
G_{fs}	Forward Transconductance	$V_{DS} = -10V, I_D = -5.3A$		5.5		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage ^B	$I_S = -1.7A, V_{GS} = 0V$		-0.8	-1.2	V
I_S	Continuous Source Current ^{AD}				-6	A
Dynamic Parameters						
$Q_g (-4.5V)$	Total Gate Charge	$V_{DS} = -20V, V_{GS} = -4.5V$ $I_D = -5.3A$		5.3		nC
Q_{gs}	Gate-Source Charge			1.25		
Q_{gd}	Gate-Drain Charge			2.35		
C_{iss}	Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V$ $f = 1\text{MHz}$		468		pF
C_{oss}	Output Capacitance			83		
C_{rss}	Reverse Transfer Capacitance			70		
$t_{d(on)}$	Turn-On Time	$V_{DD} = -15V, V_{GEN} = -10V,$ $I_D = -1.0A, R_G = 3.3\Omega,$		18.5		nS
t_r				11.5		
$t_{d(off)}$	Turn-Off Time			38.8		
t_f				5.3		

Note:

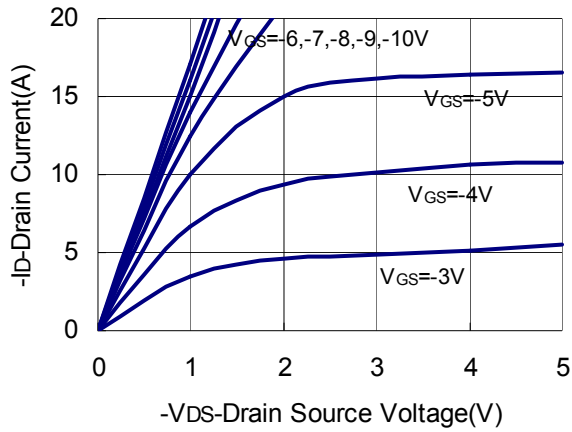
- The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$.
- The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD} = -25V, V_{GS} = -10V, L = 0.1\text{mH}$.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date

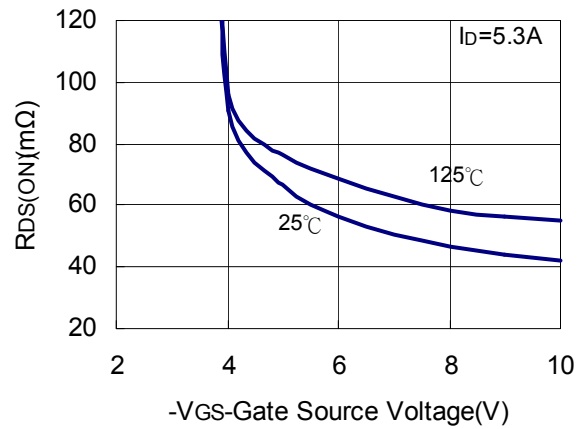
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TYPICAL CHARACTERISTICS

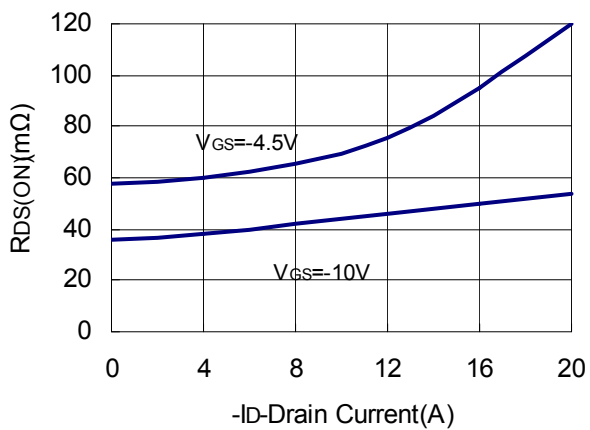
Output Characteristics



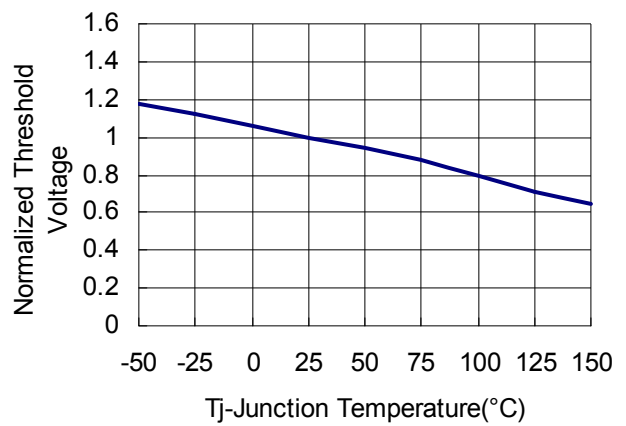
Drain-Source On Resistance



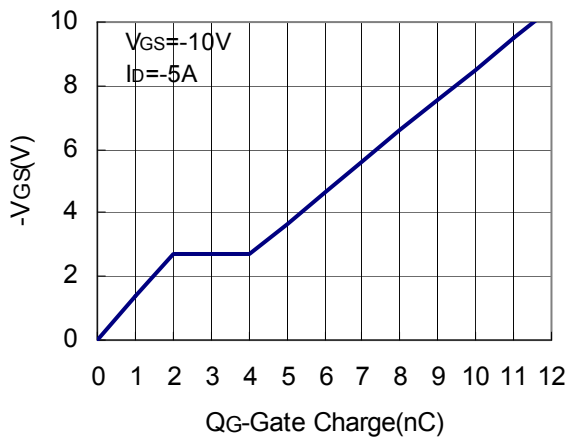
Drain Source On Resistance



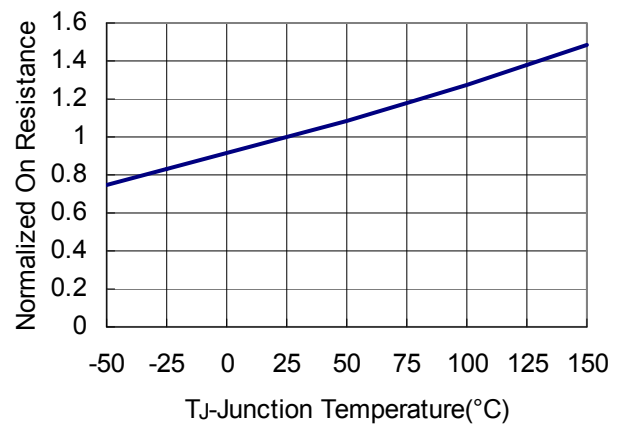
Gate Threshold Voltage



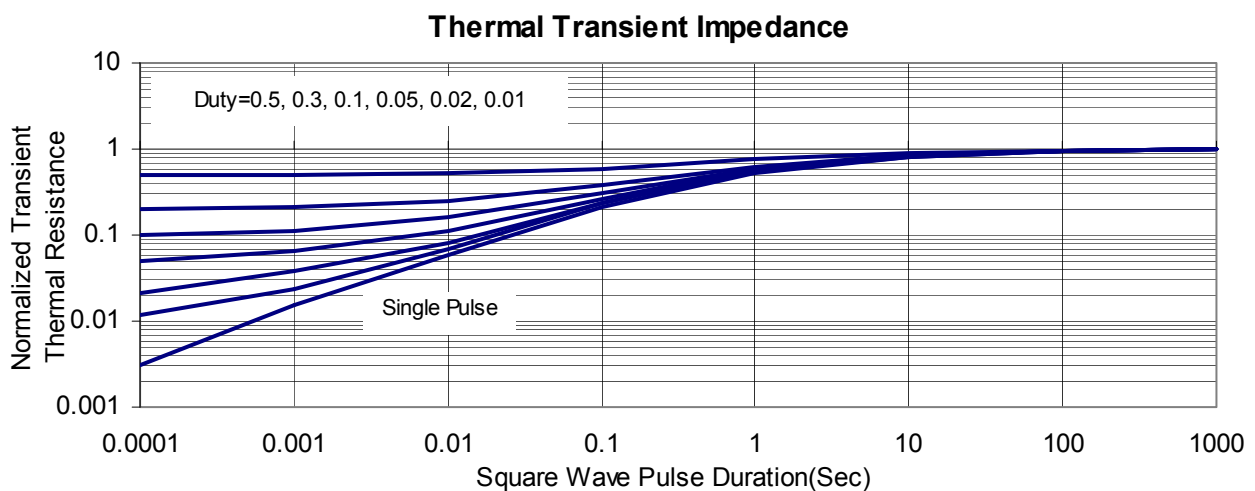
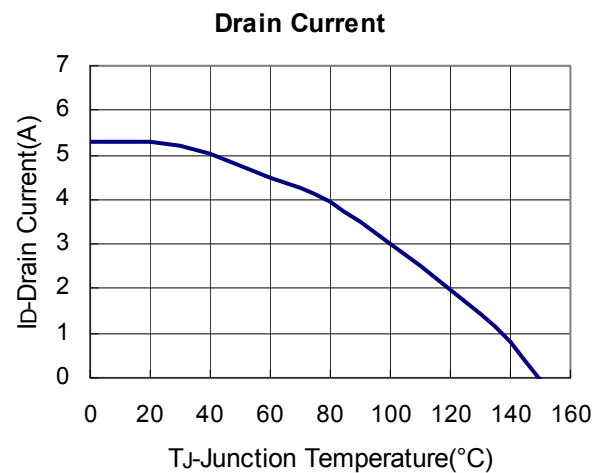
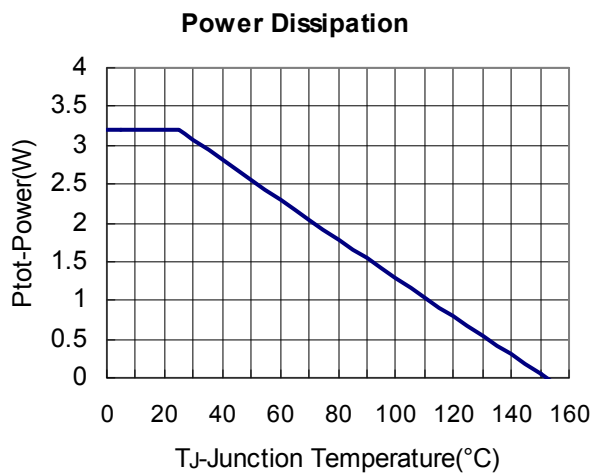
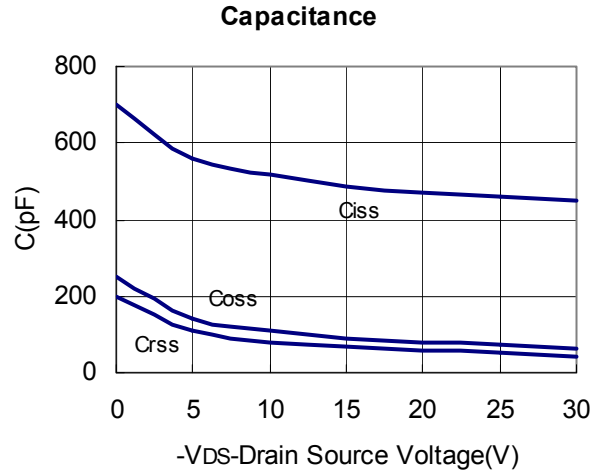
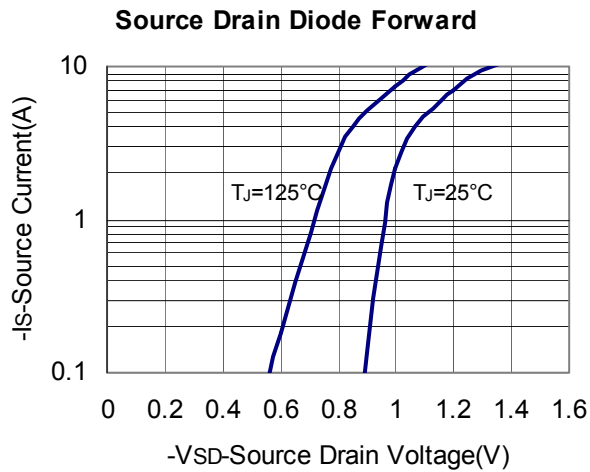
Gate Charge



Drain Source On Resistance



TYPICAL CHARACTERISTICS



■ SOP-8 PACKAGE DIMENSIONS

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.040	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

