

SMC82C55AC-5

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

- 24 Bit Input/Output
- Improved DC Driving Capability
- Low Power

DESCRIPTION

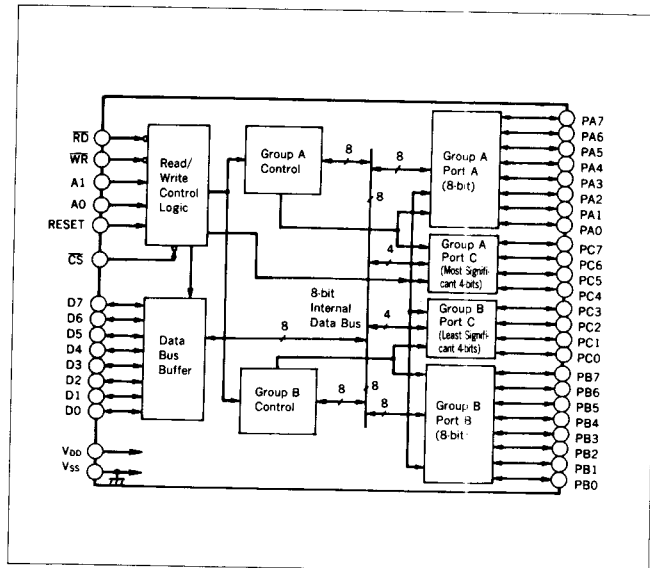
The SMC82C55AC-5 is a CMOS General Purpose Programmable I/O device designed for use with an 8/16 bit CPU. The device has 24 programmable I/O pins that can be individually programmed in two groups of 12.

FEATURES

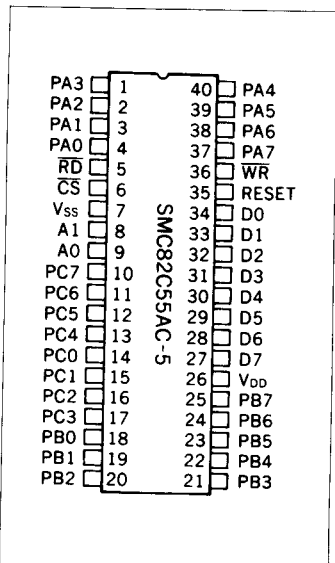
- 24 programmable I/O pins
- Compatible with 80XX series of microprocessors
- Direct bit set/reset capability
- Improved DC driving capability
- Single 5V ($\pm 10\%$) power supply
- TTL compatible
- Package.....40-pin DIP
40-pin SOP*

* Under development

BLOCK DIAGRAM



PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$, $T_a=25^{\circ}C$)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	With respect to V_{SS}	-0.3 to 7	V
Input voltage	V_I		-0.3 to $V_{DD}+0.3$	V
Output voltage	V_O		-0.3 to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	—	-20 to 75	$^{\circ}C$
Storage temperature	T_{stg}	—	-65 to 150	$^{\circ}C$
Soldering temperature and time	T_{sol}	—	260 $^{\circ}C$, 10s (lead)	—

■ RECOMMENDED OPERATING CONDITIONS

($T_a = -20$ to $75^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5	5.5	V
Supply voltage	V_{SS}	—	—	0	—	V

■ ELECTRICAL CHARACTERISTICS

($T_a = -20$ to $75^{\circ}C$, $V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, unless otherwise noted)

● DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—	2.0	—	$V_{DD}+0.3$	V
Low-level input voltage	V_{IL}	—	-0.3	—	0.8	V
Output high voltage*2	V_{OH}	$I_{OH} = -400\mu A$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 2.5mA$	—	—	0.45	V
Supply current from V_{DD}	I_{DD}	$V_{SS}=0V$. All input mode. RESET=0V. Other pins= V_{DD}	—	—	10	μA
Input leak current	I_{LI}	$V_{SS}=0V$, $V_I=0V$, V_{DD}	—	—	± 10	μA
Off-state output current	I_{OZ}	$V_{SS}=0V$, $V_I=0V$, V_{DD}	—	—	± 10	μA
Input capacitance	C_I	$V_{IL}=V_{SS}$, $f=1MHz$, 25mVrms, $T_a=25^{\circ}C$	—	—	10	pF
Input/output terminal capacitance	$C_{I/O}$	$V_{I/O}=V_{SS}$, $f=1MHz$, 25mVrms, $T_a=25^{\circ}C$	—	—	20	pF

*1 Current flowing into an IC is positive, out is negative.

*2 The sum total I_{OH} current must be less than -64mA on port B, C, and -32mA on Port A.

● AC Electrical Characteristics

($T_a = -20$ to $75^{\circ}C$, $V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, unless otherwise noted)

○ Timing Requirements

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Read pulse width	$t_{W(R)}$	t_{RR}		200	—	—	ns
Peripheral setup time before read	$t_{SU(PE-R)}$	t_{IR}		0	—	—	ns
Peripheral hold time after read	$t_{H(R-PE)}$	t_{HR}		0	—	—	ns
Address setup time before read	$t_{SU(A-R)}$	t_{AR}		0	—	—	ns
Address hold time after read	$t_{H(R-A)}$	t_{RA}		0	—	—	ns
Write pulse width	$t_{W(W)}$	t_{WW}		200	—	—	ns
Data setup time before write	$t_{SU(DQ-W)}$	t_{DW}		100	—	—	ns
Data hold time after write	$t_{H(W-DQ)}$	t_{WD}		0	—	—	ns
Address setup time before write	$t_{SU(A-W)}$	t_{AW}		0	—	—	ns
Address hold time after write	$t_{H(W-A)}$	t_{WA}		0	—	—	ns
Acknowledge pulse width	$t_{W(ACK)}$	t_{AK}		300	—	—	ns
Strobe pulse width	$t_{W(STB)}$	t_{ST}		350	—	—	ns
Peripheral setup time before strobe	$t_{SU(PE-STB)}$	t_{PS}		0	—	—	ns
Peripheral hold time after strobe	$t_{H(STB-PE)}$	t_{PH}		150	—	—	ns
Read/write cycle time	$t_{C(RW)}$	t_{RV}		850	—	—	ns

● Switching Characteristics

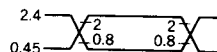
(Ta = -20 to 75°C, V_{DD} = 5V ± 10%, unless otherwise noted)

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Propagation time from read to data output	t _{PZX(R-DQ)}	t _{RD}	C _L = 150pF			170	ns
Propagation time from read to data floating *3	t _{PXZ(R-DQ)}	t _{DF}		10		100	ns
Propagation time from write to output	t _{PHL(W-PE)} t _{PLH(W-PE)}	t _{WB}				350	ns
Propagation time from strobe to IBF flag	t _{PLH(STB-IBF)}	t _{SIB}				300	ns
Propagation time from strobe to interrupt	t _{PLH(STB-INTR)}	t _{SIT}				300	ns
Propagation time from read to interrupt	t _{PHL(R-INTR)}	t _{RIT}				400	ns
Propagation time from read to IBF flag	t _{PHL(R-IBF)}	t _{RIB}				300	ns
Propagation time from write to interrupt	t _{PHL(W-INTR)}	t _{WIT}				450	ns
Propagation time from write to OBF flag	t _{PHL(W-OBF)}	t _{WOB}				650	ns
Propagation time from acknowledge to OBF flag	t _{PLH(ACK-OBF)}	t _{AOB}				350	ns
Propagation time from acknowledge to interrupt	t _{PLH(ACK-INTR)}	t _{AIT}				350	ns
Propagation time from acknowledge to data output	t _{PZX(ACK-PE)}	t _{AD}				300	ns
Propagation time from acknowledge to data floating *3	t _{PXZ(ACK-PE)}	t _{KD}		20		250	ns

*3 Test conditions are not applied.

*4 A.C Testing waveform

Input pulse level 0.45 to 2.4V
 Input pulse rise time 10ns
 Input pulse fall time 10ns
 Reference level input V_{IH} = 2V, V_{IL} = 0.8V
 Output V_{OH} = 2V, V_{OL} = 0.8V



■ FUNCTIONS

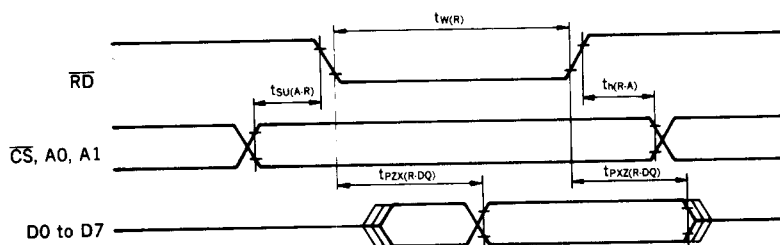
The SMC82C55AC-5 has programmable I/O pins that interface peripheral equipment to the CPU. The system software programs the functional configuration of the device.

The 24 programmable I/O pins may be individually configured in two groups of 12. Each group has three major modes of operation: 0, 1 and 2. In mode 0, each group of 12 I/O pins may be programmed in sets of four inputs or outputs. In mode 1, each group of 12 I/O pins may be grouped as one 8-bit I/O data port and one 4-bit control/status port. Mode 2 is used in Group A only, as one 8-bit bidirectional port and one 5-bit control/status port.

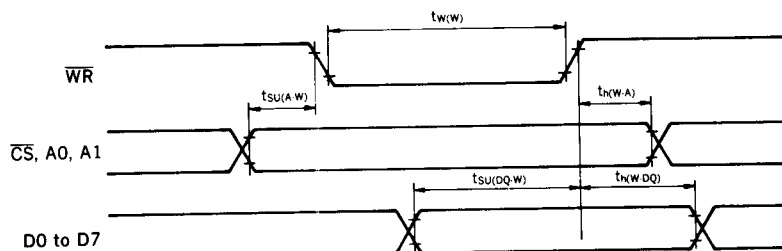
In mode 1 or 2, the control/status port bits can be set or reset by the CPU. A RESET pin is provided to clear all internal registers and set all ports to an input mode.

●Timing Chart

○Data bus read operation



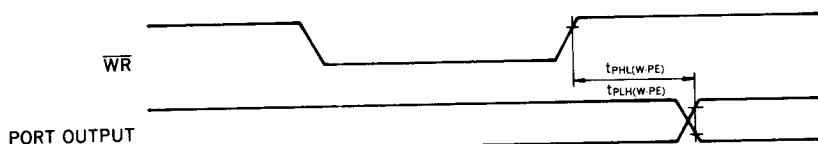
○Data bus write operation



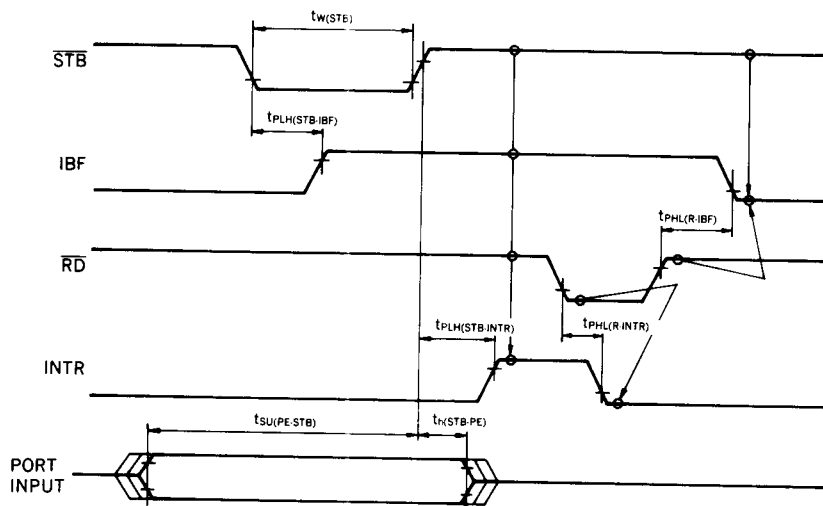
○Mode 0 Port input



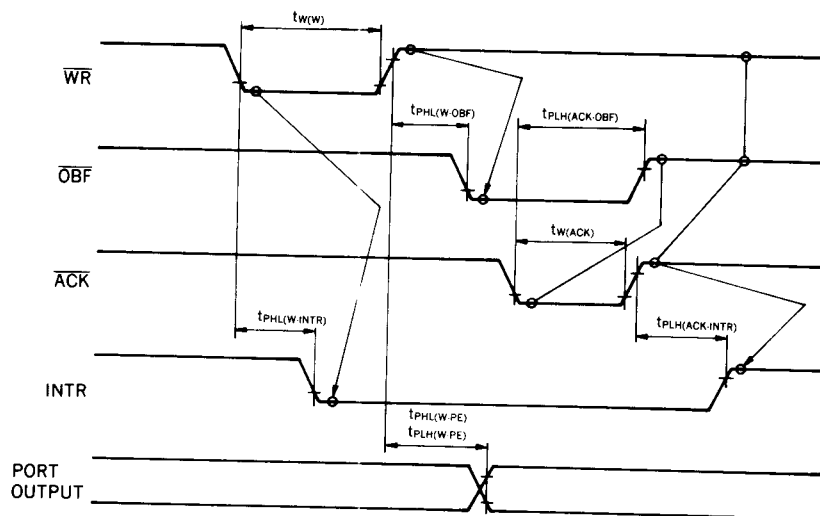
○Mode 0, 1 Port output



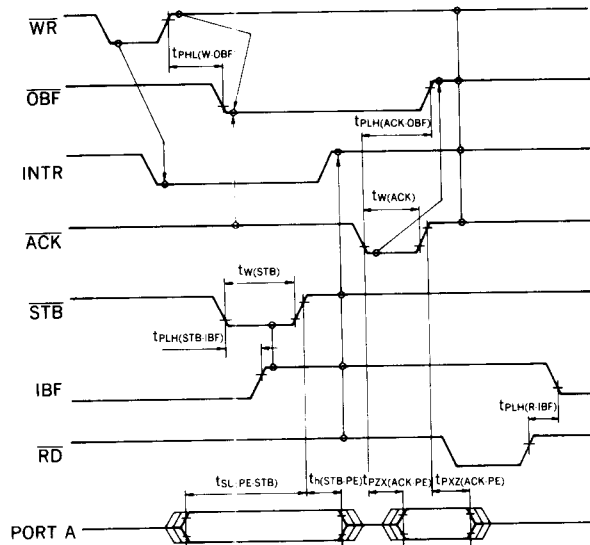
○ Mode 1 Strobed input



○ Mode 1 Strobed output



Mode 2 Bidirectional



$$*5 \text{ INTR} = \text{IBF} \cdot \text{MASK} \cdot \text{STB} \cdot \text{RD} + \text{OBF} \cdot \text{MASK} \cdot \text{ACK} \cdot \text{WR}$$

APPLICATION

The SMC 82C55AC-5 is used as a general purpose programmable I/O device designed to interface peripheral equipment to the 80XX series of microprocessors.

PACKAGE DIMENSIONS

