Siliconix

SMD15N06

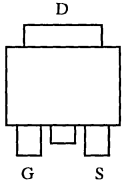
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

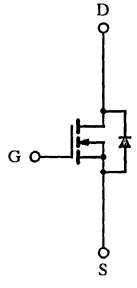
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
60	0.10	15

DPAK (TO-252)



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[b]	T_C = 25°C	I_D	15	A
	T_C = 100°C		7.5	
Pulsed Drain Current (maximum current limited by package)		I_{DM}	16	
Maximum Power Dissipation	T_C = 25°C	P_D	40	W
	T_A = 25°C		2.0[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction-to-Ambient Free Air[b]	R_{thJA}	60	°C/W
Junction-to-Case	R_{thJC}	3.0	

Notes:
a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
b. When mounted on 1" square PCB (FR-4 material).

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	15			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 7.5 A			0.10	Ω
		V_{GS} = 10 V, I_D = 7.5 A, T_J = 125°C			0.18	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 7.5 A	5.0			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		TBD		pF
Output Capacitance	C_{oss}			TBD		
Reverse Transfer Capacitance	C_{rss}			TBD		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 15 A		TBD	24	nC
Gate-Source Charge[c]	Q_{gs}			TBD	4.0	
Gate-Drain Charge[c]	Q_{gd}			TBD	8.0	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1.67 Ω I_D ≅ 15 A, V_{GEN} = 10 V, R_G = 25 Ω		TBD	30	ns
Rise Time[c]	t_r			TBD	85	
Turn-Off Delay Time[c]	$t_{d(off)}$			TBD	90	
Fall Time[c]	t_f			TBD	110	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S	T_C= 25°C			15	A
Pulsed Current	I_{SM}				16	
Forward Voltage[b]	V_{SD}	I_F = 3.3 A, V_{GS} = 0 V			2.2	V
Reverse Recovery Time	t_{rr}	I_F = 3.3 A, di/dt = 100 A/µs		TBD		ns
Reverse Recovery Charge	Q_{rr}			TBD		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.