

Preliminary



User's Manual (SMDK S5PV210 Rev0.0)

Development Kit

for S5PV210

Dec 02, 2009

REV 0.0

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S5PV210 RISC Microprocessor SMDK S5PV210 User's manual, Revision 0.0

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Revision History

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0.00	- Initial Release (SMDK S5PV210 Rev0.00)		AP development	Dec, 02, 2009



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1 INTRODUCTION

1.1 SYSTEM OVERVIEW

SMDK S5PV210 (S5PV210 Development Kit) is a platform for code development of SAMSUNG's S5PV210 16/32-bit RISC microcontroller (ARM-CORTEX A8). S5PV210 is used in hand-held devices and general applications.

The S5PV210 is a 32-bit RISC cost-effective, low power, high performance microprocessor solution for mobile phones and general applications, and integrates an ARM Cortex-A8 which implements the ARM architecture V7-A with supporting numerous peripherals.

To provide optimized Hardware (H/W) performance for the 3G and 3.5G communication services, S5PV210 adopts 64-bit internal bus architecture and includes many powerful hardware accelerators for tasks such as motion video processing, display control and scaling. Integrated Multi Format Codec (MFC) supports encoding and decoding of MPEG-1/2/4, H.263, H.264 and decoding of VC1, Divx. This Hardware accelerators support realtime video conferencing and Analog TV out, HDMI for NTSC and PAL mode

The S5PV210 has an optimized interface to external memory capable of sustaining the demanding memory bandwidths required in high-end communication services. The memory system has Flash/ ROM external memory ports for parallel access and DRAM port for high bandwidth. DRAM port can be configured to support LPDDR1(=mobile DDR), DDR2 or LPDDR2.

Flash/ROM Port supports NAND Flash, NOR-Flash, OneNAND, SRAM and ROM type external memory.

To reduce total system cost and enhance overall functionality, S5PV210 includes many hardware peripherals such as TFT 24-bit true color LCD controller, Camera Interface, MIPI DSI, CSI-2, System Manager for power management, ATA I/F, 4 UART, 24-channel DMA, 4 Timers, General I/O Ports, 3 IIS, S/PDIF, 3 IIC-BUS interface, 3 HS-SPI, USB Host 2.0, USB OTG 2.0 operating at high speed (480Mbps), 4 SD Host & High Speed Multi-Media Card Interface and 4 PLLs for clock generation.

Package on Package (POP) option with MCP is available for small form factor applications.

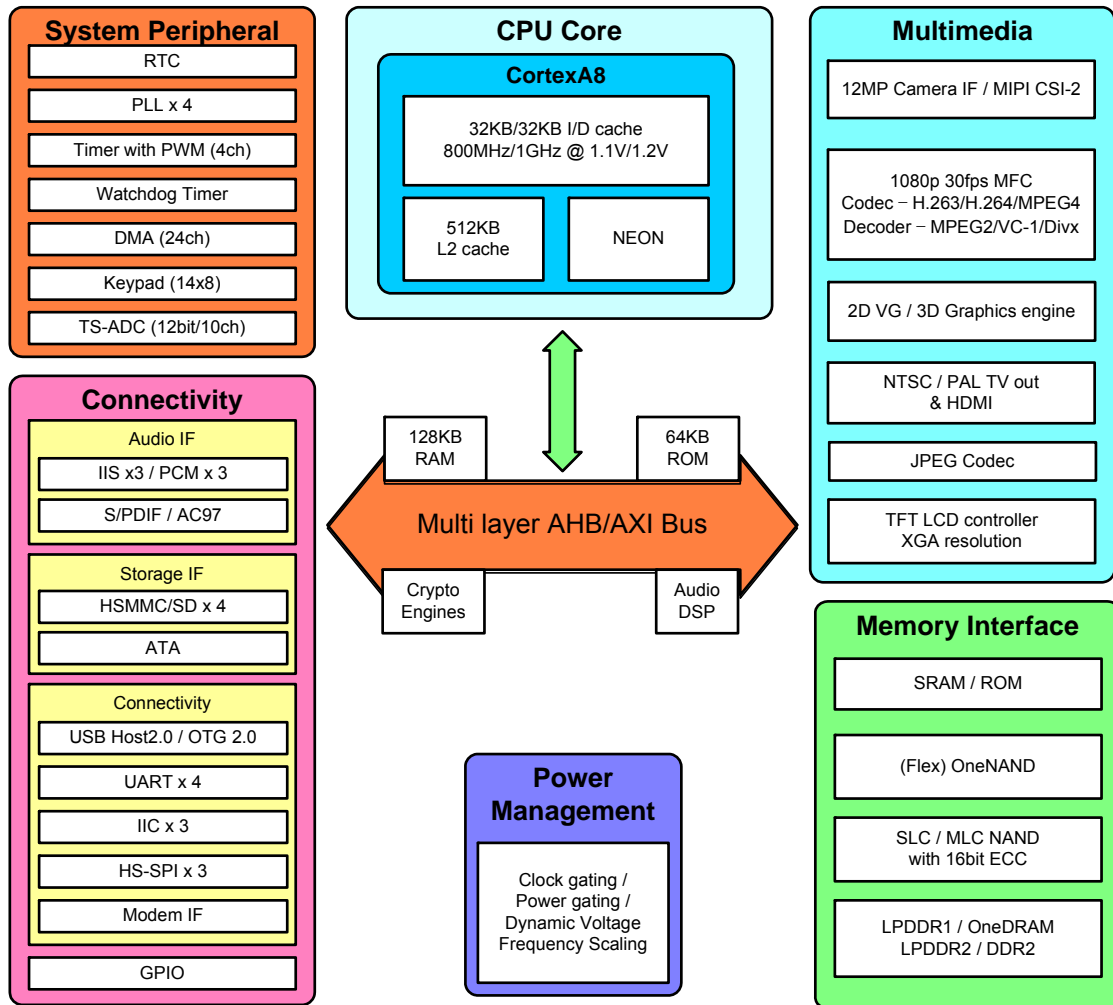


Figure 1 S5PV210 Functional Block Diagram

1.2 SMDK S5PV210 FEATURES

The SMDK S5PV210 (S5PV210 Development Kit) highlights the basic system-based hardware design which uses the S5PV210. It can evaluate the basic operations of the S5PV210 and assist in developing codes.

The features of SMDK S5PV210 include:

- Microcontroller : S5PV210 (16/32 bit RISC microcontroller, **ARM-CORTEX A8**)
- External memory
 - . AMD 8Mbit NOR Flash (Socket 1EA)
 - . SAMSUNG NAND Flash (Socket 1EA)
 - . SAMSUNG OneNAND (External Board, Optional)
 - . SAMSUNG 16Mbit SRAM 1EA
 - . Dram port 0 : SAMSUNG 4 x 1Gb DDR2 SDRAM(x8)
 - . Dram port 1 : SAMSUNG 4 x 1Gb DDR2 SDRAM(x8) or SAMSUNG 4 x 2Gb DDR2 SDRAM(x8)
- TFT LCD & Touch panel interface (External Board, default: 4.8" WVGA LMS480KF02)
- ATA interface (2 CF card sockets)
- SD/SDIO/MMC interface (3 SD Sockets)
- Digital Video & Audio : **HDMI 1.3 Video(720p) & S/PDIF 5.1 Channel Audio I/F**
- TV Out interface (**Composite**)
- USB Host , USB OTG 2.0 interface
- High Speed SPI interface
- IIS/AC97/PCM Interface : WM9713, WM8580 Audio CODEC on board
- General Camera Interface : 2 port
- MIPI Camera Interface : **MIPI-CS12** (1Gbps/Lane Serial Communication)
- High Speed Serial MIPI Interface LCD : **MIPI-DSI** (1Gbps/Lane Serial Communication)
- Keypad interface
- Ethernet Interface : DM9000(10/100Mbps Ethernet controller) on board
- 2 port UART interface
- JTAG port
- Module Connector (M1 ~ M4)
 - . M1 (Module1): For GPS Daughter Board (UART, SPI) : Samsung GPD14B01 (SiRFSTAR III GSD3) (Optional)
 - . M2 (Module2): For Mobile TV Daughter Board (SPI, IIC) or HD Radio (SPI, IIS)
 - Mobile TV: Samsung S5P4F31 (TBD, Optional)
 - HD Radio: SiPORT SD1010 (TBD, Optional) , Samsung (TBD, Optional)
 - . M3 (Module3): For Bluetooth Daughter Board (UART, PCM for PMIC Audio Codec)
 - . M4 (Module4): For Audio Daughter Board (AC97, IIS, IIC)



2 SMDK S5PV210 REAL VIEW

2.1 SMDK S5PV210 CPU BOARD REAL VIEW

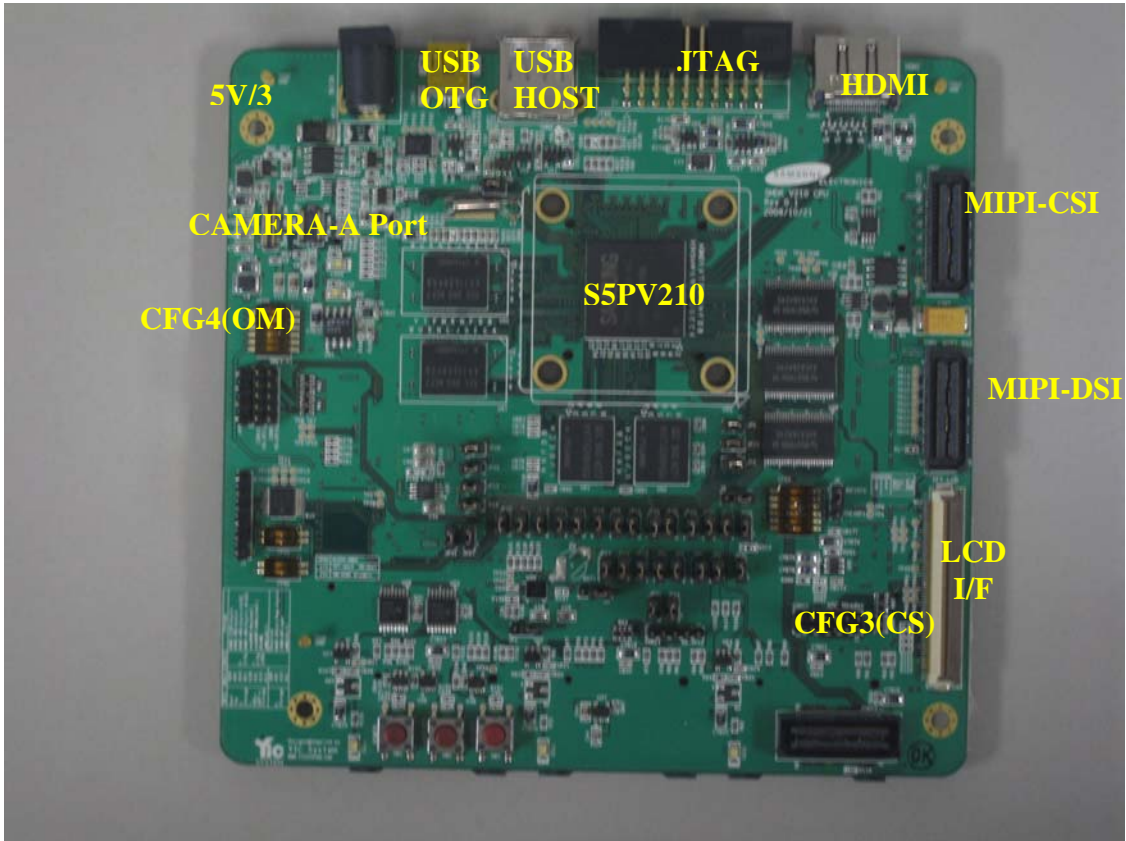


Figure 2 S5PV210 CPU BOARD TOP VIEW

External
OneNAND

POWER RESET

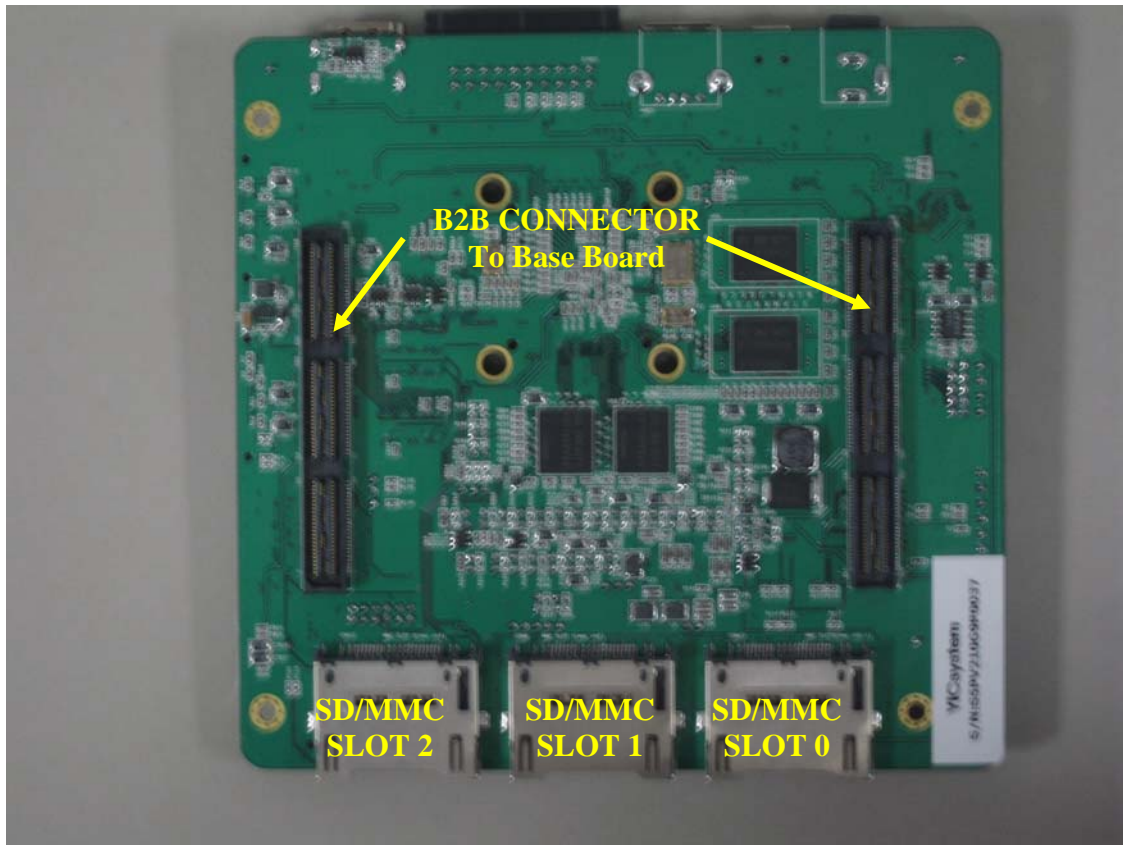


Figure 3 S5PV210 CPU BOARD BOTTOM VIEW

2.2 SMDK S5PV210 BASE BOARD REAL VIEW

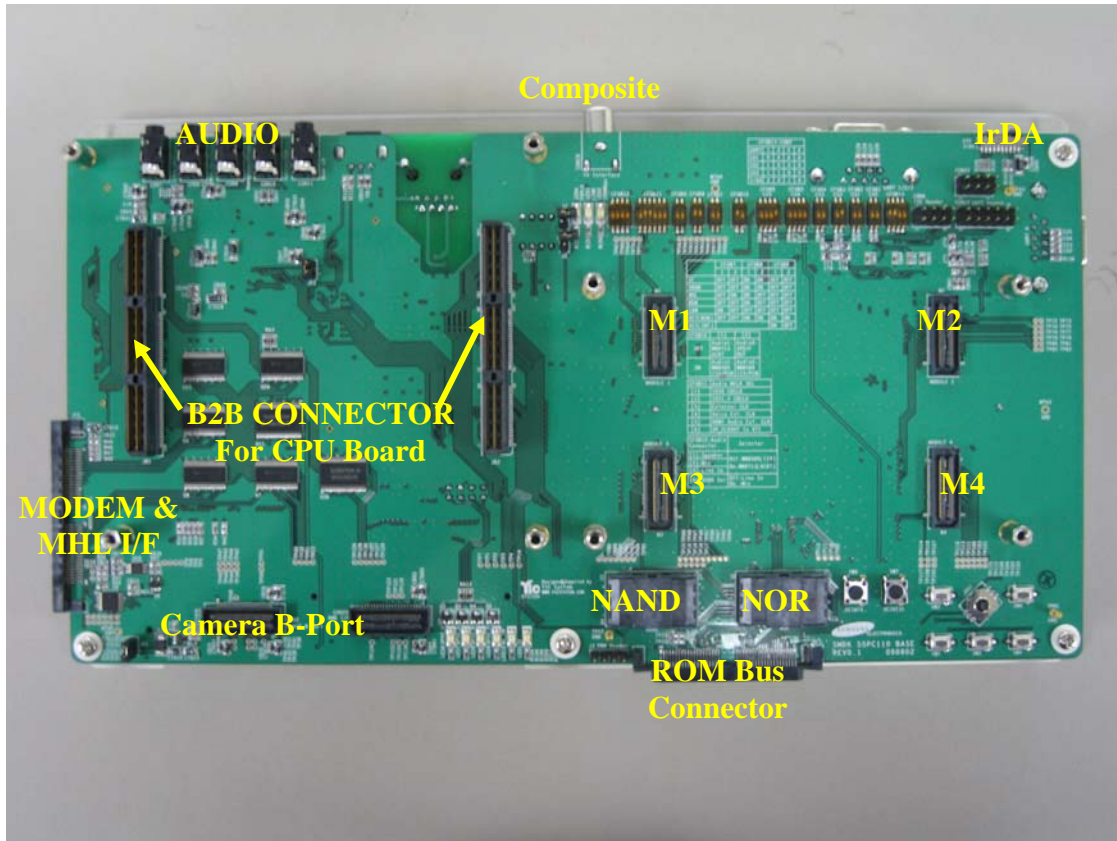


Figure 4 S5PV210 BASE BOARD TOP VIEW

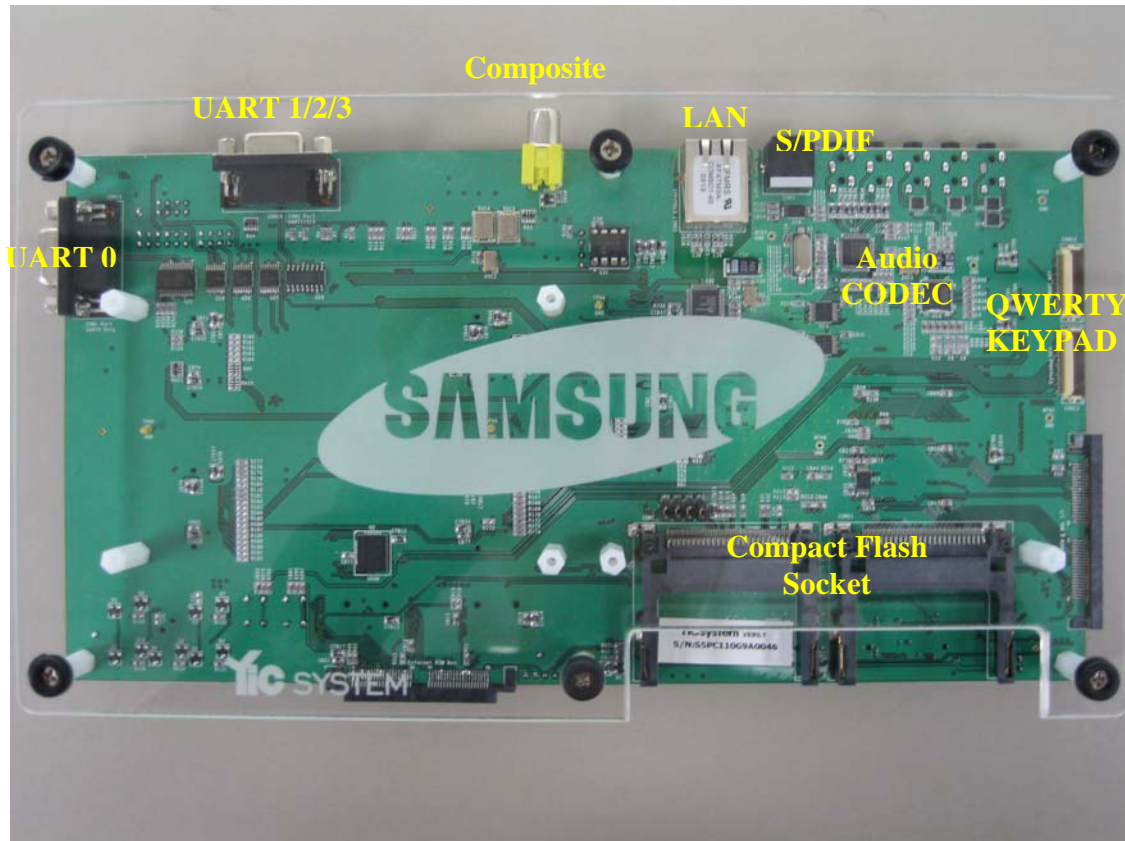


Figure 5 S5PV210 BASE BOARD BOTTOM VIEW

2.3 SMDK S5PV210 LCD BOARD REAL VIEW

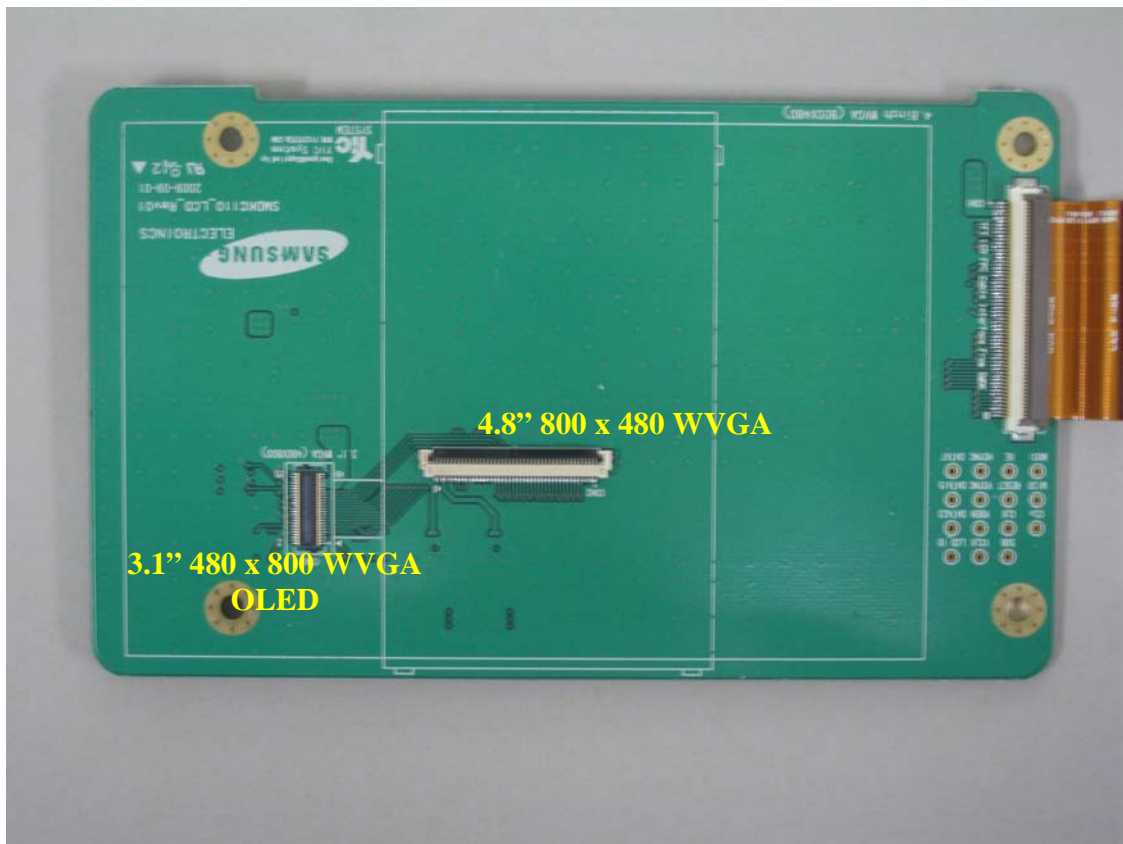


Figure 6 S5PV210 LCD BOARD TOP VIEW

3 CIRCUIT DESCRIPTION

The SMDK S5PV210 is designed to test S5PV210 and develop software while hardware is being developed. Figure 10 highlights the SMDK S5PV210's block diagram.

3.1 POWER DISTRIBUTION TREE

SMDK S5PV210 is operated by 1.1V for Internal, 1.8V for Memory and 3.3V for Input/Output pad and several peripherals. SMDK S5PV210 is supplied by 5V/3A DC Adaptor Power. The SMDK S5PV210 has distributed power plane, with power going separately to the MCU and the main power plane.

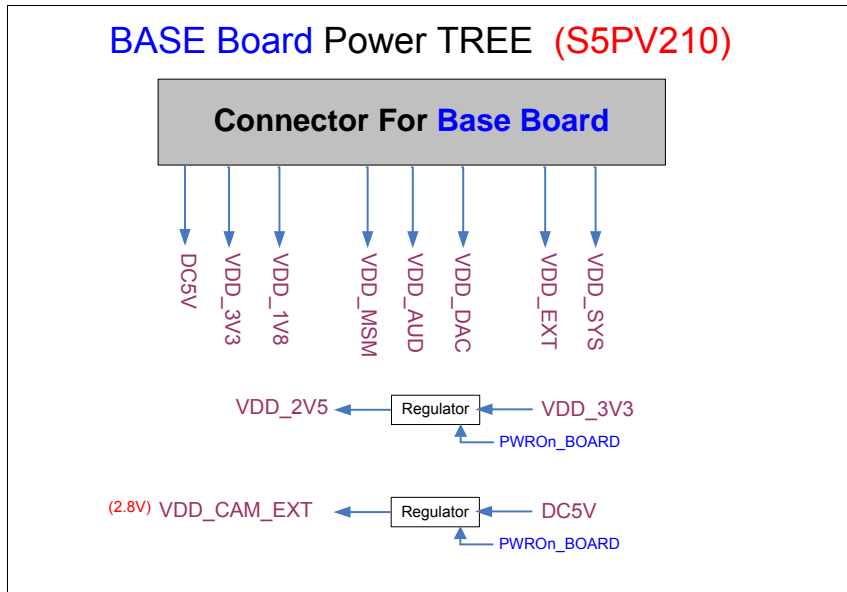


Figure 7 S5PV210 BASE BOARD POWER DISTRIBUTION TREE

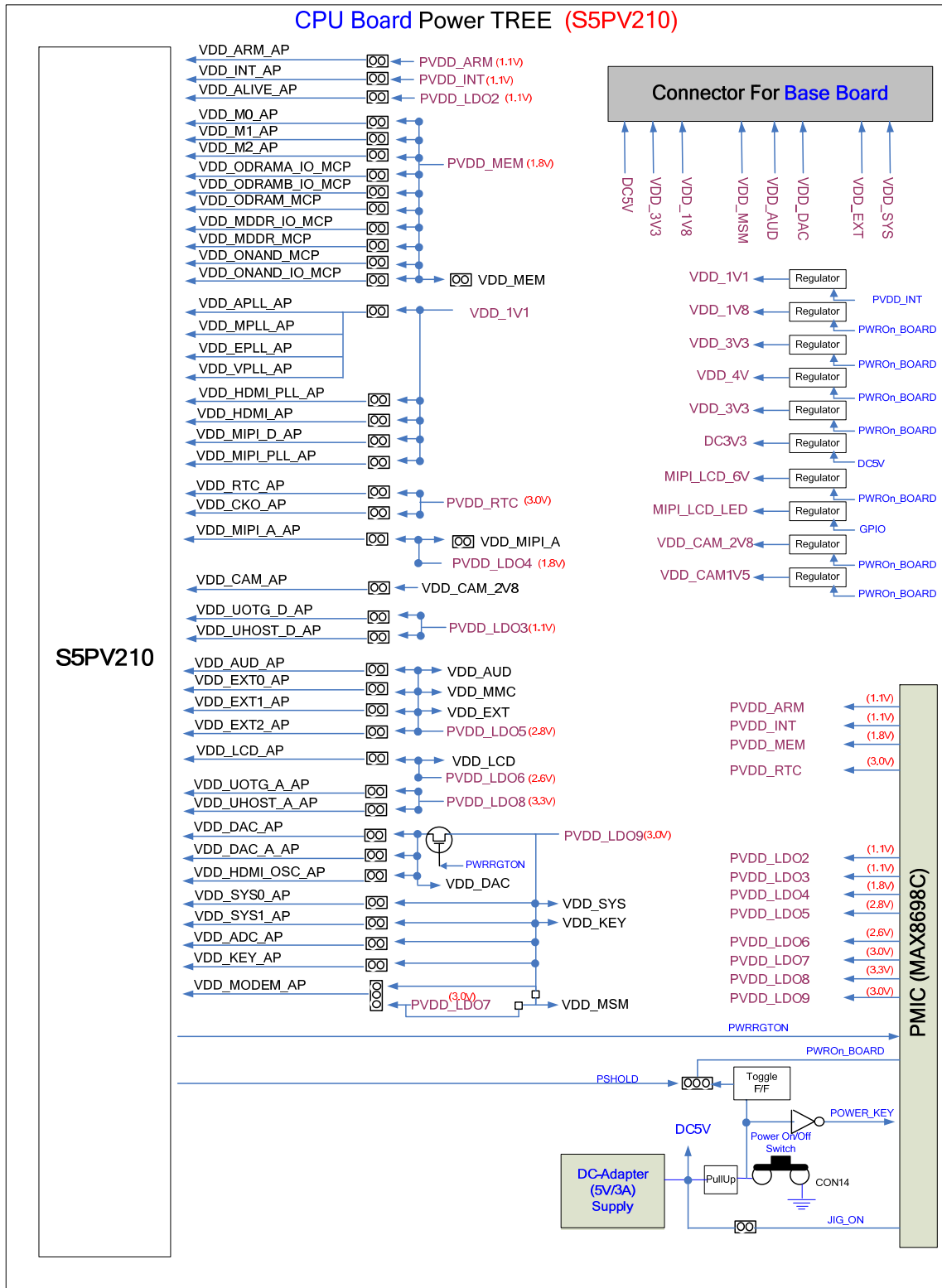


Figure 8 S5PV210 CPU BOARD POWER DISTRIBUTION TREE

3.2 FUNCTIONAL BLOCK DIAGRAM

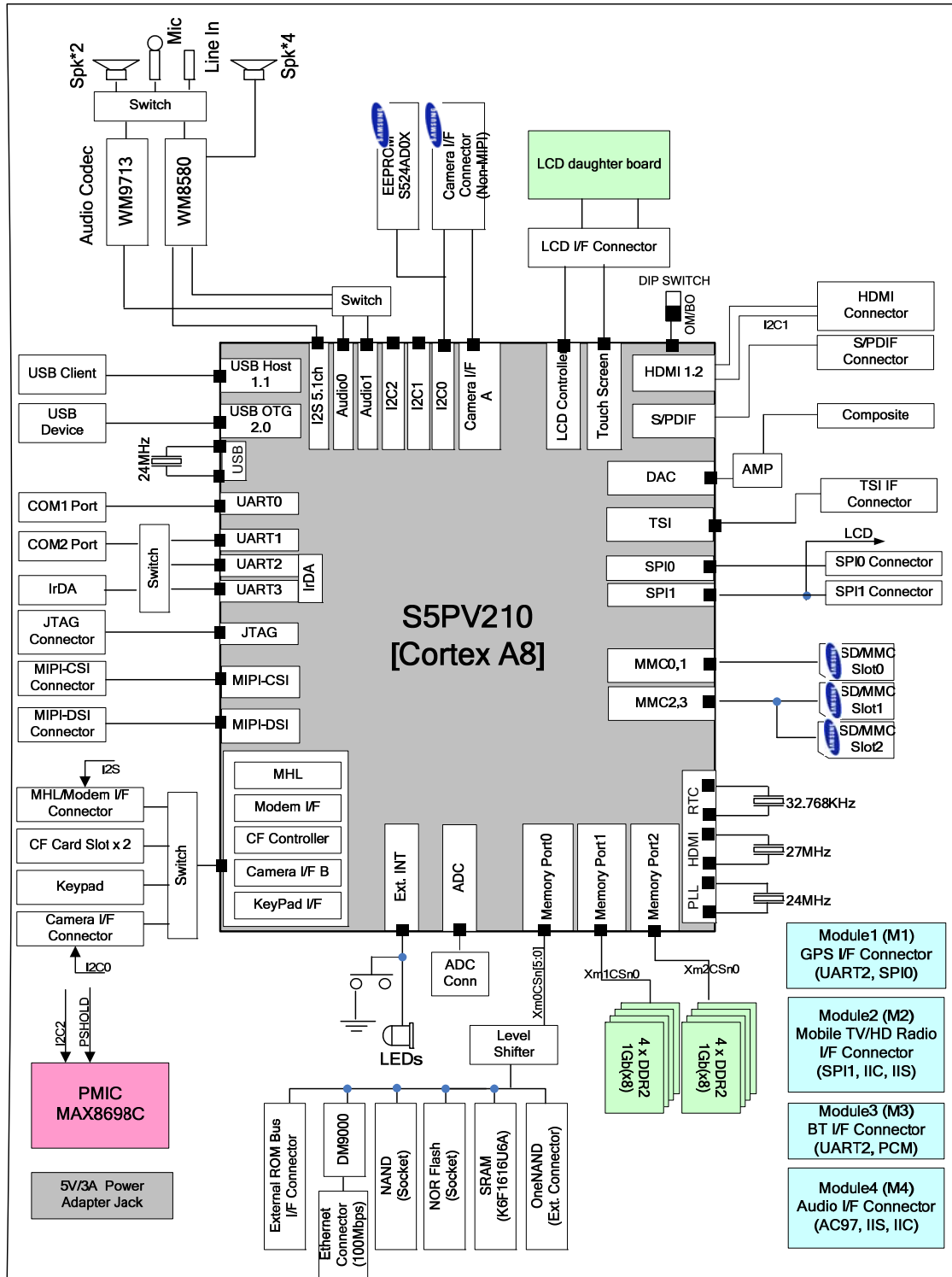


Figure 9 S5PV210 SMDK FUNCTIONAL BLOCK DIAGRAM

4 SMDK S5PV210 SYSTEM CONFIGURATIONS

Perform the following steps to use SMDK S5PV210 board.

- **CFG** is on CPU board and **CFGB** is on Base board.
- Configuration value meaning - **X**: don't care, **1**: ON **0**: OFF

Configuration Switch (DIP Switch)



Off(Switch Open) → On (Switch Short)

1. Select the Clock source(CFG4)

Please refer to 'PLL CLOCK SOURCE SELECTION'

2. Select the Boot Device(storage) and set Boot Mode configuration switches (CFG4)

Please refer to 'BOOT MODE SELECTION'

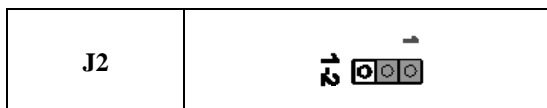
3. Set the CFG switch or Jumper for each booting device.

External OneNAND

- Check If OneNAND daughter card is connected on **CON14**(on CPU board).
- Set CFG3[6:1] to X0X010. (Xm0CSn4)

CFG3					
CS5			CS4		
[6]	[5]	[4]	[3]	[2]	[1]
X	OFF	X	OFF	ON	OFF

- Set J2(on CPU board) to 1-2 SHORT.



SD/MMC or eMMC

- Insert a Card to **HS-MMC slot0** (CON13 on CPU board).

- Set CFG2[2:1] to X0. (to use SDMMC channel 0 of S5PV210)

CFG2	Description
[1]	OFF

NAND Flash

- Insert a NAND Flash to **NAND socket** (U4 on Baseboard).
- Set CFGB3[2:1] to 10. (Xm0CSn2)

CFGB3	
[2]	[1]
ON	OFF

NOR Flash

- Insert a NOR Flash to **NOR socket** (U3 on Baseboard).
- Set CFGB1[2:1] to 01. (Xm0CSn0)

CFGB1	
[2]	[1]
OFF	ON

- Set CFGB7[2:1] to 00 and CFGB8[2:1] to 11 and CFGB9[2:1] to 00. (to use SROM Addr [16:22])

CFGB7	
[2]	[1]
OFF	OFF

CFGB8	
[2]	[1]
ON	ON



CFGB9	
[2]	[1]
OFF	OFF

4. Set CFGB13 for debugging message channel .

UART ch2 is for default debugging message channel and booting channel.(ch3 in case of EVT0)

- Connect to UART cable to **COM2**(CON15 on Base board)
- Set CFGB13[4:1] to 0001

CFGB13	[4]	[3]	[2]	[1]
UART2	OFF	OFF	OFF	ON

5. Check default Jumper setting.

<CPU Board>

- JP1~40 Short
- J4 1-2 short
- J5 1-2 short
- J8 2-3 short
- JP41 Open

<BASE Board>

- JP1 Short
- J1,J2 Open

6. Connect 5V power adapter and push the power button.

7. Check the Power LED if it is operating normally.

Refer to LED description section.

4.1 PLL CLOCK SOURCE SELECTION

Main input clock for the S5PV210 system can be selected by setting the XOM[0] values.

Description	CFG4[1] , (XOM[0])
24MHz X-tal Clock (XXTI)	OFF
24MHz X-tal Clock (XusbXTI)	ON (default)

4.2 BOOT MODE SELECTION

4.2.1 Switch Configuration

Description		CFG4[6:2]						
CFG4[6]	CFG4[5:2]	CFG4[6]	CFG4[5]	CFG4[4]	CFG4[3]	CFG4[2]		
I-ROM Booting sequence: Storage	eSSD	OFF	OFF	OFF	OFF	OFF	OFF	
	Nand 2KB, 5cycle (Nand 8bit ECC)					ON		
	Nand 4KB, 5cycle (Nand 8bit ECC)				OFF	OFF		
	Nand 4KB, 5cycle (Nand 16bit ECC)				ON	ON		
	OnenandMux				OFF	OFF		
	OnenandDemux				ON	ON		
	SD/MMC				ON	OFF		
	eMMC(4-bit)				ON	ON		
	Reserved				ON	ON		
	Nand 2KB, 4cycle (Nand 8bit ECC)				ON	OFF	OFF	ON
	NOR boot				ON	ON	OFF	OFF
	eMMC(8-bit)				ON	ON		
I-ROM	eSSD	ON	OFF	OFF	OFF	OFF		
Booting sequence:	Nand 2KB, 5cycle					ON		



UART						
->USB						
->Storage	Nand 4KB, 5cycle				ON	OFF
	Nand 4KB, 5cycle (Nand 16bit ECC)				ON	ON
	OnenandMux(Audi)				OFF	OFF
	OnenandDemux(Audi)				ON	ON
	SD/MMC			ON	ON	OFF
	eMMC(4-bit)				ON	ON

Note) If CFG4[6] is set to 1, It is used for debug mode that UART boot is first and USB boot is second. UART boot has some kind of error case. In case of UART error, the iROM boot sequence moves to USB boot. USB boot also has some kind of error case like UART. If USB boot is fail, boot sequence move to main storage boot.
Please refer to iROM application note which is more detail about error case.

4.3 CONFIGURATION SWITCH DESCRIPTION IN CPU BOARD

4.3.1 CFG3: SELECTION FOR CS#4,#5

Description	CFG3					
	CS5			CS4		
	[6]	[5]	[4]	[3]	[2]	[1]
ON		External OneNand	Connect to Base CS#5		External OneNand	Connect to Base CS#4

4.3.2 J2: SELECTION for Interrupt of Ext. OneNAND

J2	Description
1-2 short	Connect to ONDXL_INT0
2-3 short	Connect to ONDXL_INT1(default)



4.3.3 CFG2: Configuration of MMC slot 0

<i>CFG2</i>	<i>Description</i>
[1]	ON : MMC port 1 4bit Data Width OFF : MMC port 0 8bit Data Width (default)
[2]	ON : HDMI I2C Buffer Disable OFF : HDMI I2C Buffer Enable

4.3.4 CFG1: TSI I/F

<i>CFG3</i>	<i>Description</i>
[1]	ON : TSI I/F Buffer Enable OFF : TSI I/F Buffer Disable
[2]	ON : TSI RX OFF : TSI TX

4.3.5 J3: PSHOLD selection

<i>J3</i>	<i>Description</i>
1-2 short	Not using PSHOLD
2-3 short	Using PSHOLD. PSHOLD should be programmed Output-HIGH during pressing the power button .

4.3.6 JP1: JIG ON selection

JIG ON is used to turn on board without pressing power button.

<i>JP1</i>	<i>Description</i>
short	Turn on system power always.
open	Turn on system power by pressing power button.





ELECTRONICS

4.4 CONFIGURATION SWITCH DESCRIPTION IN BASE BOARD

4.4.1 CFGB1: SROM BANK0 CHIP SELECTOR

CFGB1 component is used to select devices as SROM BUS I/F 0(B_Xm0CSn0).

<i>Description</i>	CFGB1	
	[2]	[1]
NOR (AMD) Flash	OFF	ON
SRAM	ON	OFF

4.4.2 CFGB2: SROM BANK1 CHIP SELECTOR

CFGB2 component is used to select devices as SROM BUS I/F 1(B_Xm0CSn1).

<i>Description</i>	CFGB2	
	[2]	[1]
NOR (AMD) Flash	OFF	ON
SRAM	ON	OFF

4.4.3 CFGB3: SROM BANK2 CHIP SELECTOR

CFGB3 component is used to select devices as SROM BUS I/F 2(B_Xm0CSn2/NFCSn0).

<i>Description</i>	CFGB3	
	[2]	[1]
SRAM	OFF	ON
Nand CS 0	ON	OFF

4.4.4 CFGB4: SROM BANK3 CHIP SELECTOR

CFGB4 component is used to select devices as SROM BUS I/F 3(B_Xm0CSn3/NFCSn1).

<i>Description</i>	CFGB4	
	[2]	[1]
SRAM	OFF	ON

Nand CS 1	ON	OFF
-----------	----	-----

4.4.5 CFGB5: SROM BANK4 CHIP SELECTOR

CFGB5 component is used to select devices as SROM BUS I/F 4(B_Xm0CSn4/NFCSn2).

<i>Description</i>	CFGB5			
	[4]	[3]	[2]	[1]
SRAM	OFF	OFF	OFF	ON
NAND CS 2	OFF	OFF	ON	OFF
External Rom Bus Connector	OFF	ON	OFF	OFF
Ethernet	ON	OFF	OFF	OFF

4.4.6 CFGB6: SROM BANK5 CHIP SELECTOR

CFGB6 component is used to select devices as SROM BUS I/F 5(B_Xm0CSn5/NFCSn3).

<i>Description</i>	CFGB6			
	[4]	[3]	[2]	[1]
SRAM	OFF	OFF	OFF	ON
NAND CS 3	OFF	OFF	ON	OFF
External Rom Bus Connector	OFF	ON	OFF	OFF
Ethernet	ON	OFF	OFF	OFF

4.4.7 CF,MODEM,CAM_B,KEY,MHL,SROM ADDR SWITCHING

CFGB7,8,9 component is used to switching Xmsm signals which are muxed following signals.

(CF Card I/F, Modem I/F, Camera B I/F, Keypad I/F, MHL I/F, SROM Addr[16:22])

<i>Description</i>	CFGB7	CFGB8	CFGB9
--------------------	--------------	--------------	--------------



	[1]	[2]	[1]	[2]	[1]	[2]
CF Card	OFF	OFF	ON	ON	ON/OFF	OFF
SROM Addr [22:16]	OFF	OFF	ON	ON	ON/OFF	OFF
MHL I/F	OFF	ON	ON	OFF	ON/OFF	OFF
MODEM I/F	OFF	OFF	ON	OFF	ON/OFF	OFF
Camera B port	ON	OFF	OFF	OFF	ON/OFF	OFF
Keypad muxed with Xmsm signals	OFF	OFF	ON	ON	ON	ON
Keypad muxed with XEINT signals					ON	OFF

4.4.8 CFGB10: Audio Port

CFGB10 component is used to select devices as Audio I/F 1,2.

<i>Description</i>	Audio2	Audio1
	[2]	[1]
OFF	SPDIF Out	AC97(WM9713)
ON	IIS/PCM(WM8580)	IIS/PCM(WM8580)

4.4.9 CFGB11: Audio Codec(WM8580) Master clock selection

<i>CFGB11</i>	<i>Mater Clock source</i>
[1]	I2S0 CDCLK
[2]	I2S1,2 CDCLK
[3]	External CLK
[4]	External Voice CLK
[5]	External HDMI Audio CLK
[6]	AP CLKOUT

4.4.10 CFGB12: Audio Device Input/Output Connection

<i>CFGB12</i>	<i>Description</i>
[1] : Speaker	OFF: IIS (WM8580) ON: AC97 (WM9713)
[2] : MIC	
[3] : Line In	
[4] : WM8580	OFF: Line In ON: MIC

4.4.11 CFGB13: UART/IrDA Connection

CFGB13 component is used to select COM2(CON15) Port connection.

CFGB13	[1]	[2]	[3]	[4]
UART1	OFF	X	X	X
UART2	ON	OFF	X	X
UART3	ON	ON	OFF	X
IrDA	X	X	ON	X

4.5 LED & SWITCH Description

4.5.1 LED description

<CPU Board>

1. LED4: 5V Power(adapter) Status
2. LED5: System power(from PMIC) Status



3. LED3: Card Insertion status of MMC slot 0
4. LED1: Card Insertion status of MMC slot 1
5. LED2: Card Insertion status of MMC slot 2

<Base Board>

6. LED1: CF card Power status
7. LED2,3,4: Ethernet status
8. LED6: For debugging (GPH2_4)
9. LED7: For debugging (GPH2_5)
10. LED8: For debugging (GPH2_6)
11. LED9: For debugging (GPH2_7)
12. LED10: 5V Power(adapter) Status

4.5.2 Switch description

<CPU Board>

1. SW2 : Warm reset switch
2. SW3: System reset switch
3. SW1: Power On switch

<Base Board>

4. SW6 : For EINT test (XEINT4)
5. SW7 : For EINT test (XEINT31)

5 SMDK Daughter Board

Each Daughter board can be connected on SMDK connector.

5.1 External OneNAND

External OneNAND can be mounted on **CON14**.

5.1.1 Real view



Figure 10 External OneNAND

5.1.2 Schematic



EXTERNAL_ONE
NAND.pdf

5.2 CSI Daughter Board

CSI Daughter Board can be mounted on **CON2**.

5.2.1 Real view

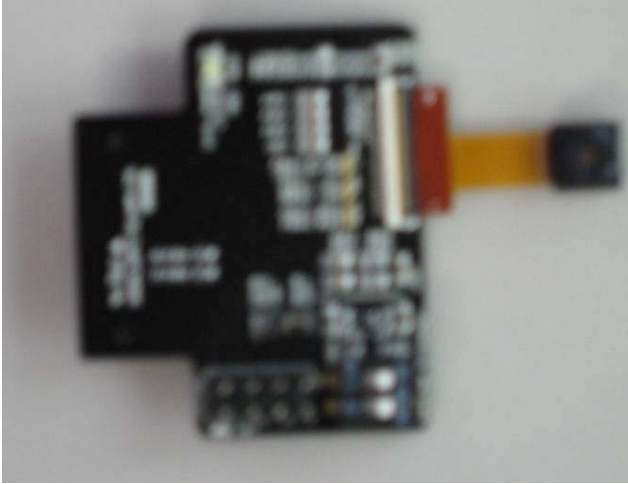


Figure 11 CSI Daughter Board

5.2.2 Schematic



CSI_daughter_BO
ARD.pdf

5.3 DSI Daughter Board

DSI Daughter Board can be mounted on **CON1**.

5.3.1 Real view

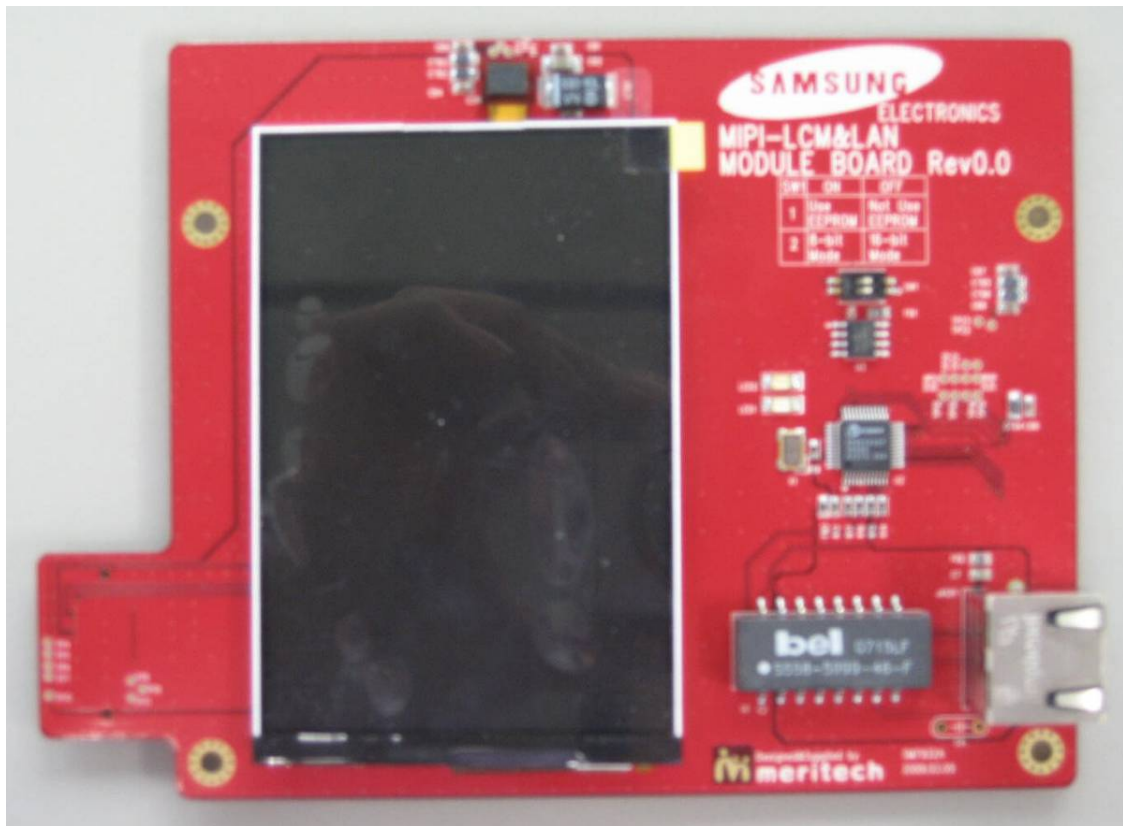


Figure 12 DSI Daughter Board

5.3.2 Schematic


MIPI-LCM&LAN_
BD_SCHEMATIC_f

6 SMDK SCHEMATIC REVISION HISTORY

This document contains information of corrected points on the schematic of SMDK S5PV210.

Boards	Page	Contents	Corrected points (ECN)
CPU Board			
Base Board			
LCD Board			

7 SMDK SCHEMATIC

There are 3 parts of SMDK Schematic.

1. CPU & Base Board Rev0.1
2. LCD Board Rev0.1



SMDKV210_CPU_
REV0_1.pdf



SMDKV210_BASE
_BD_SCH_REV01.r



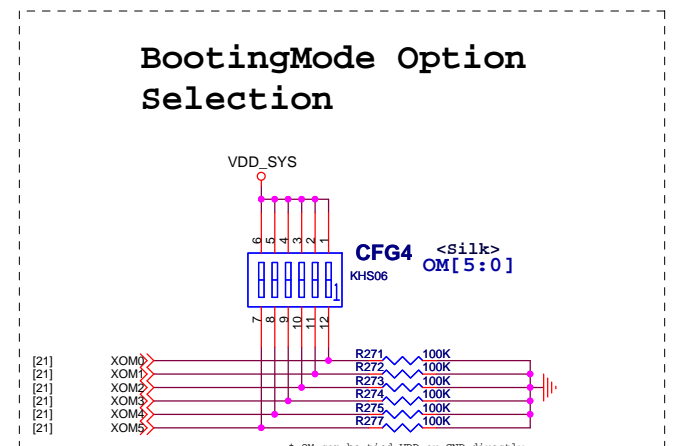
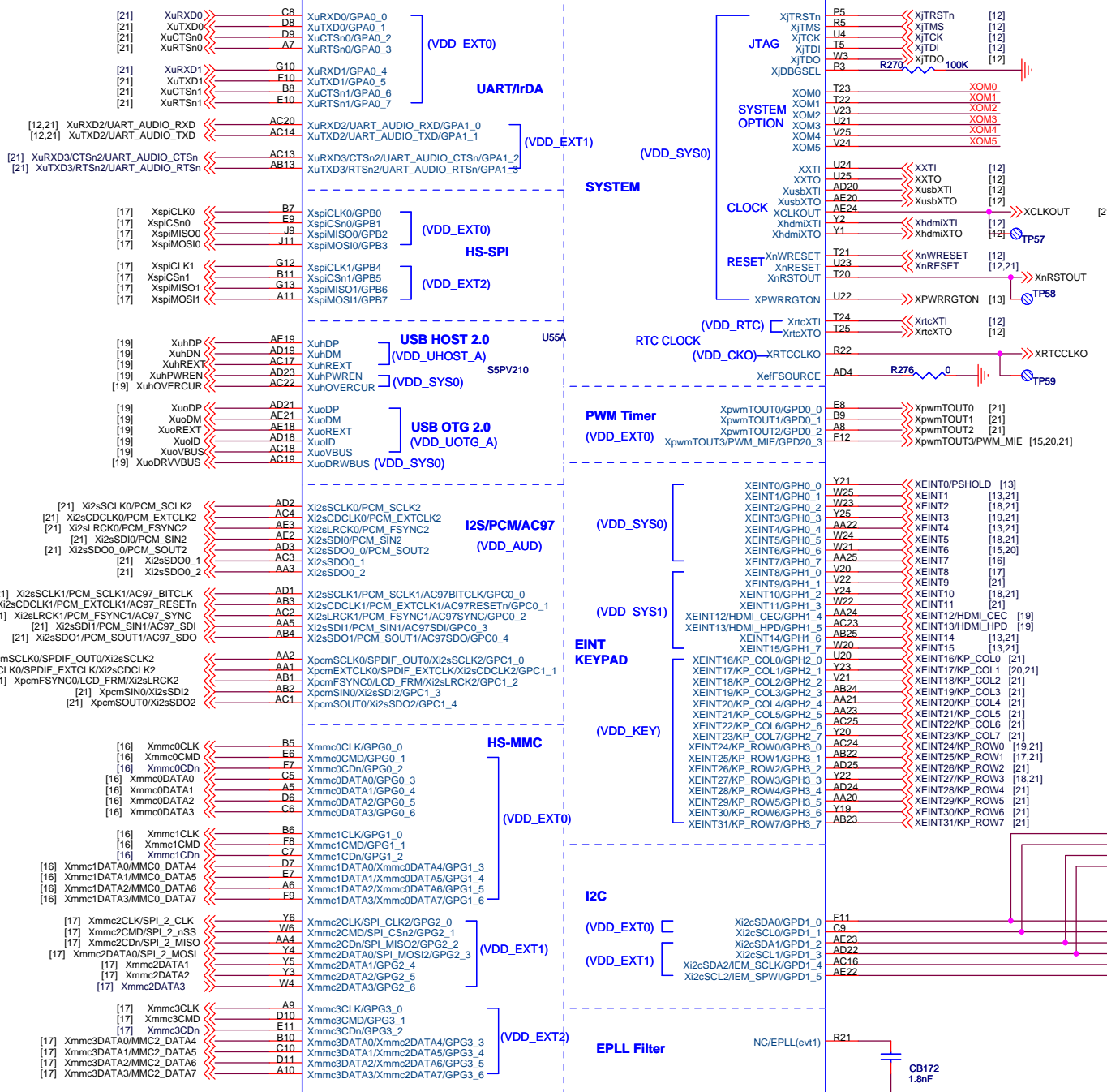
S5PV210_SMDK_L
CD_SCHEMATIC_'



SMDK_S5PV210_CPU B'd (S5PV210 Evaluation Board) Schematics

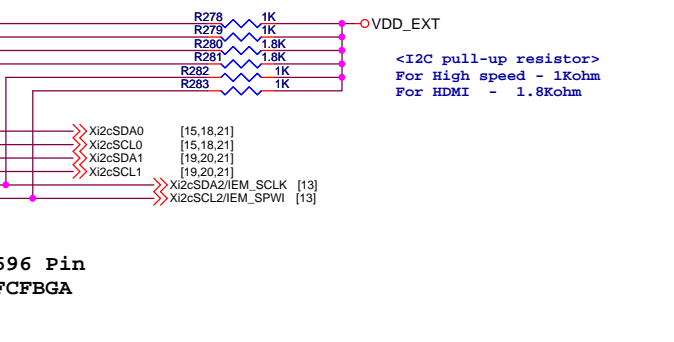
Revision	Date	Description
Rev 0.0	2009. 09	Preliminary Version

Table of Contents		Part Reference
Page	Function	<Component><Number>
01	Revision History	U : Component or Regurator IC
02	S5PV210 (SYS&Connectivity)/ Boot Option	C : Capacitor
03	S5PV210 (MCP & SROM Memory)	CB : Capacitor Bypass
04	S5PV210 (Media)	CT : Capacitor Tantal
05	S5PV210 (Gen_Power)	CTB : Capacitor Tantal Bypass
06	XM1 DDR2(1Gbit *2) #0,1	J : Jumper
07	XM1 DDR2(1Gbit *2) #2,3	JB : CPU To Base connector
08	XM2 DDR2(1Gbit *2) #0,1	JP : Jumper Power
09	XM1 DDR2(1Gbit *2) #2,3	R : Resistor
10	Power Jumper shunt	RA : Resistor Array
11	Power (DC jack & Regulator)	RP : Resistor Power
12	Reset/ Clock Source/ JTAG	VR : Variable Resistor
13	Power (PMIC)	L : Inductor
14	Memory (SROM EBI IF)	FB : Ferrite Bead
15	OneNAND / LCD I/F(NonMIPI)	OSC : Oscillator
16	MMC #0	X : X-tal (Crystal)
17	MMC #1/#2/ HS-SPI	Q : Transistor or FET
18	Camera A-Port I/F	D : Diode
19	HDMI/ MIPI-CSI/ MIPI-HSI/ USB	ZD : Zener Diode
20	MIPI-DSI	LED : LED Diode
21	B2B Connector(CPU)	SW : SWitch Tact/Push
		CON : CONnector
		CFG : ConFiGure switch (DIP/Slide)
		TP : Test Point (SMD)
		TPH : Test Point Hole (Through Hole)
		MTH: Mount Through Hole
		MOD : MODule Interface connector

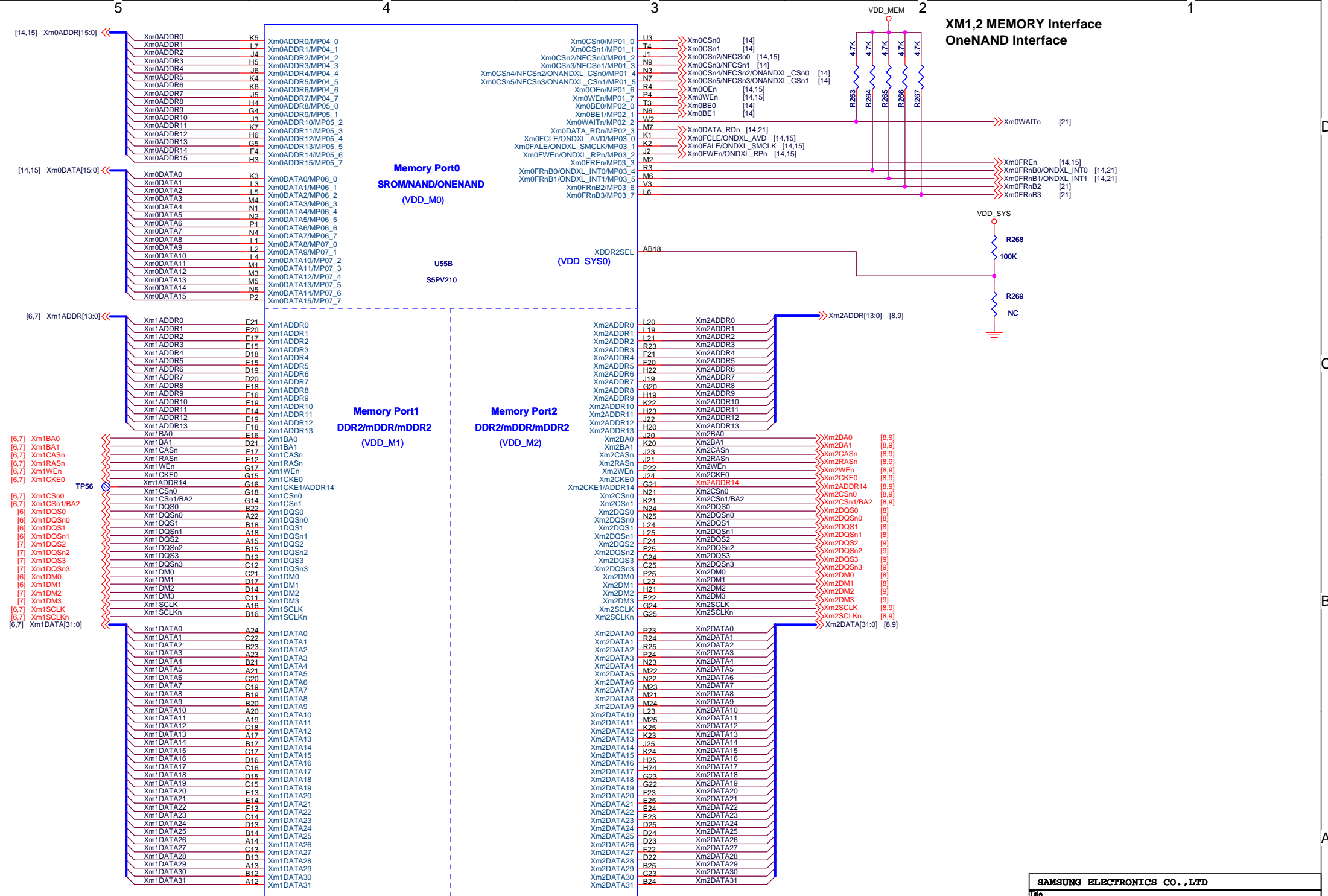


<Silk>

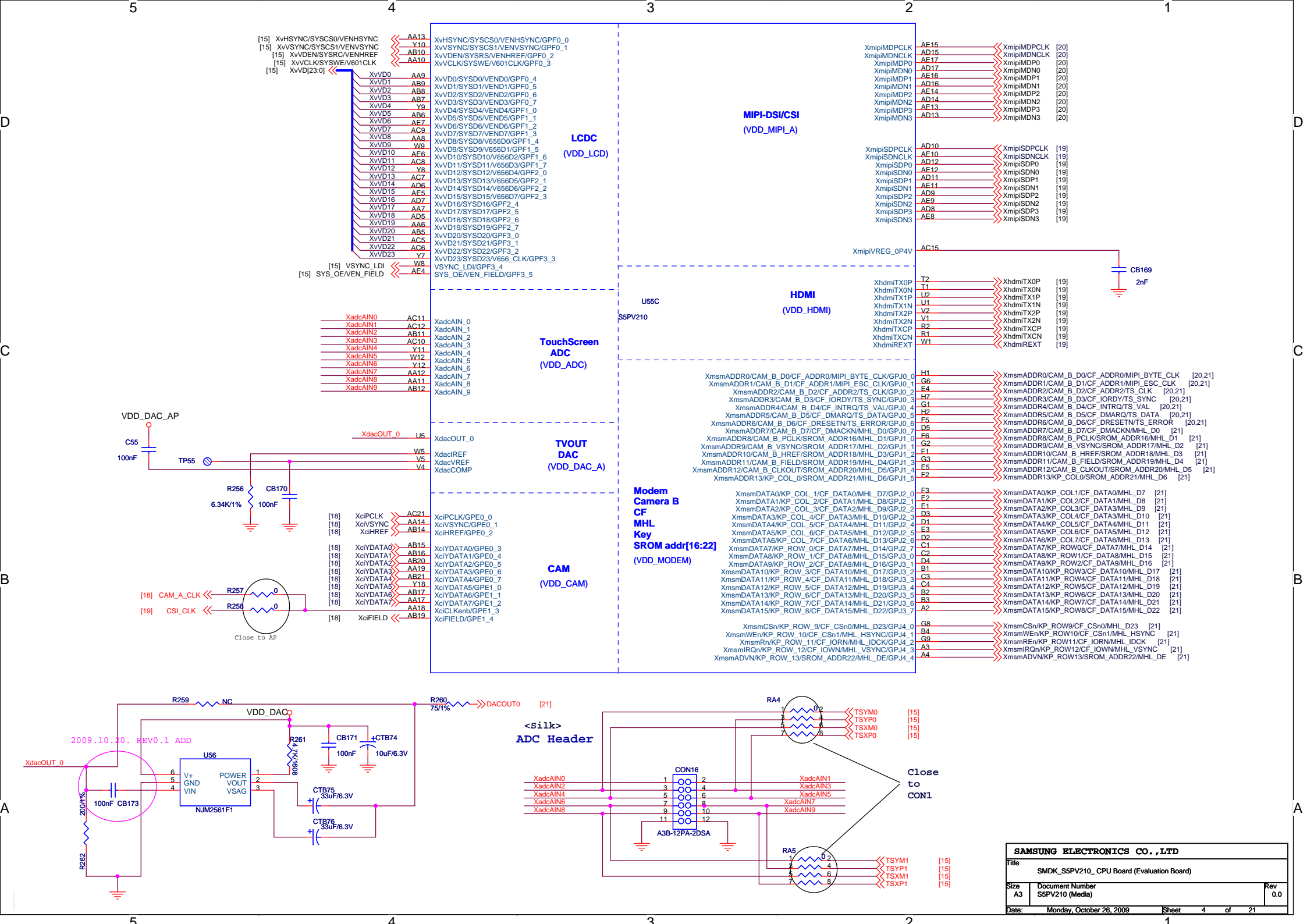
OM[5]	OM[4:1]	OM[0]	Storage
0	0 0 0 0		NAND 512B-4cycle
Boot Seq.	0 0 0 1		NAND 2KB-5cycle
0: Storage	0 0 1 0		NAND 4KB-5cycle 8-ECC
	0 0 1 1		NAND 4KB-5cycle 16-ECC
1: USB-> UART-> Storage	0 1 0 1	0: X-TAL	OneNAND Mux(Audi)
	0 1 1 0	1: X-TAL (USB)	SD/MMC
0: Storage	1 0 0 0		eMMC(4bit)
	1 0 0 1		Reserved
	1 0 1 0		iROM NOR boot
	1 0 1 1		eMMC(8bit)

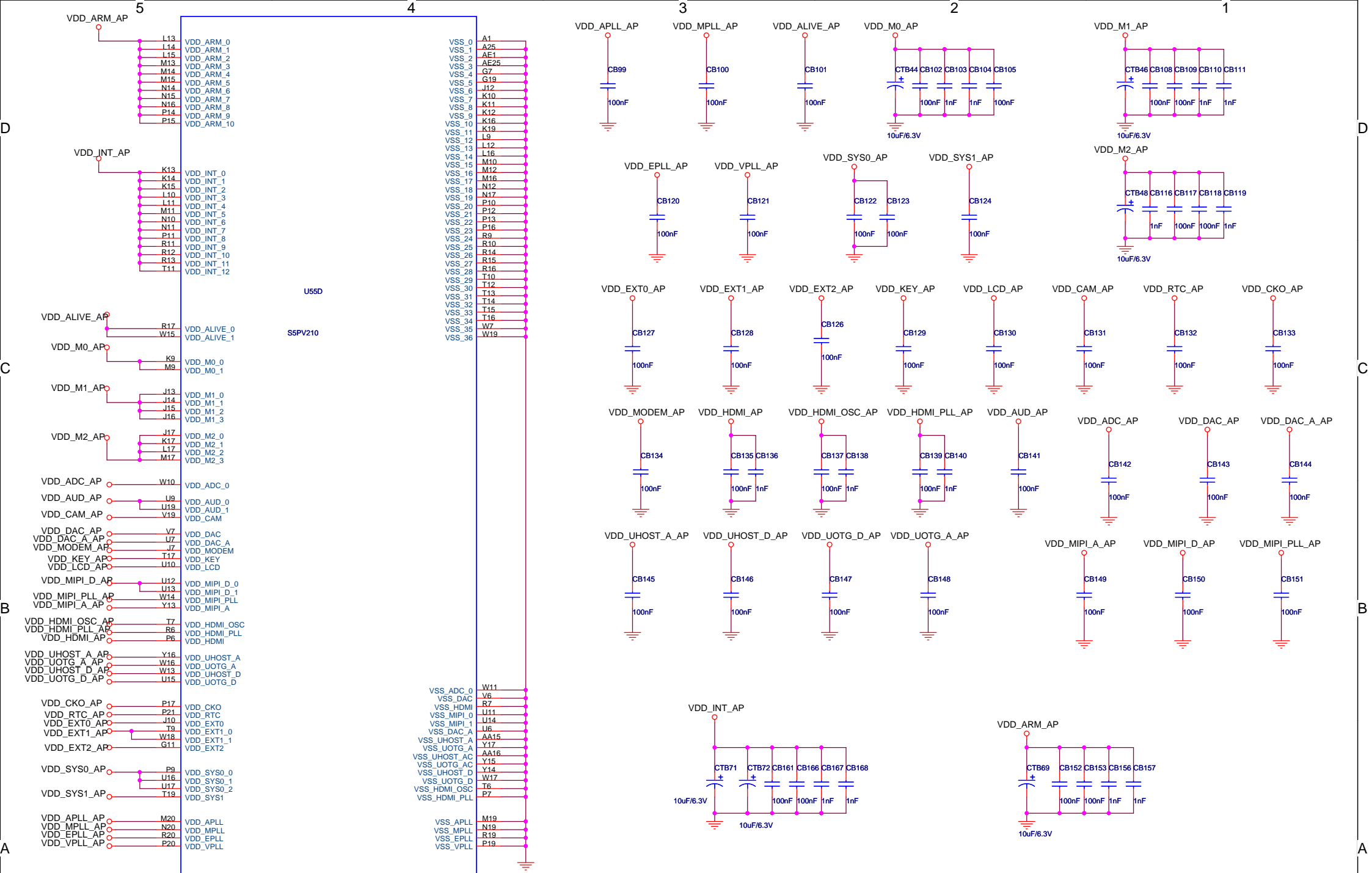


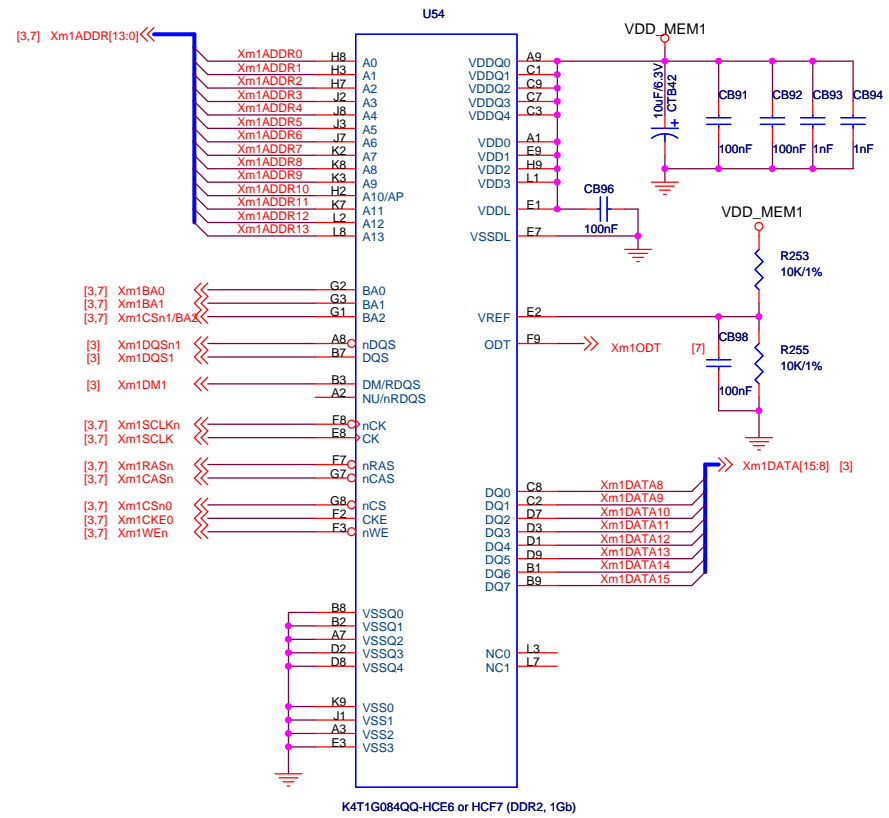
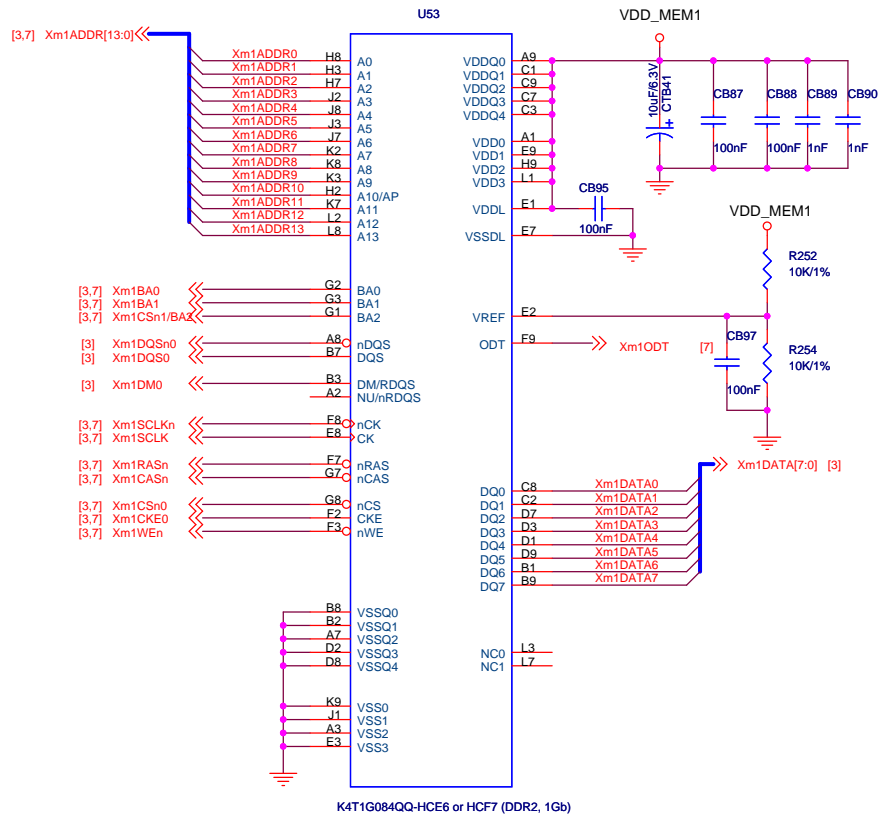
596 Pin FCFBGA



SAMSUNG ELECTRONICS CO., LTD		
Title SMDK_SSPV210_CPU Board (Evaluation Board)		
Size A3	Document Number SSPV210 (DDR2 & SROM Memory)	Rev 0.0
Date: Monday, October 26, 2009	Sheet 3	of 21

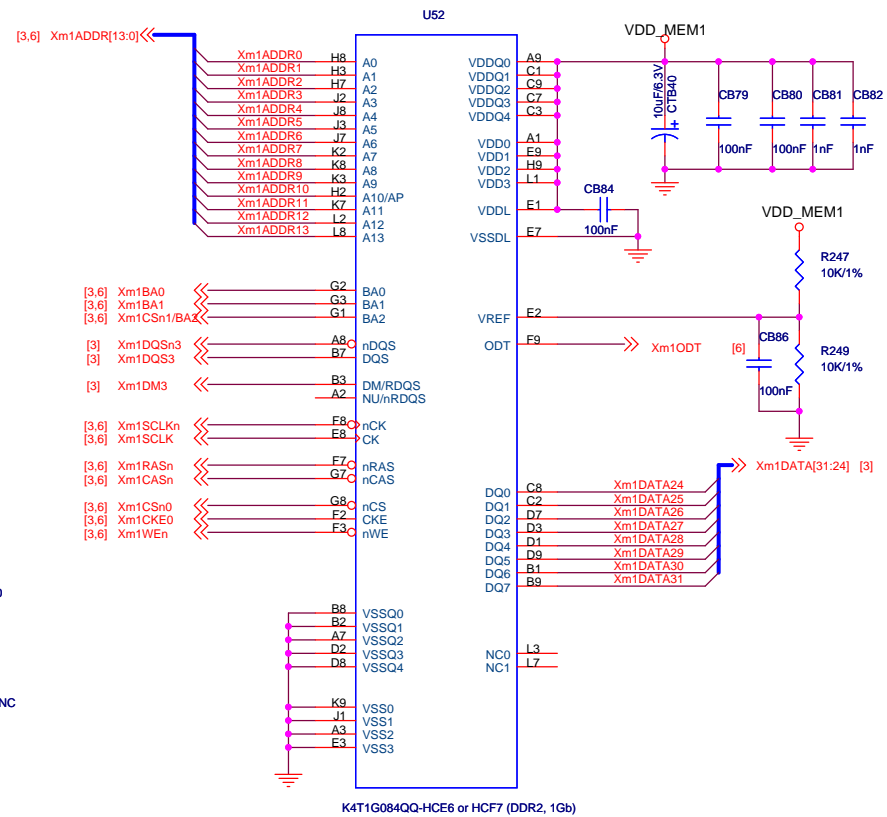
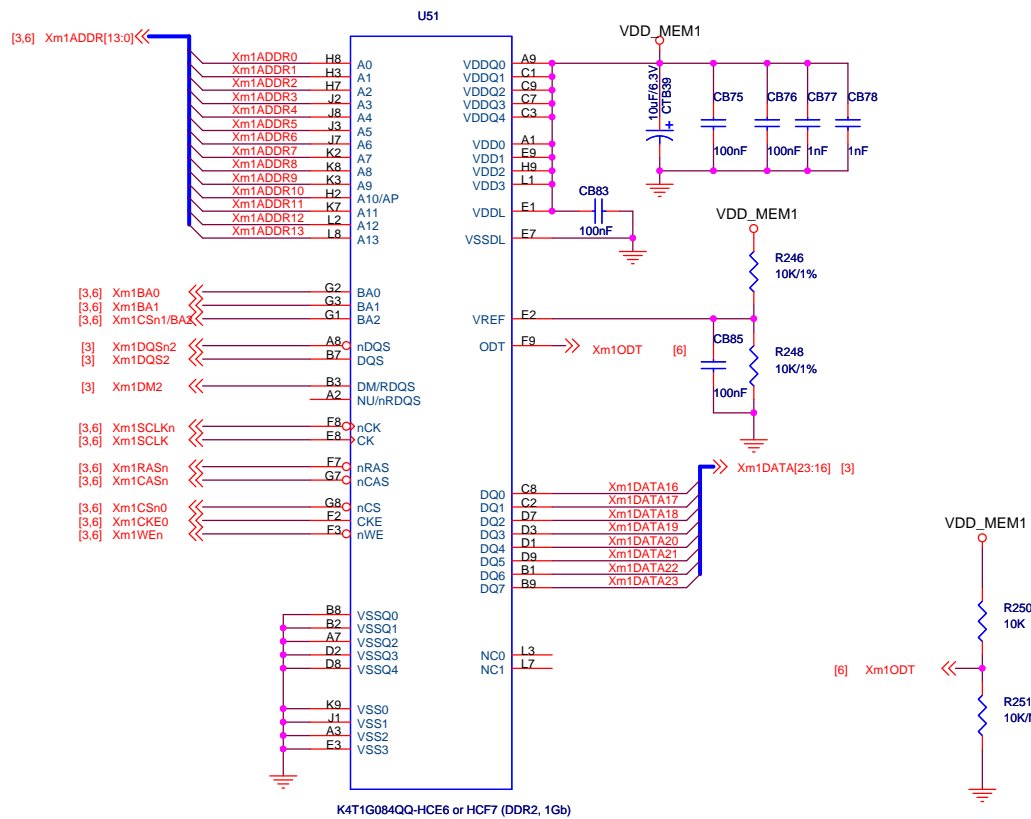






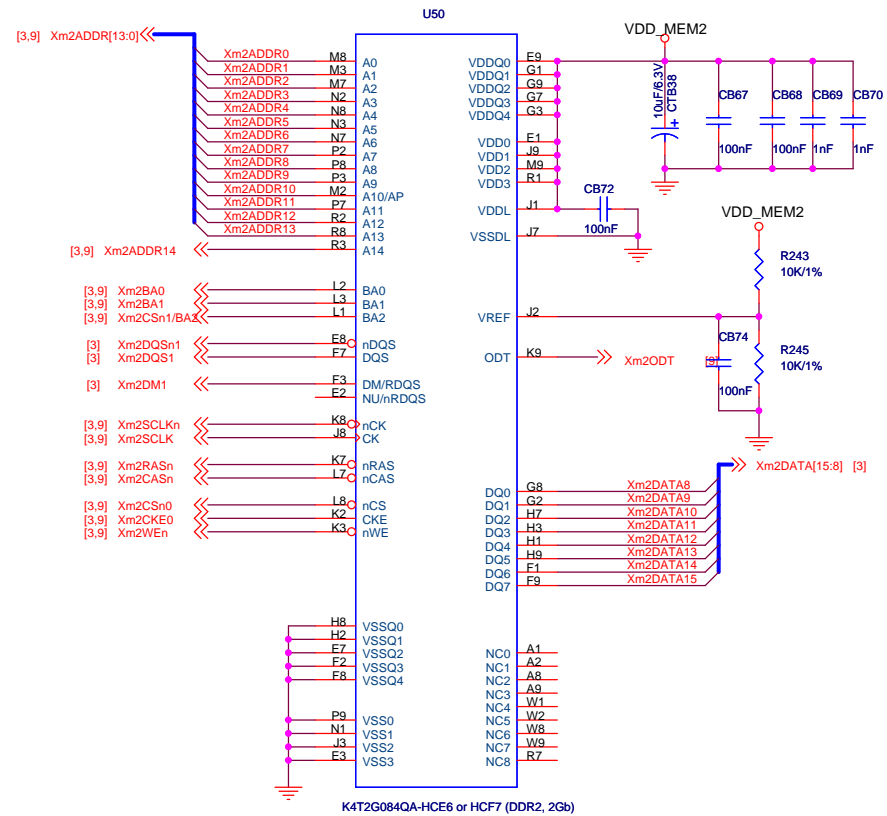
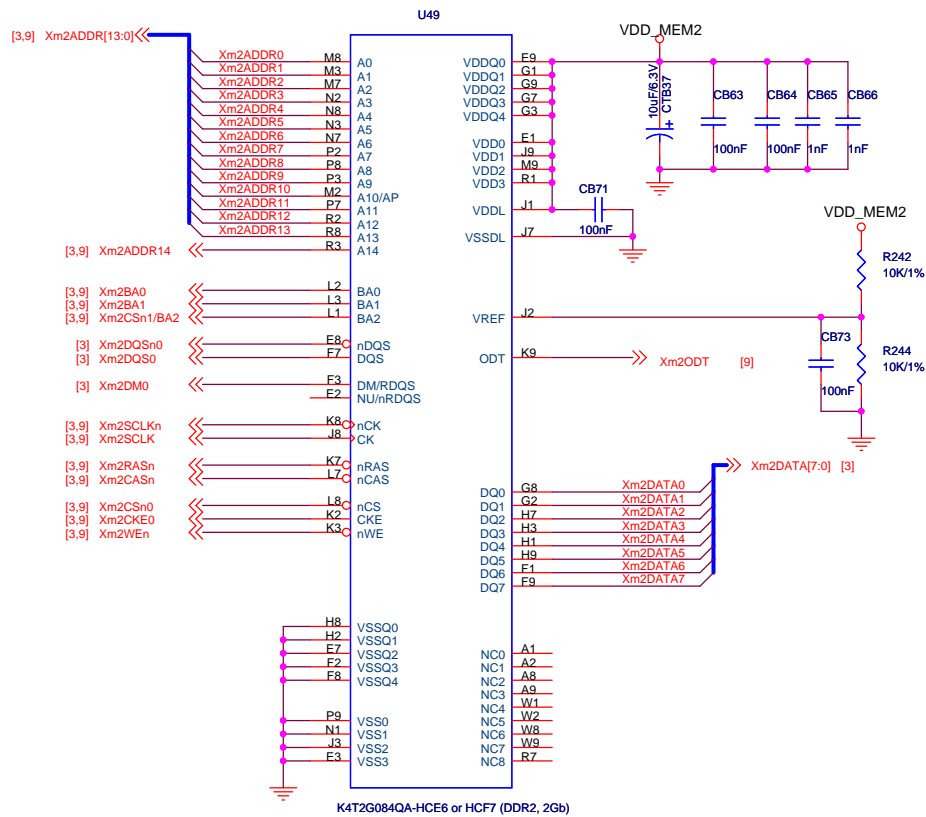
XM1 DDR2(For 1Gbit x8)

SAMSUNG ELECTRONICS CO., LTD		
Title	SMDK_S5PV210_POP CPU Board (Evaluation Board)	
Size	Document Number	Rev
A3	DDR2(1Gbit*4) XM1 #1,2	0.0
Date:	Monday, October 26, 2009	Sheet 6 of 21



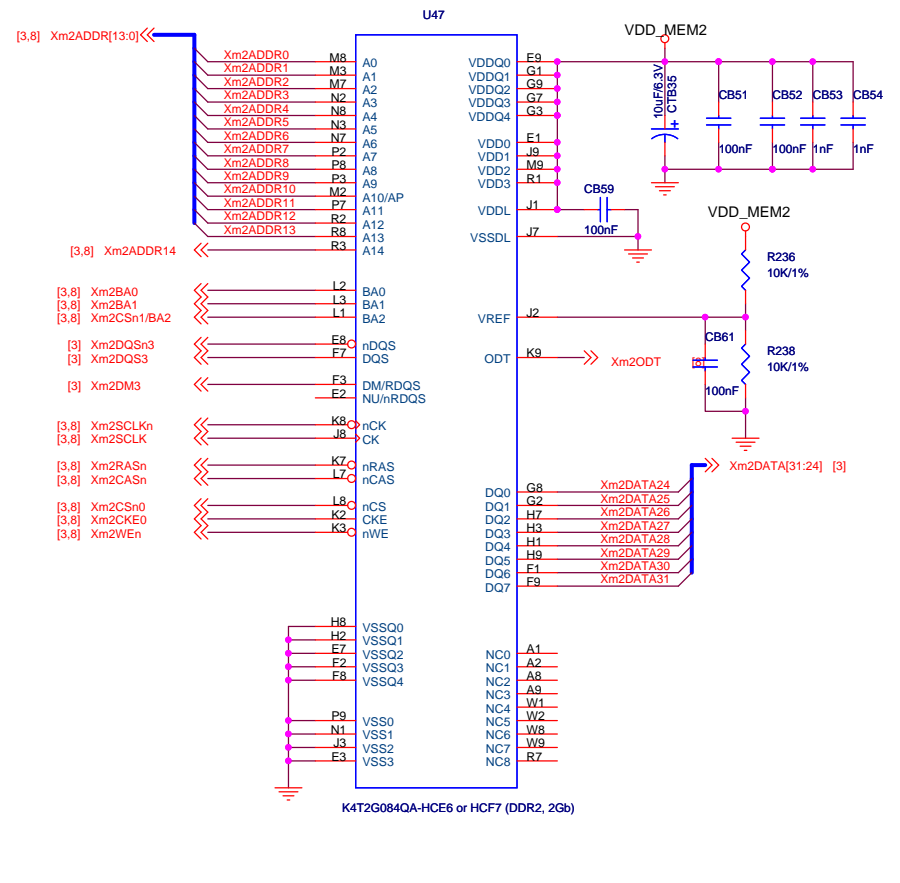
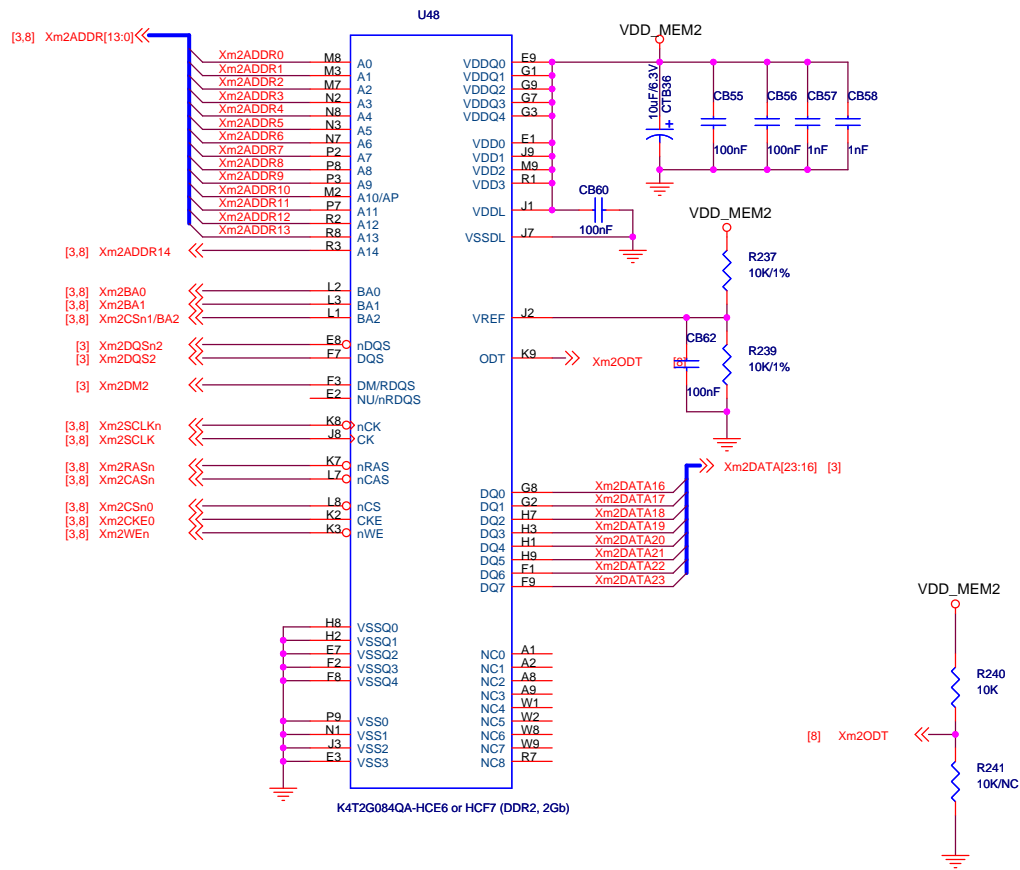
XM1 DDR2(For 1Gbit x8)

SAMSUNG ELECTRONICS CO., LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: DDR2(1Gbit*4) XM1 #2,3	Rev: 0.0
Date: Monday, October 26, 2009	Sheet: 7	of 21



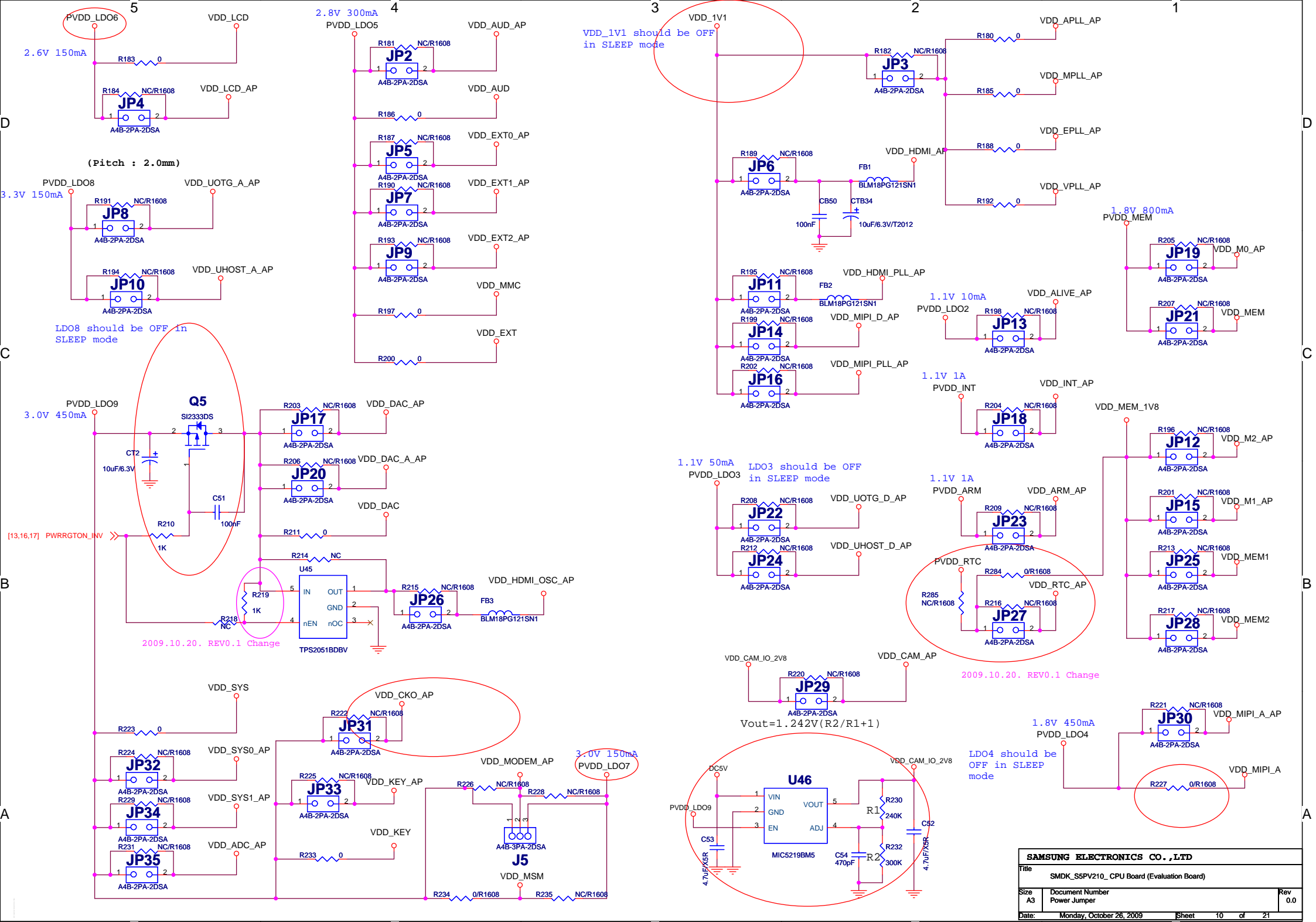
XM2 DDR2(For 2Gbit x8)

SAMSUNG ELECTRONICS CO., LTD		
Title: SMDK_S5PV210_CPU Board (Evaluation Board)		
Size: A3	Document Number: DDR2(2Gbit*4) XM2 #0,1	Rev: 0.0
Date: Monday, October 26, 2009	Sheet: 8	of 21



XM2 DDR2(For 2Gbit x8)

SAMSUNG ELECTRONICS CO., LTD		
Title	SMDK_S5PV210_POP CPU Board (Evaluation Board)	
Size	Document Number	Rev
A3	DDR2(2Gbit*4) XM2 #2,3	0.0
Date:	Monday, October 26, 2009	Sheet 9 of 21



VDD_1V1 should be OFF in SLEEP mode

(Pitch : 2.0mm)

LDO8 should be OFF in SLEEP mode

LDO3 should be OFF in SLEEP mode

LDO4 should be OFF in SLEEP mode

2009.10.20. REV0.1 Change

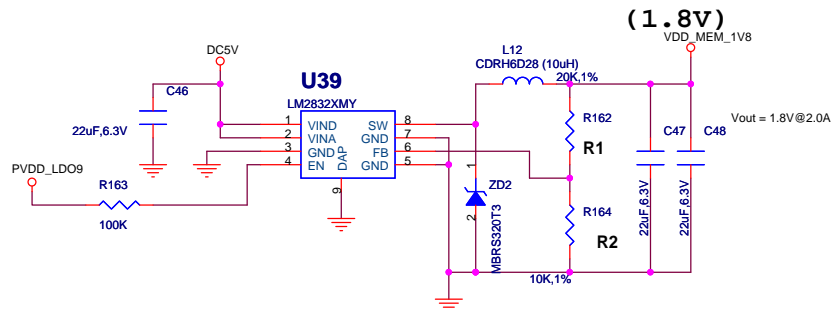
2009.10.20. REV0.1 Change

$$V_{out} = 1.242V \left(\frac{R2}{R1+1} \right)$$

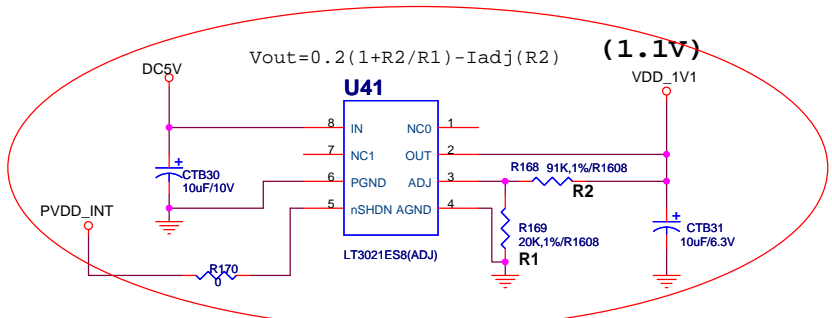
SAMSUNG ELECTRONICS CO., LTD		
Title SMDK_SSPV210_CPU Board (Evaluation Board)		
Size A3	Document Number Power Jumper	Rev 0.0
Date: Monday, October 26, 2009	Sheet 10	of 21

$$V_{out} = 0.60(1 + R1/R2)$$

$$R1 = R2(V_{out}/0.60V - 1)$$

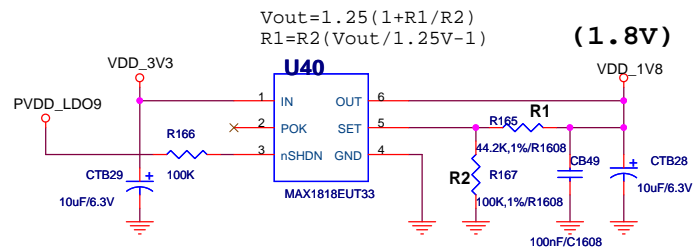


$$V_{out} = 0.2(1 + R2/R1) - I_{adj}(R2)$$



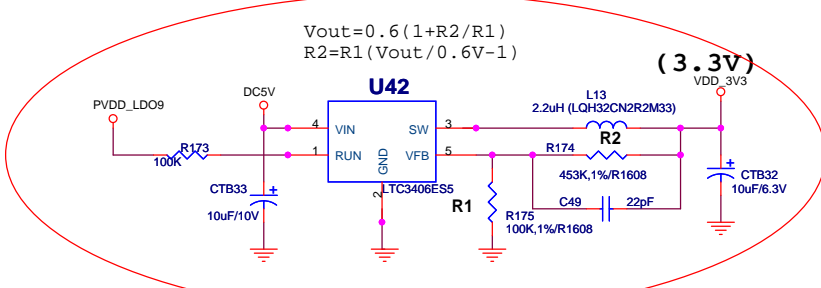
$$V_{out} = 1.25(1 + R1/R2)$$

$$R1 = R2(V_{out}/1.25V - 1)$$

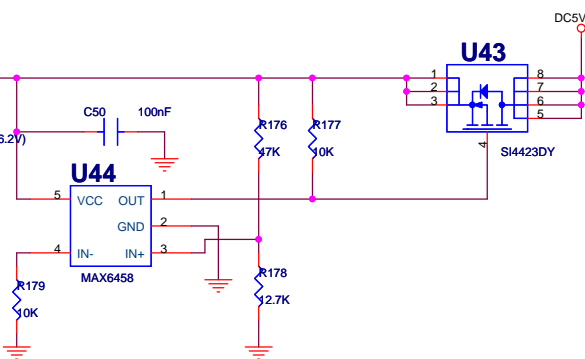
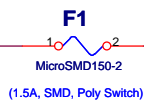
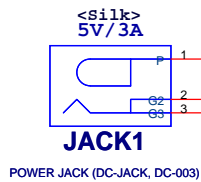
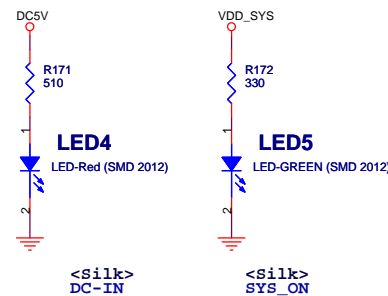


$$V_{out} = 0.6(1 + R2/R1)$$

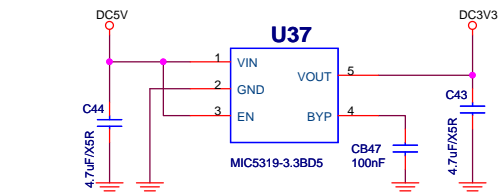
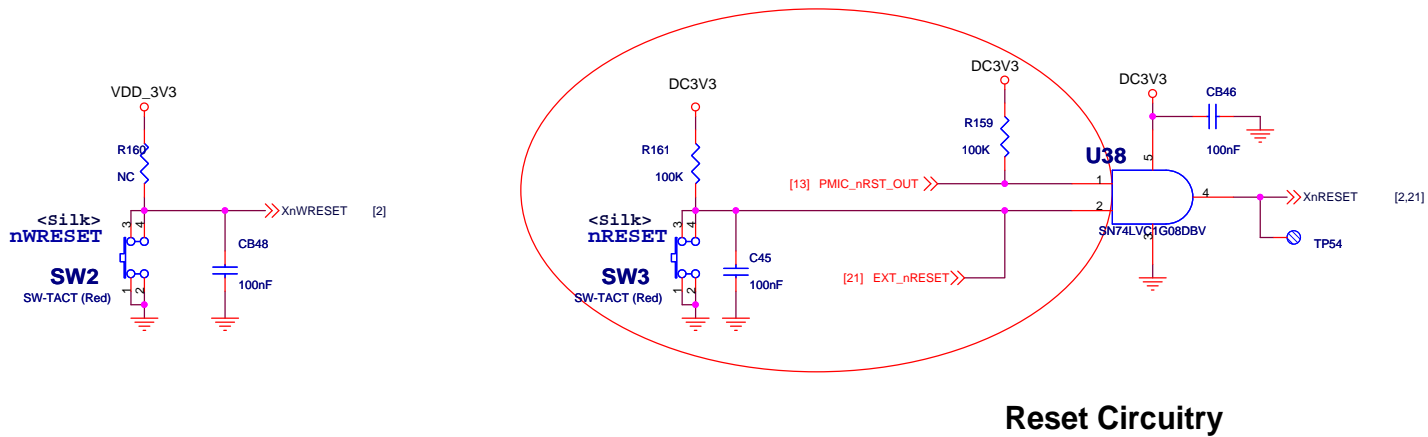
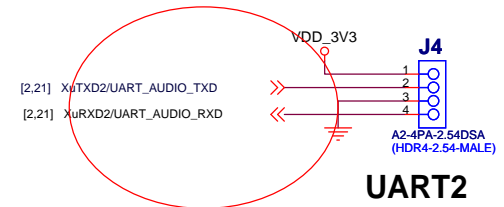
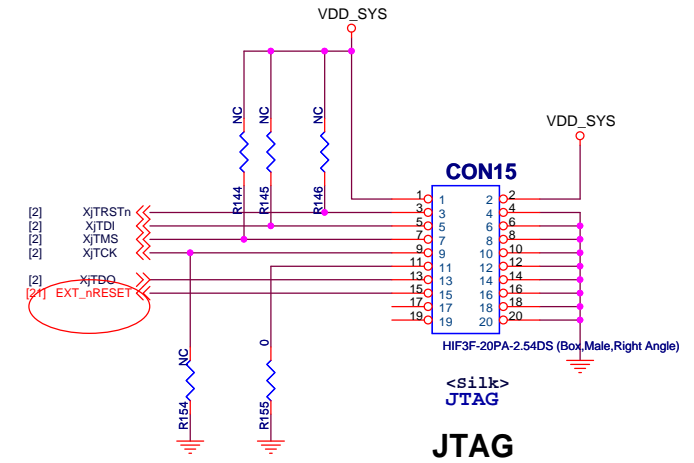
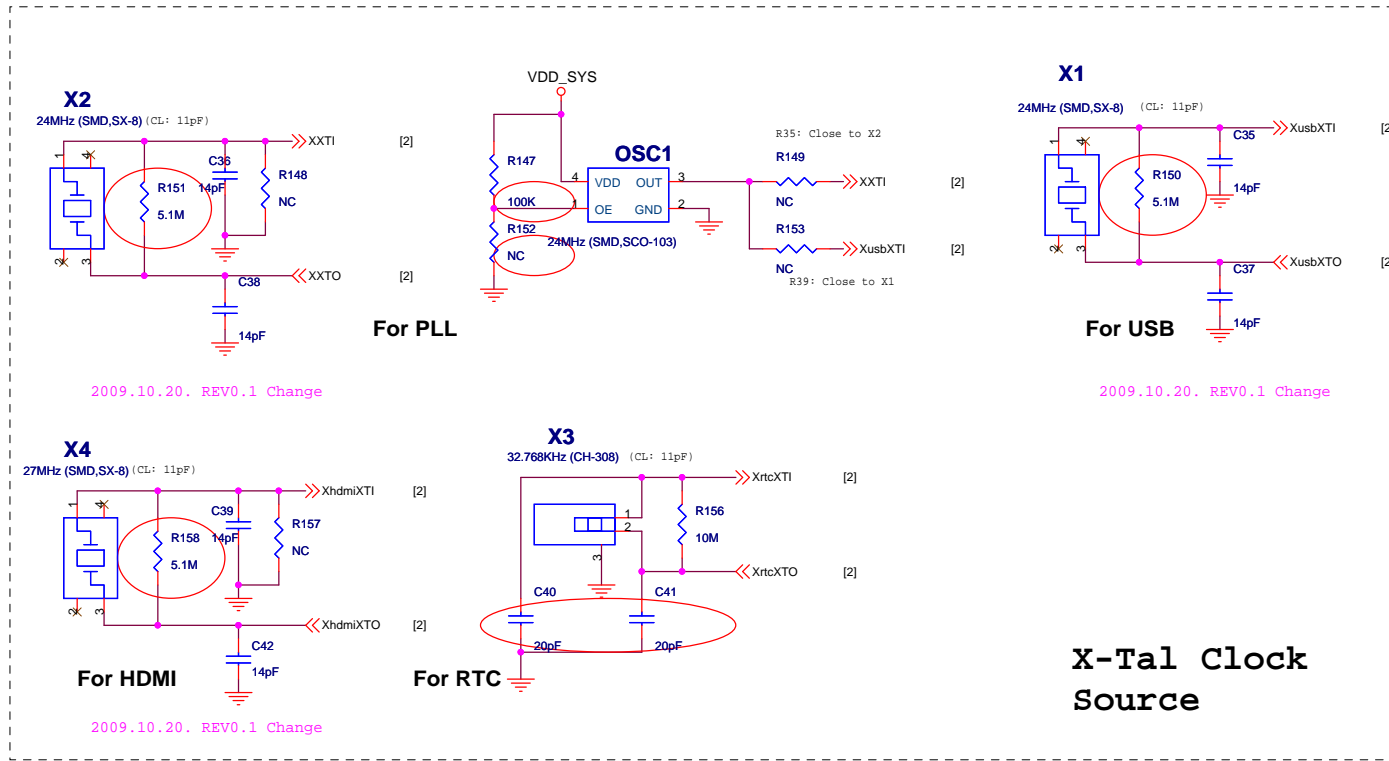
$$R2 = R1(V_{out}/0.6V - 1)$$



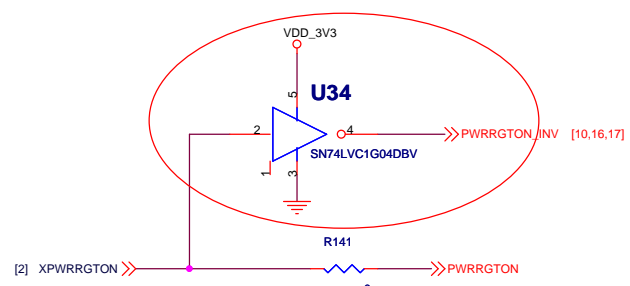
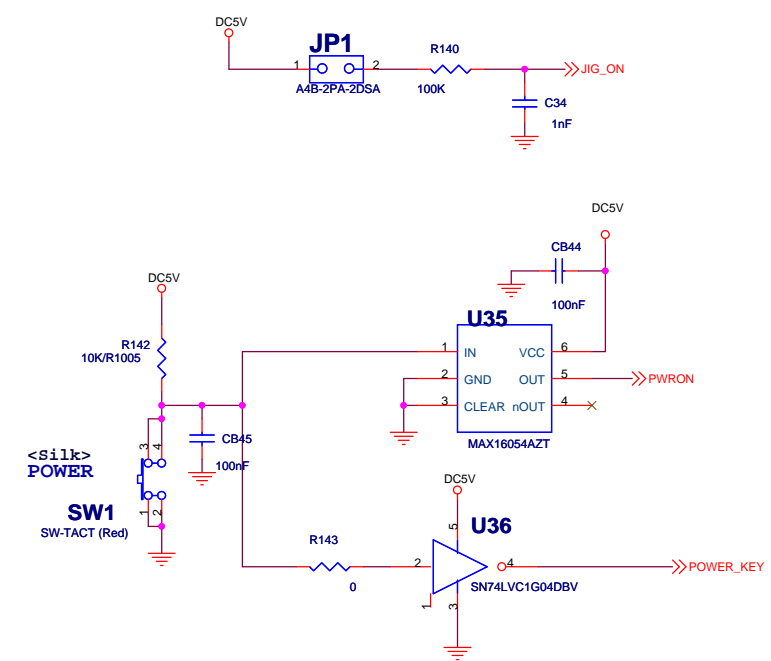
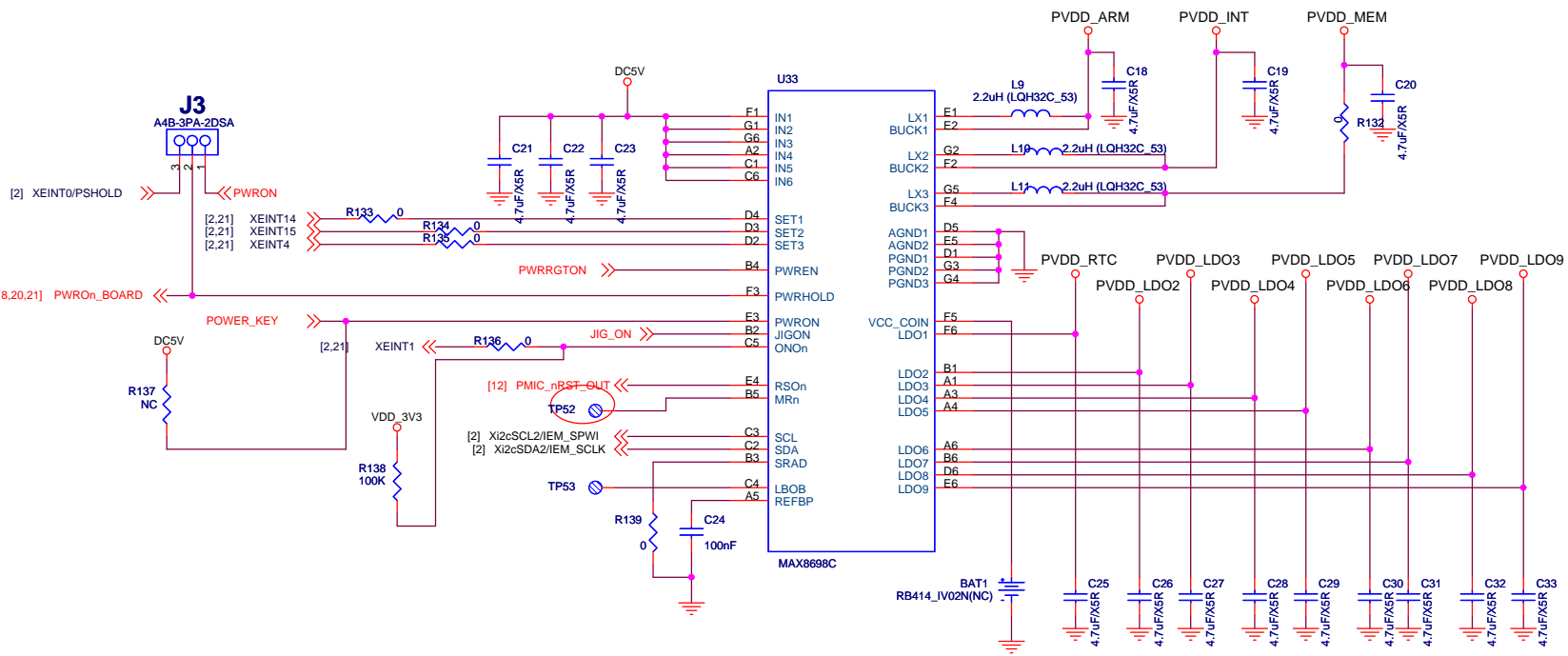
2009.10.20. REV0.1 Change



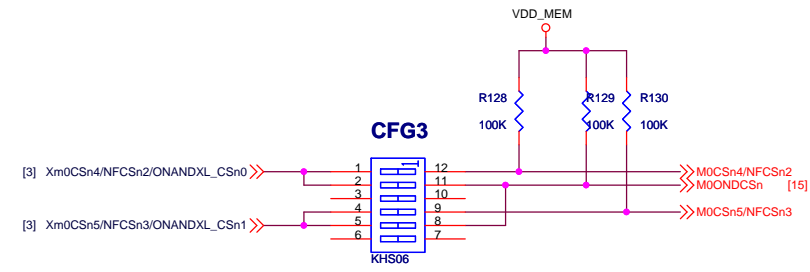
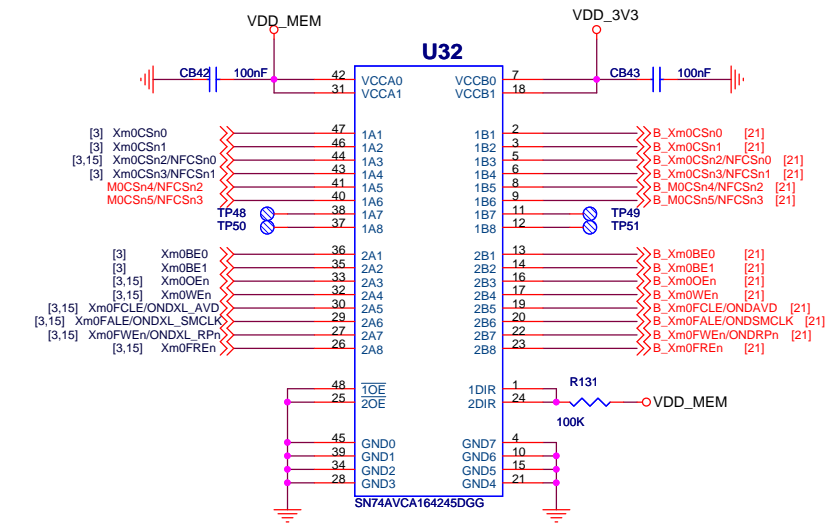
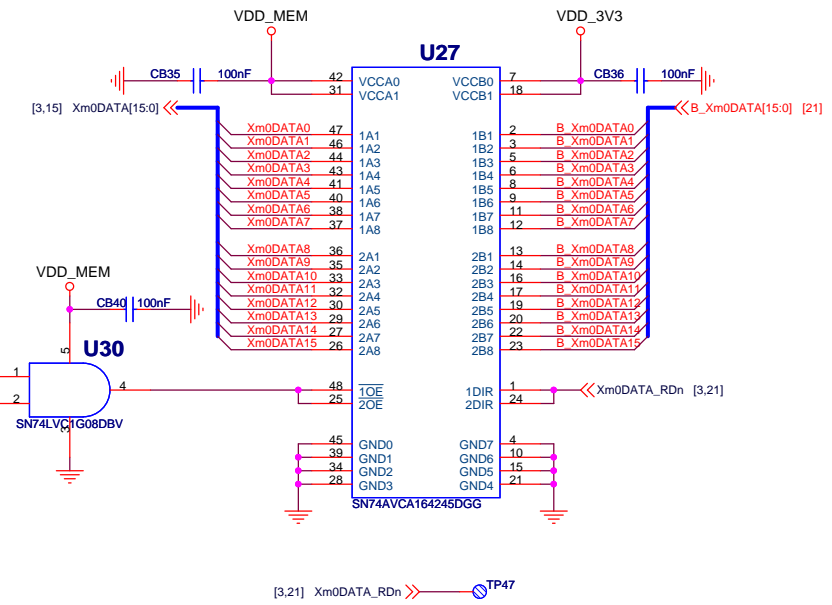
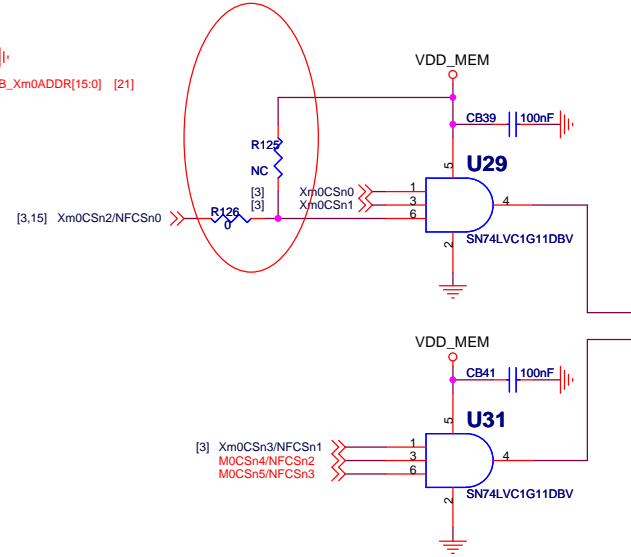
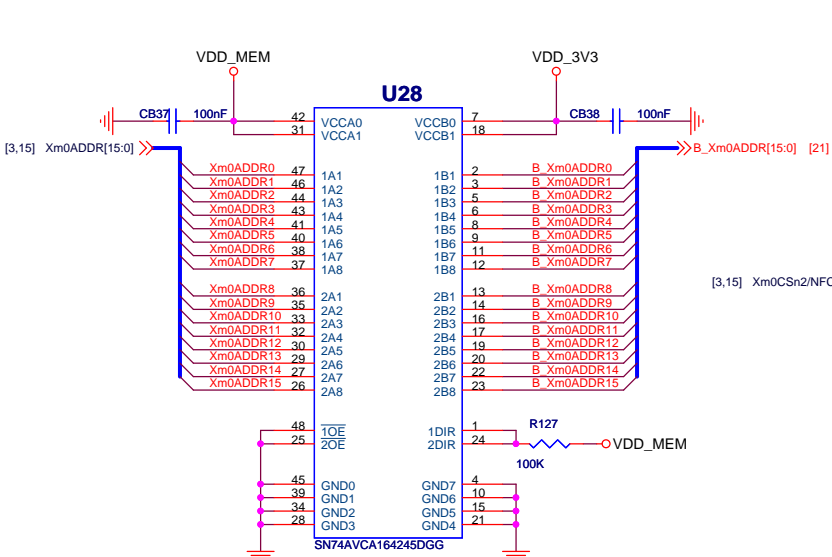
SAMSUNG ELECTRONICS CO., LTD		
Title	SMDK_S5PV210_CPU Board (Evaluation Board)	
Size	Document Number	Rev
A3	Power(DCJack&Regulator)	0.0
Date:	Monday, October 26, 2009	Sheet 11 of 21



SAMSUNG ELECTRONICS CO., LTD		
Title SMDK_S5PV210_POP CPU Board (Evaluation Board)		
Size A3	Document Number Reset / Clock source / JTAG	Rev 0.0
Date: Monday, October 26, 2009	Sheet 12	of 21

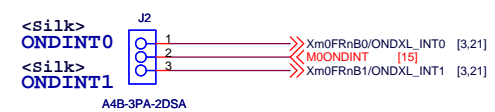


SAMSUNG ELECTRONICS CO., LTD		
Title		
SMDK_SSPV210_CPU Board (Evaluation Board)		
Size	Document Number	Rev
A3	Power - PMIC Socket	0.0
Date:	Monday, October 26, 2009	Sheet 13 of 21

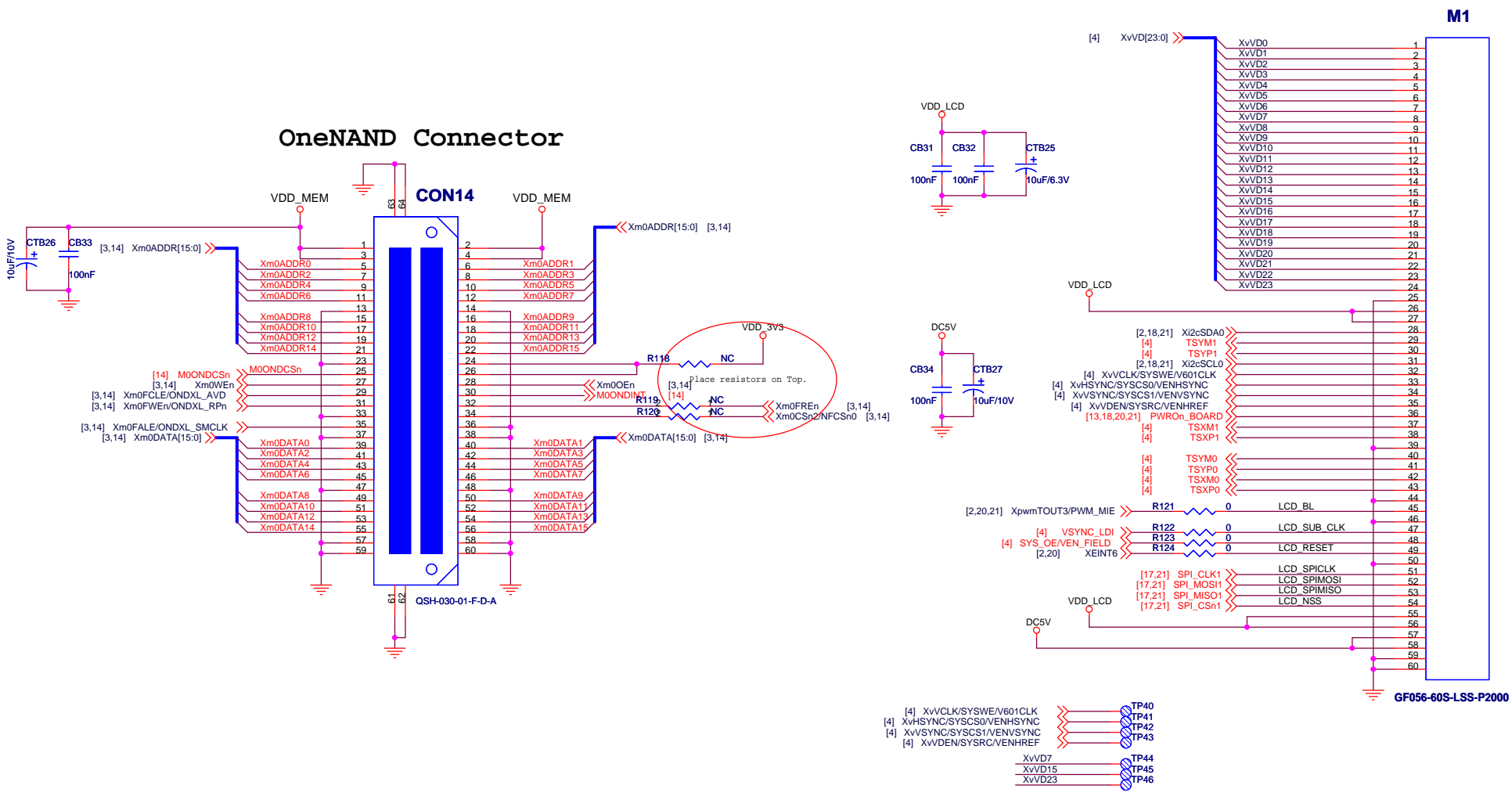


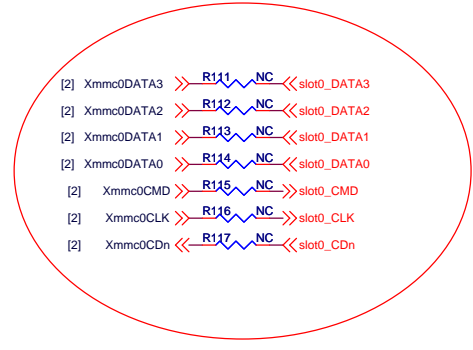
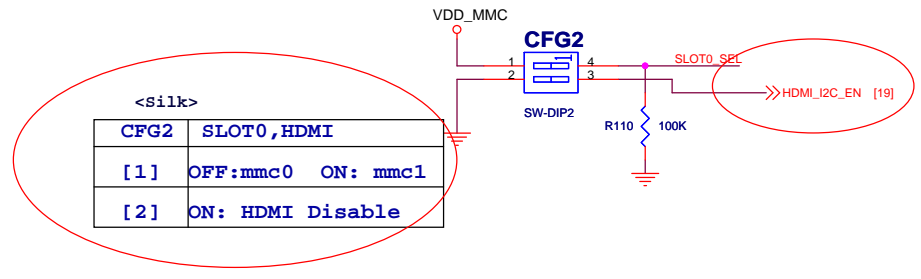
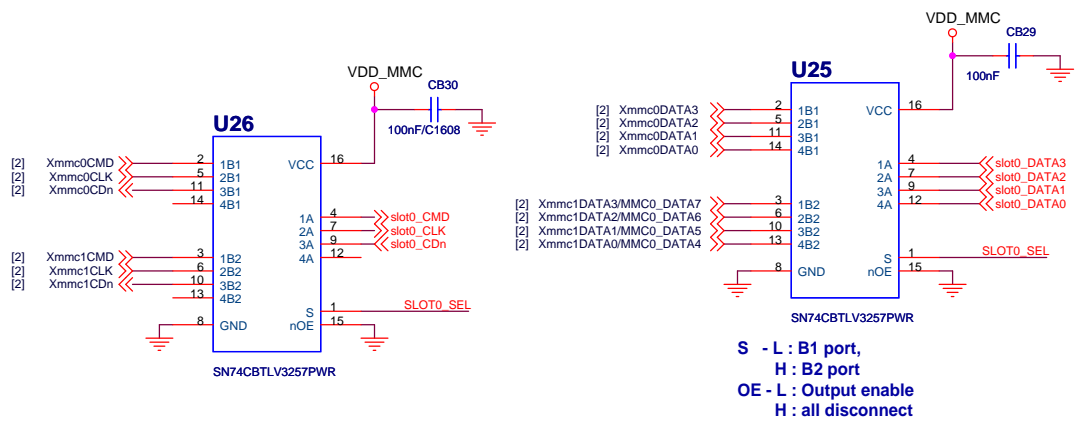
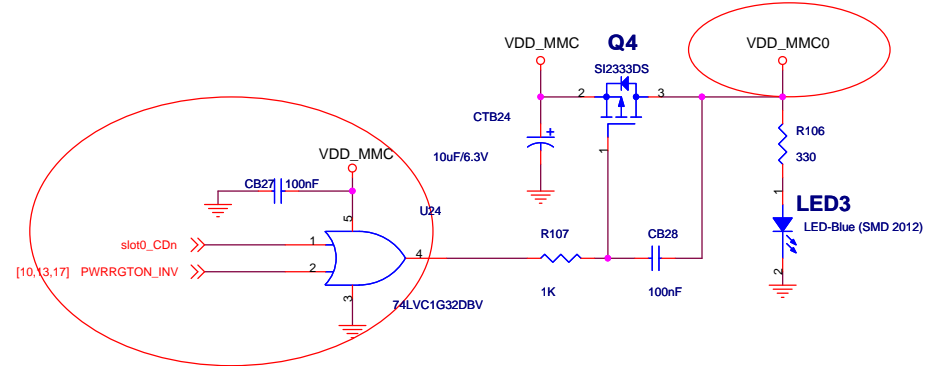
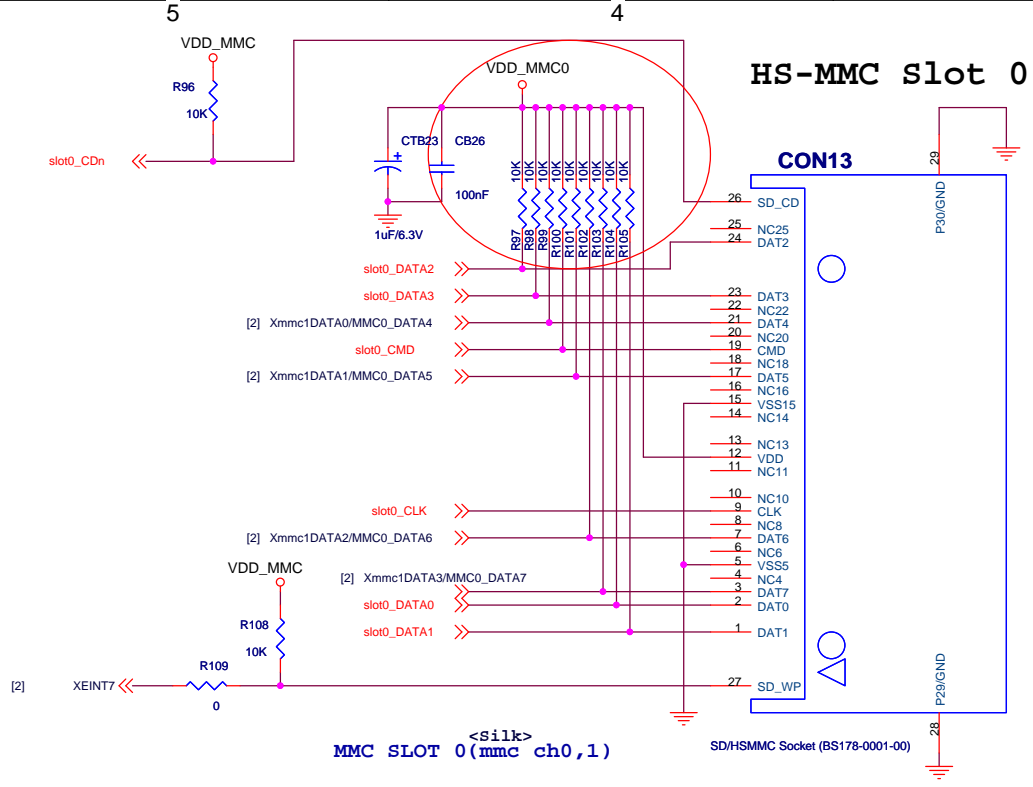
<Silk>

CS4	CS5	
1	4	Base B'd
2	5	EXT. OND
3	6	POP. OND

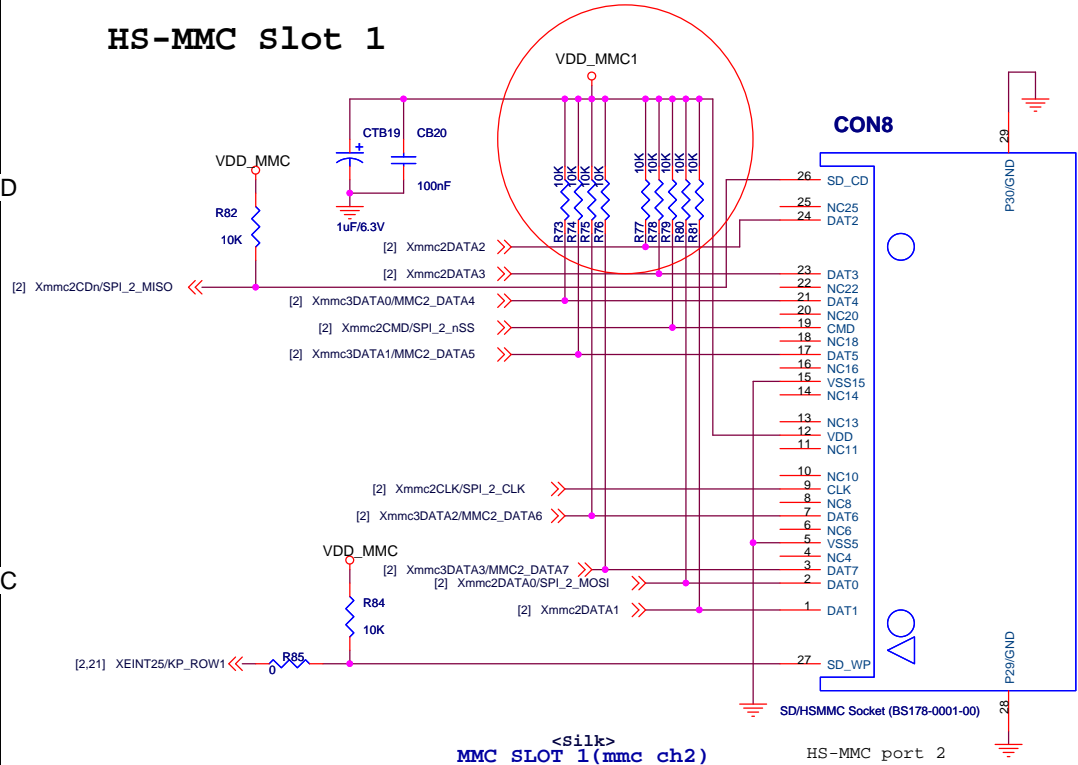


TFT LCD FPC Cable Interface (MODULE Board)



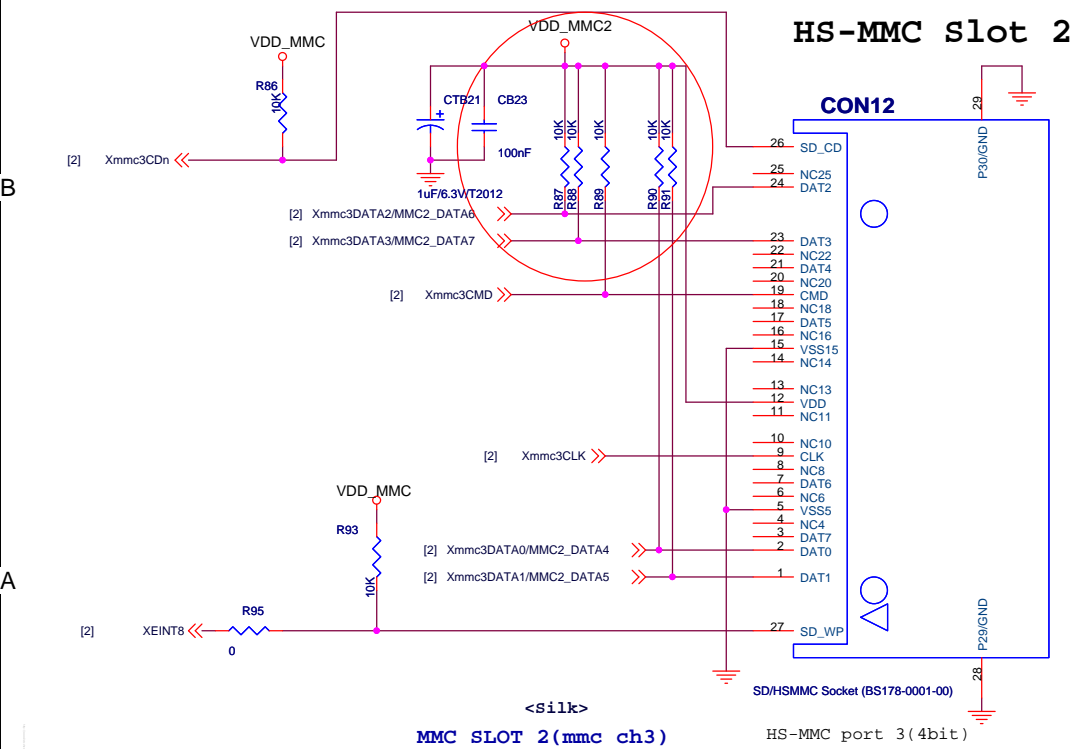


HS-MMC slot 1

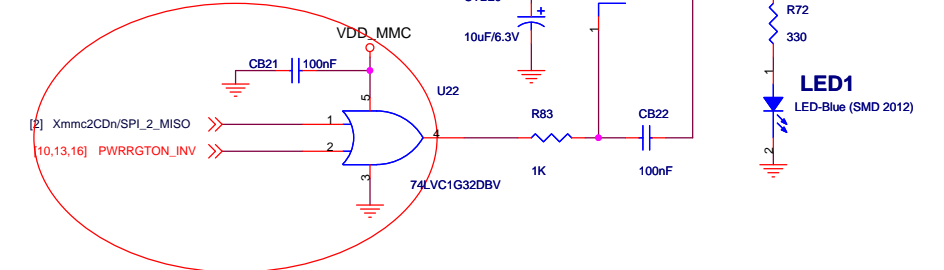


<silkscreen>
MMC SLOT 1(mmc ch2)

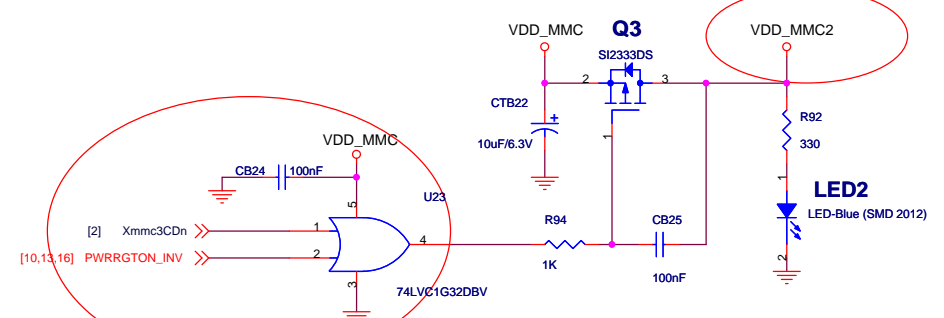
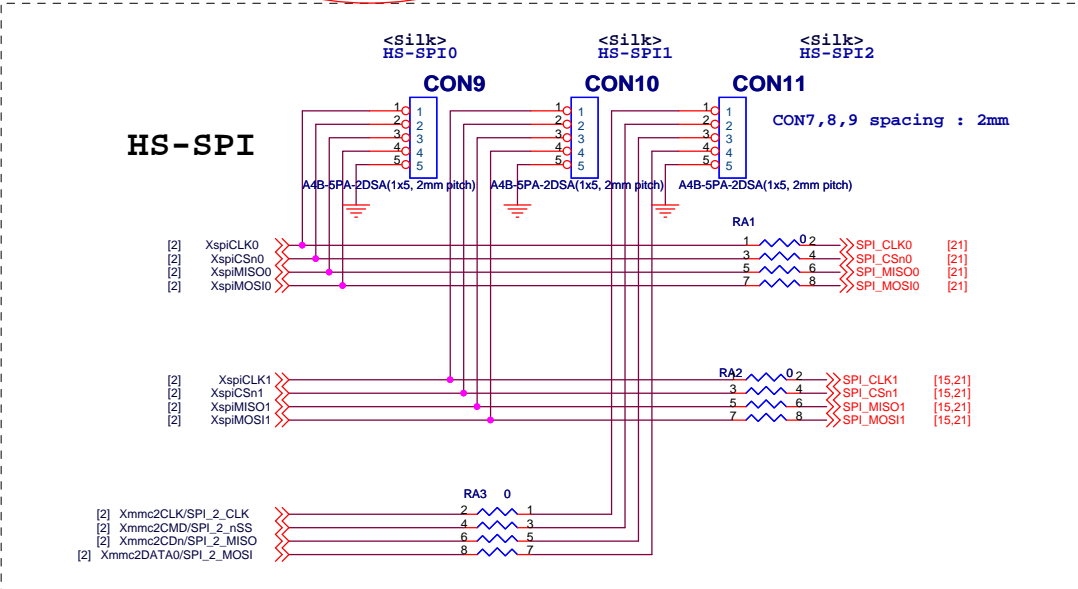
HS-MMC slot 2



<silkscreen>
MMC SLOT 2(mmc ch3)

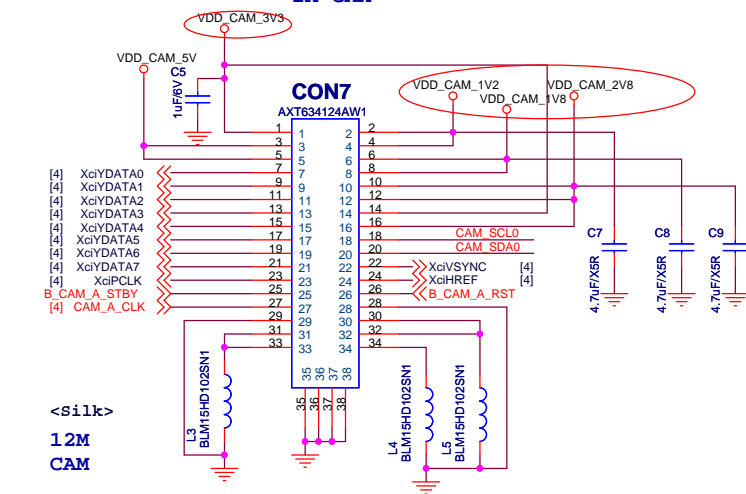
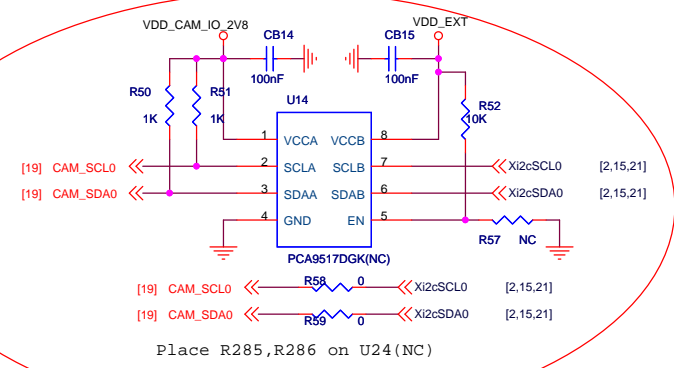
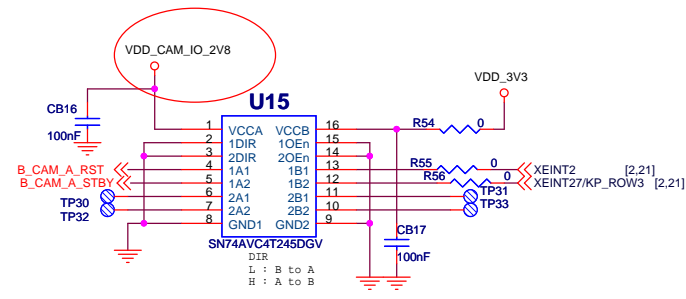
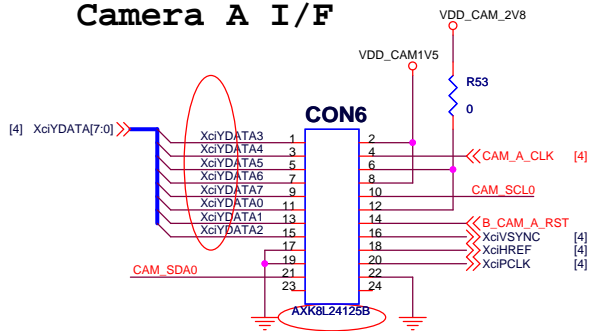


HS-SPI

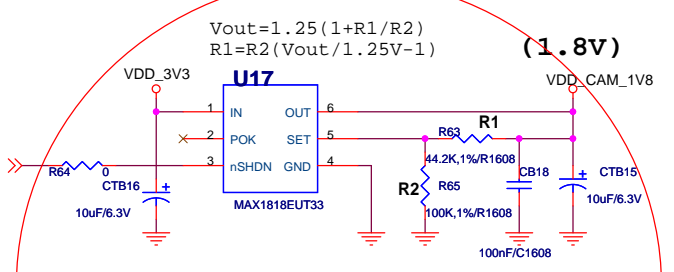
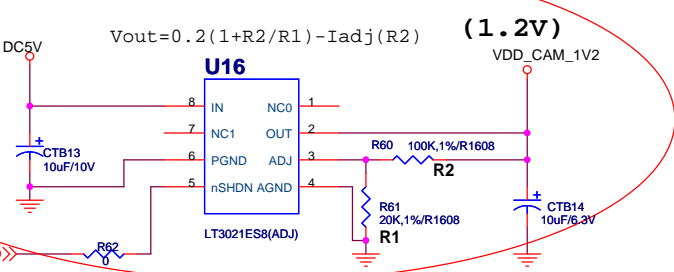


SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PV210_CPU Board (Evaluation Board)		
Size A3	Document Number MMC#1#2/ HS-SPI	Rev 0.0
Date: Monday, October 26, 2009	Sheet 17	of 21

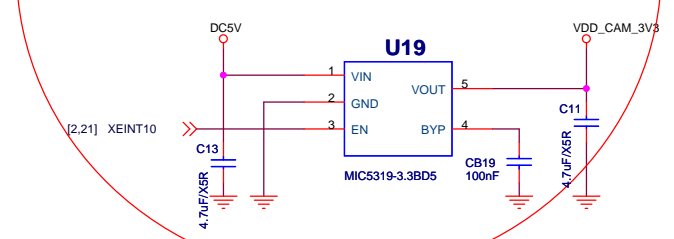
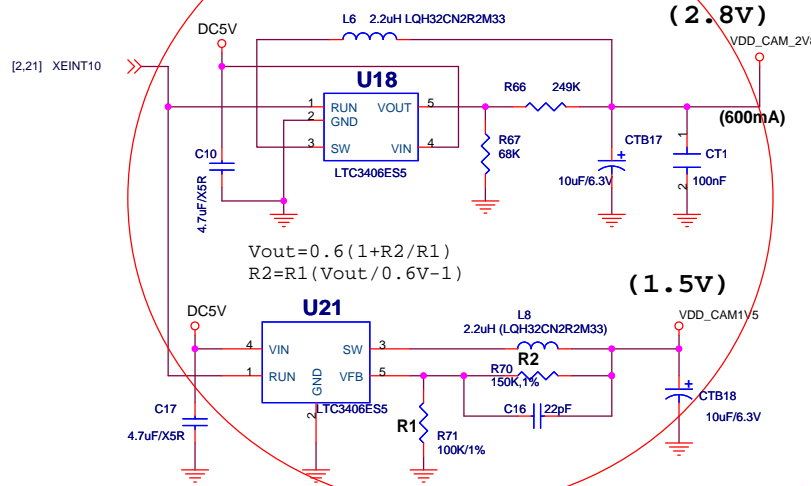
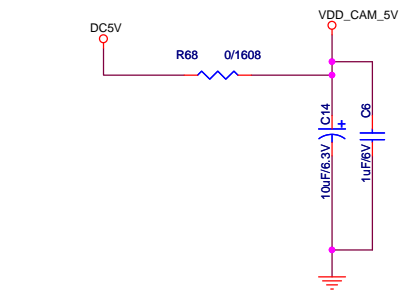
Camera A I/F



- [4] XciFIELD >> TP34 A_FIELD
- [4] XciPCLK << TP35 A_CAMCLK
- [4] XciVSYNC << TP36 A_CAMVSYNC
- [4] XciHREF << TP37 A_CAMHREF
- [4] XciYDATA0 << TP38 A_CAMDATA0
- [4] CAM_A_CLK >> TP39 FLASH

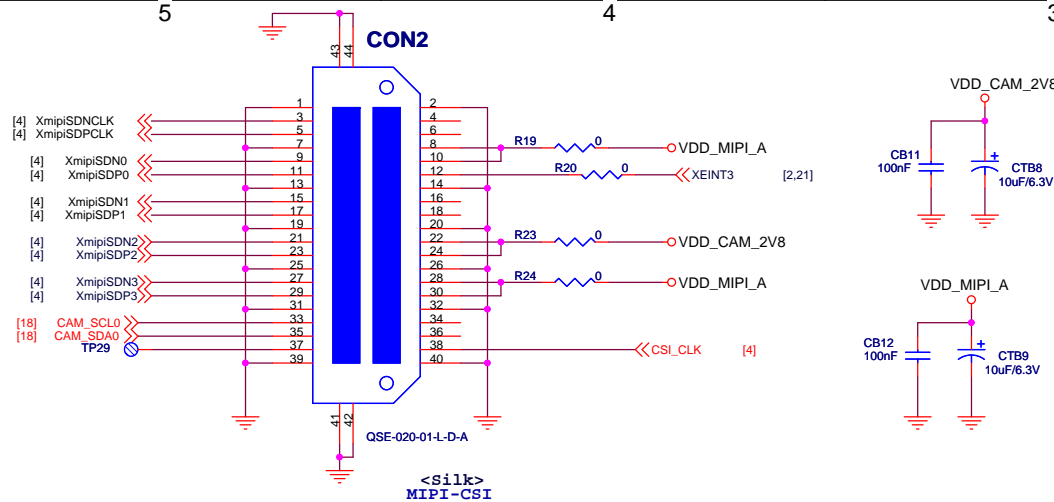


Power for CAM

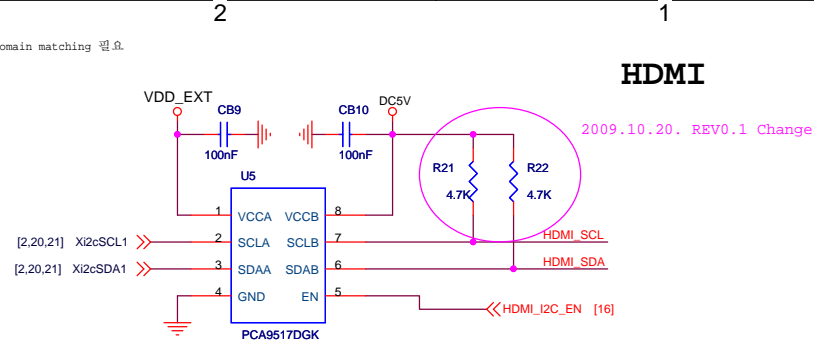


2009.10.20. REV0.1 Change

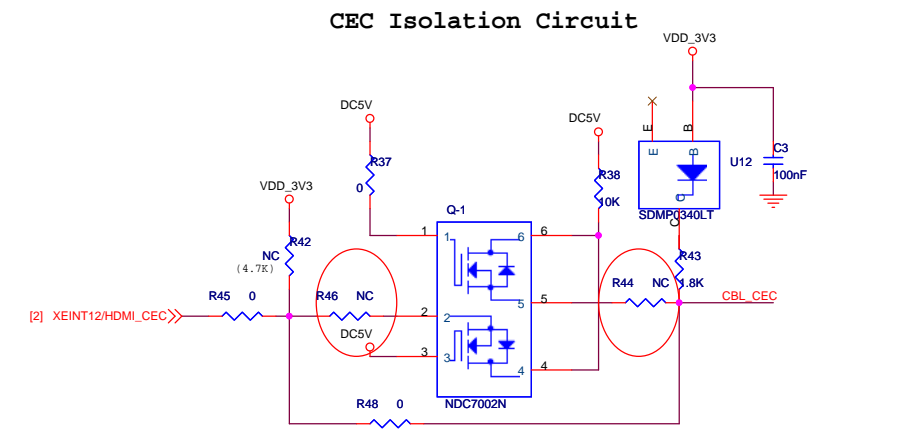
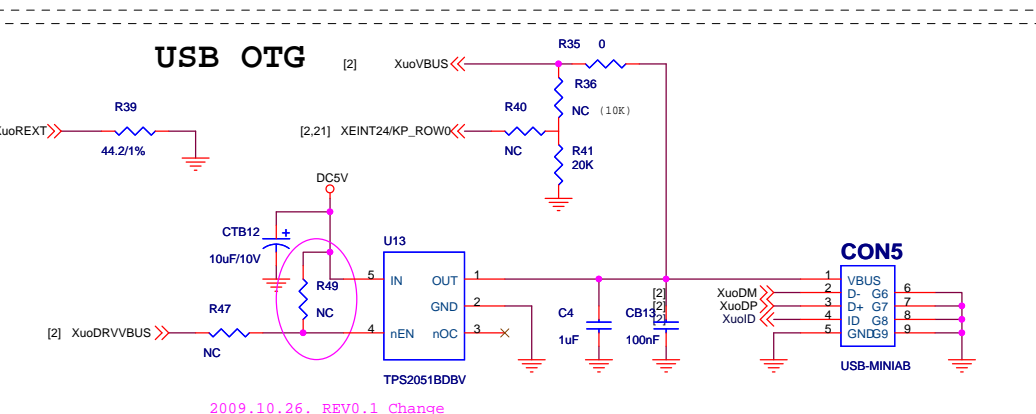
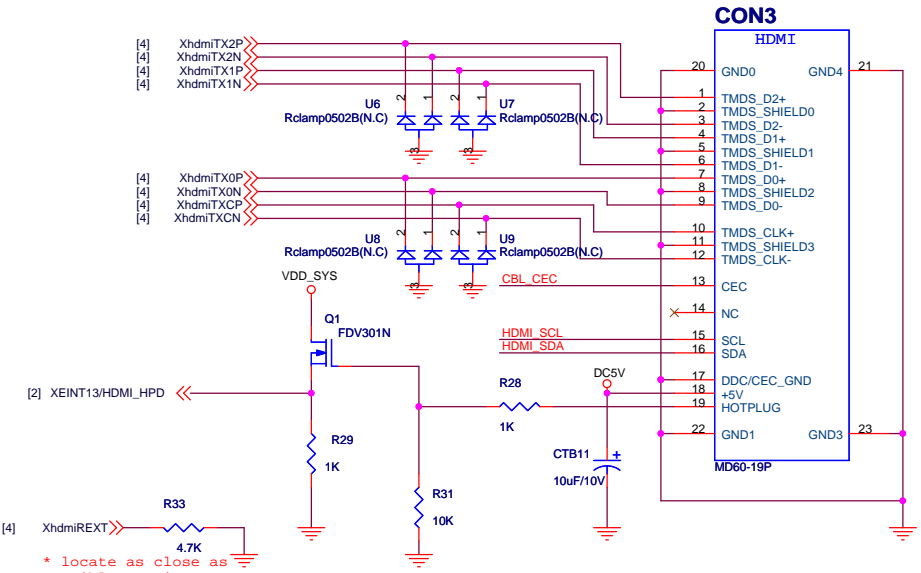
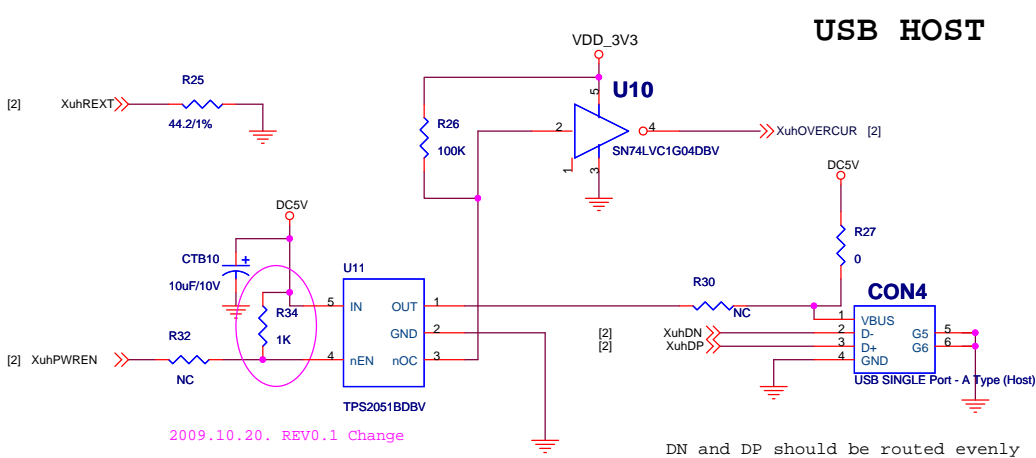
SAMSUNG ELECTRONICS CO.,LTD		
Title	SMDK_S5PV210_CPU Board (Evaluation Board)	
Size	Document Number	Rev
A3	MMC#1 / HS-SPI / Camera I/F A Port(Non-MIPI)	0.0
Date:	Monday, October 26, 2009	Sheet 18 of 21



MIPI-CSI Camera Module Interface

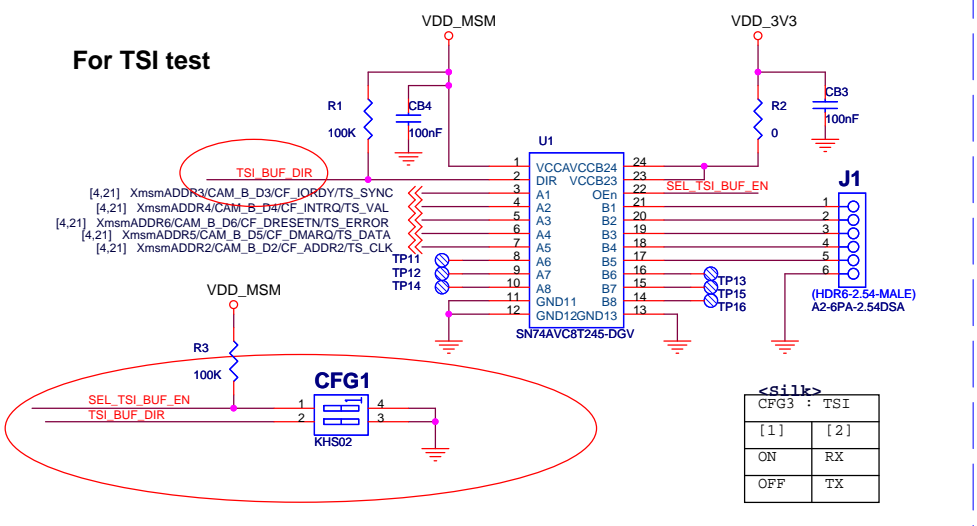


HDMI

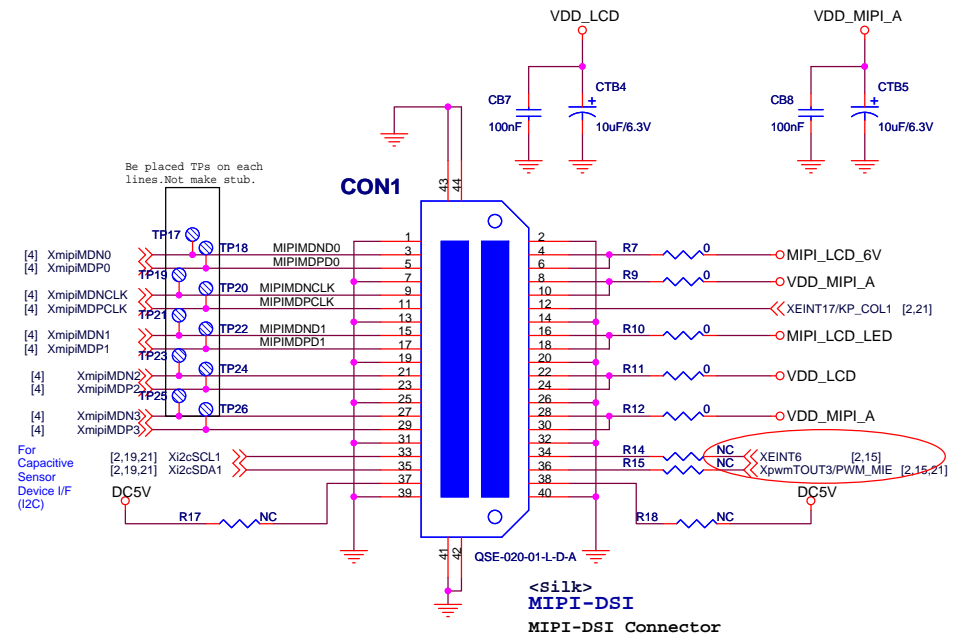
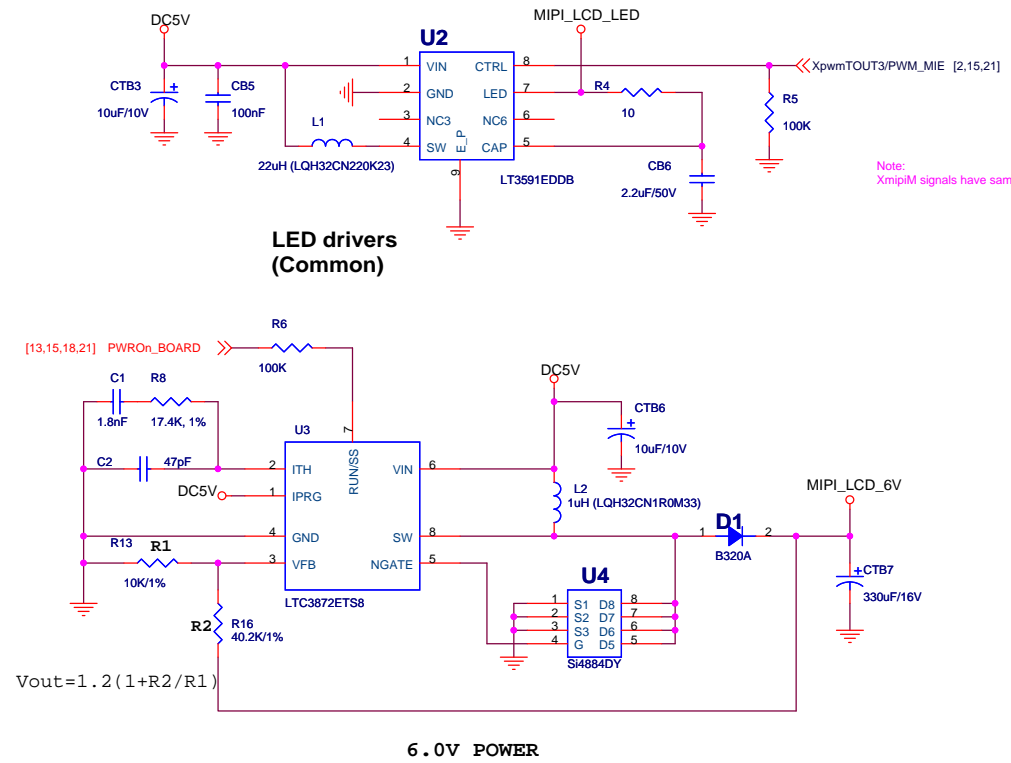


SAMSUNG ELECTRONICS CO.,LTD			
Title	SMDK_S5PV210_CPU Board (Evaluation Board)		
Size	A3	Document Number	HDMI/ MIPI-CSI/ MIPI-HS/ USB
Date	Monday, October 26, 2009	Sheet	19 of 21
Rev	0.0		

For TSI test

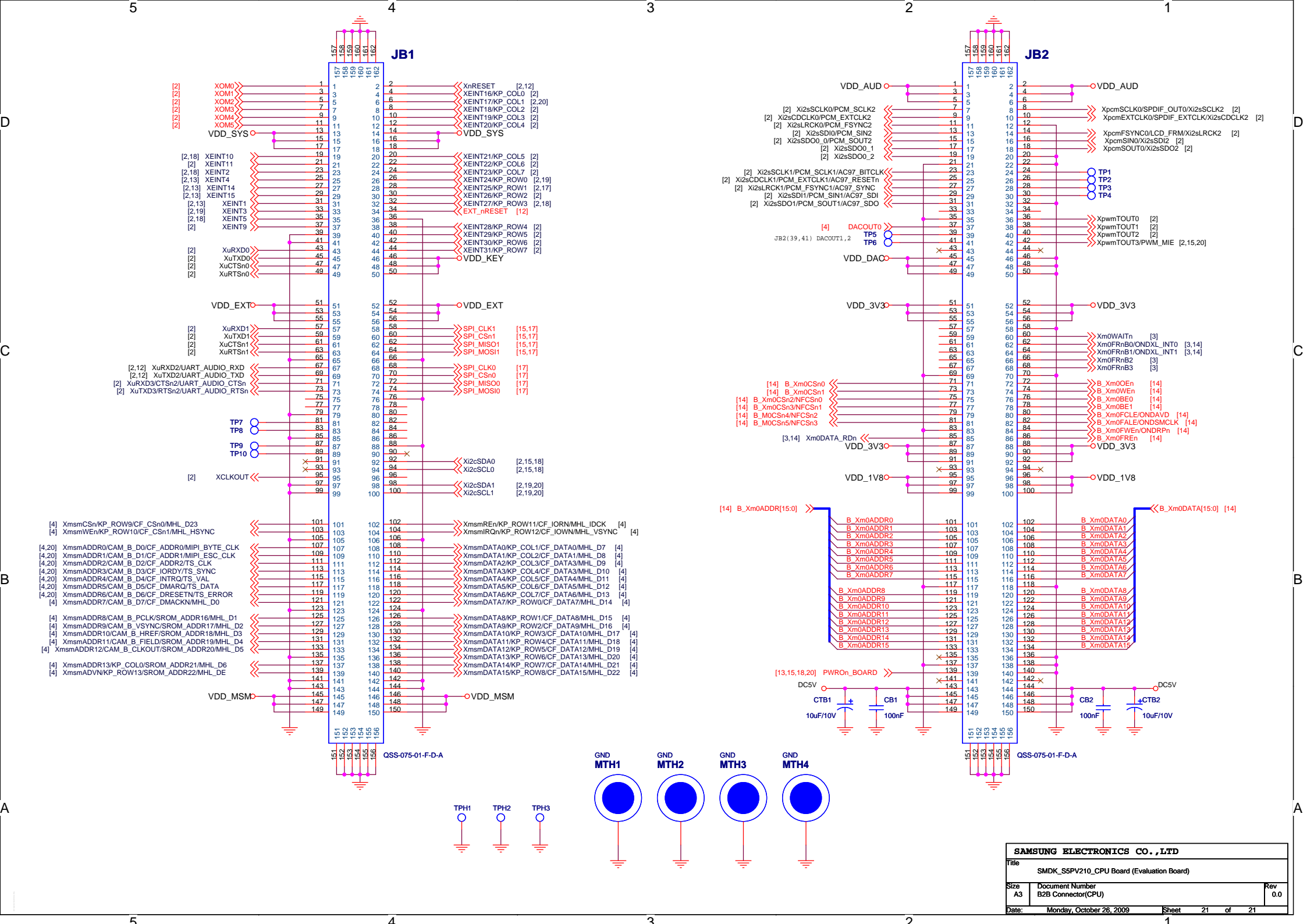


LED drivers (Common)



TP27: XmsmADDR0/CAM_B_D0/CF_ADDR0/MIPI_BYTE_CLK [4,21]
TP28: XmsmADDR1/CAM_B_D1/CF_ADDR1/MIPI_ESC_CLK [4,21]

SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK_SSPV210_CPU Board (Evaluation Board)			
Size: A3	Document Number: MIPI-DSI/TSI/24C0 IF	Rev: 0.0	
Date: Monday, October 26, 2009	Sheet: 20	of 21	

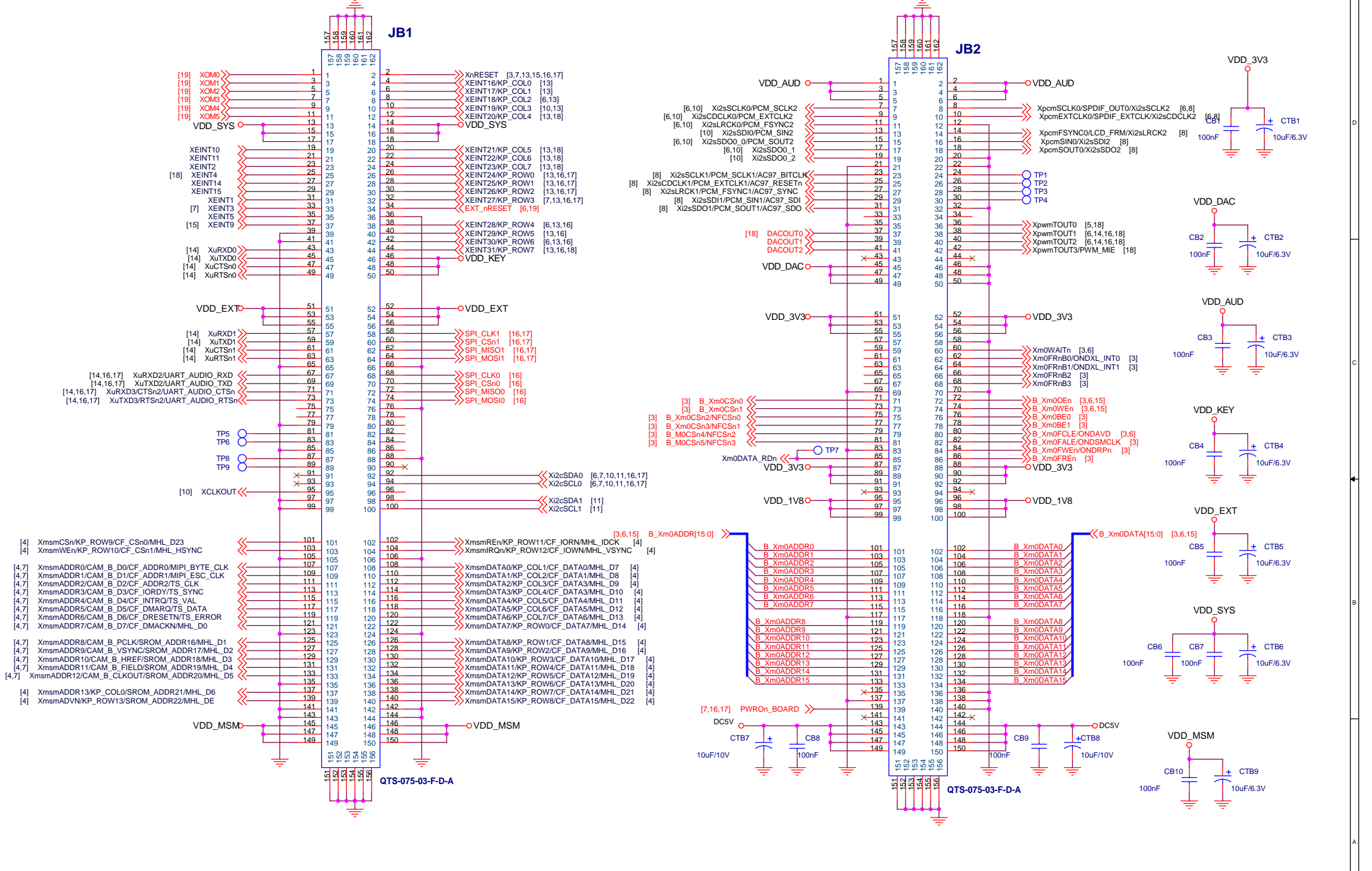


SMDK_S5PC110_Base B'd (S5PC110 Evaluation Board) Schematics

Revision	Date	Description
Rev 0.0	2009. 04.	Preliminary Version
Rev 0.1	2009. 08.	

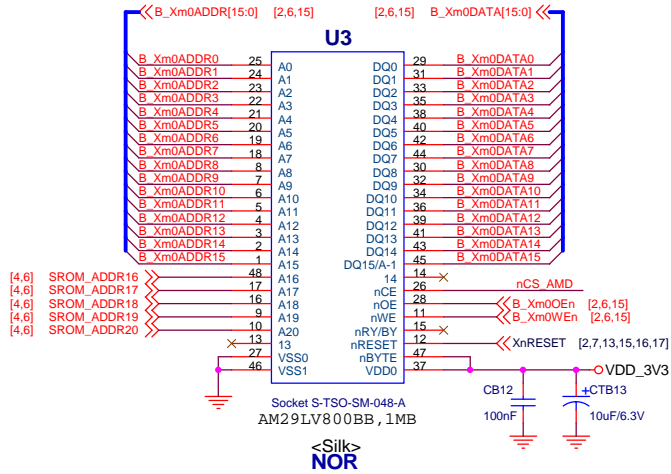
Table of Contents		Part Reference
Page	Function	<Component><Number>
01	Revision History	U : Component or Regurator IC
02	B2B Connector&power(Base Board)	C : Capacitor
03	NOR/NAND/SRAM/ChipSel	CB : Capacitor Bypass
04	CF Modem Key signal swiching	CT : Capacitor Tantal
05	Compact Flash Socket	CTB : Capacitor Tantal Bypass
06	Ext.ROM Bus/ Host_Modem IF	J : Jumper
07	Camera B-Port Interface	JB : CPU To Base connector
08	Audio Switch	JP : Jumper Power
09	Audio(WM9713_AC97)	R : Resistor
10	Audio(WM8580_IIS_5.1CH)	RA : Resistor Array
11	SPDIF OUT / IIC EEPROM Interface	RP : Resistor Power
12	Audio Jack	VR : Variable Resistor
13	External Keypad	L : Inductor
14	UART/ IrDA	FB : Ferrite Bead
15	Ethernet 100Mbps(LAN9115)	OSC : Oscillator
16	Module Connector1_2	X : X-tal (Crystal)
17	Module Connector3_4	Q : Transistor or FET
18	TV Interface/PWM/EINT/LED	D : Diode
19	RMB board interface(for SMDK b'd test)	ZD : Zener Diode
		LED : LED Diode
		SW : SWitch Tact/Push
		CON : CONnector
		CFGB : ConFiGure switch on
		Baseb'd(DIP/Slide)
		TP : Test Point (SMD)
		TPH : Test Point Hole (Through Hole)
		MTH: Mount Through Hole
		M (MOD) : MODule Interface connector

SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number Revision History	Rev 0.1
Date: Thursday, October 01, 2009	Sheet	1 of 19



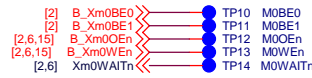
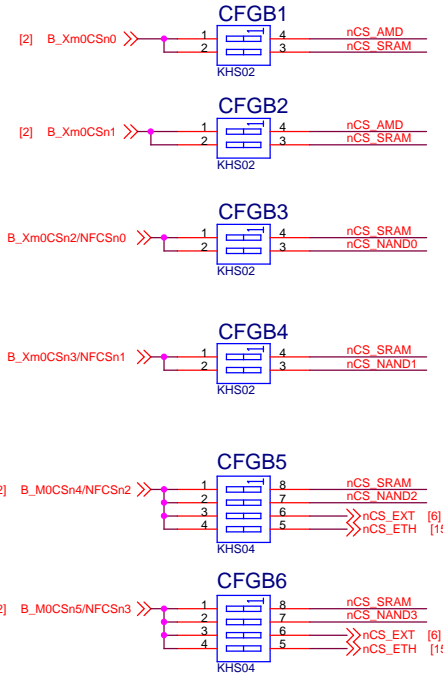
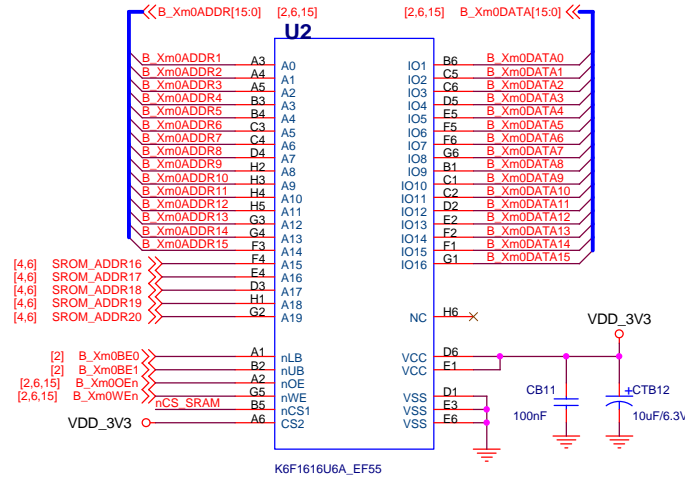
SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number B2B Connector(Base)	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 2	of 19

AMD NOR-Flash Memory (SOCKET)

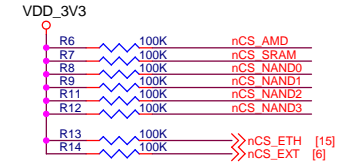
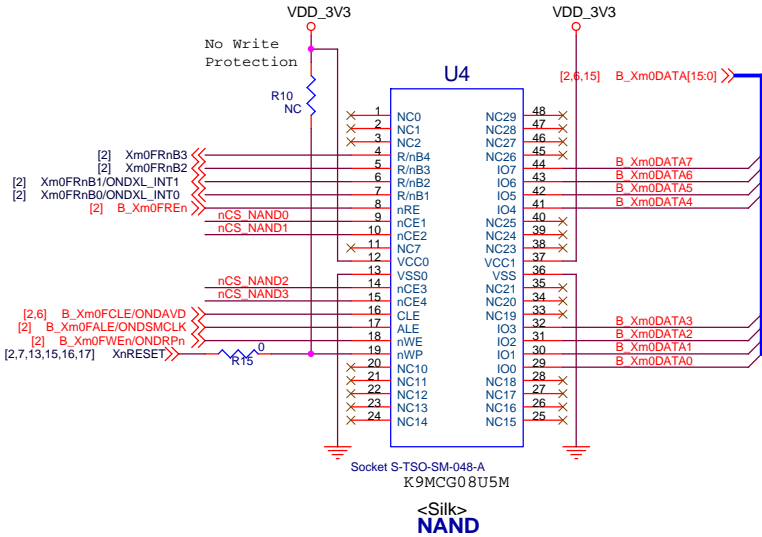


ADDR for SRAM is using byte base addressing

SRAM Memory

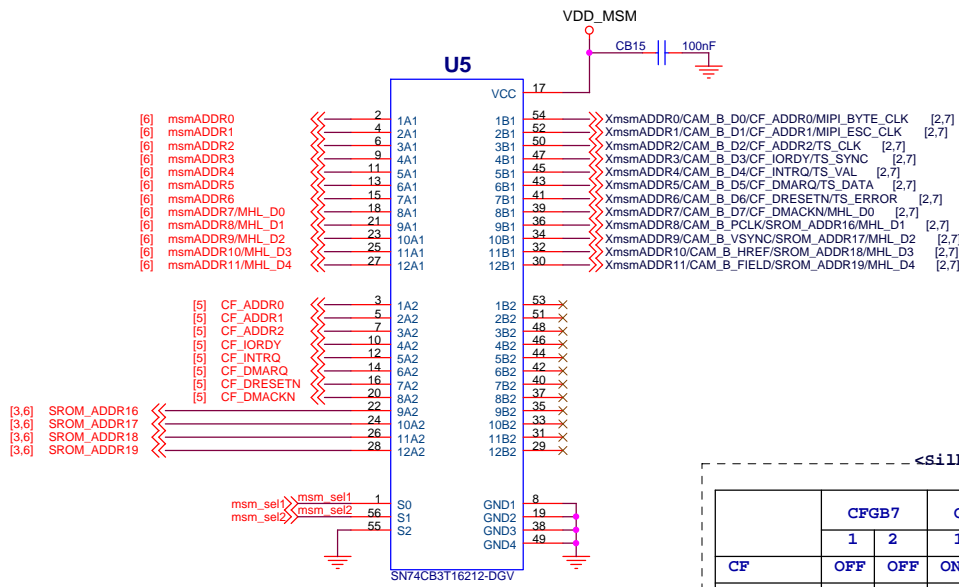


Samsung NAND-Flash memory (SOCKET)



<Silk>

CFGB1:nCS0	CFGB2:nCS1	CFGB5:nCS4
[2] SRAM	[1] NOR	[4] Ethernet
		[3] External
		[2] NAND CS2
		[1] SRAM
CFGB3:nCS2		
[2] NAND CS0		
[1] SRAM		
CFGB4:nCS3		
[2] NAND CS1		
[1] SRAM		
		CFGB6:nCS5
		[4] Ethernet
		[3] External
		[2] NAND CS3
		[1] SRAM

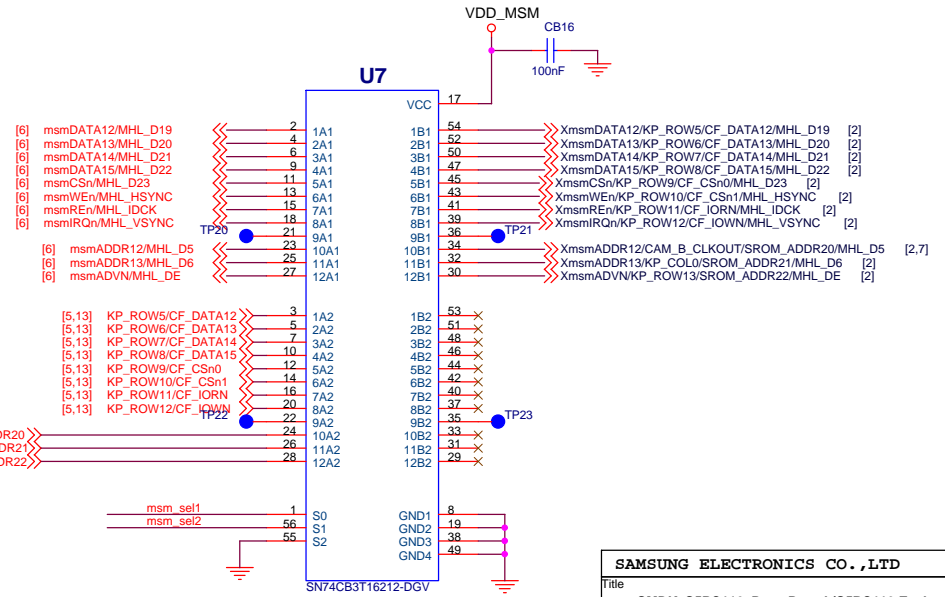
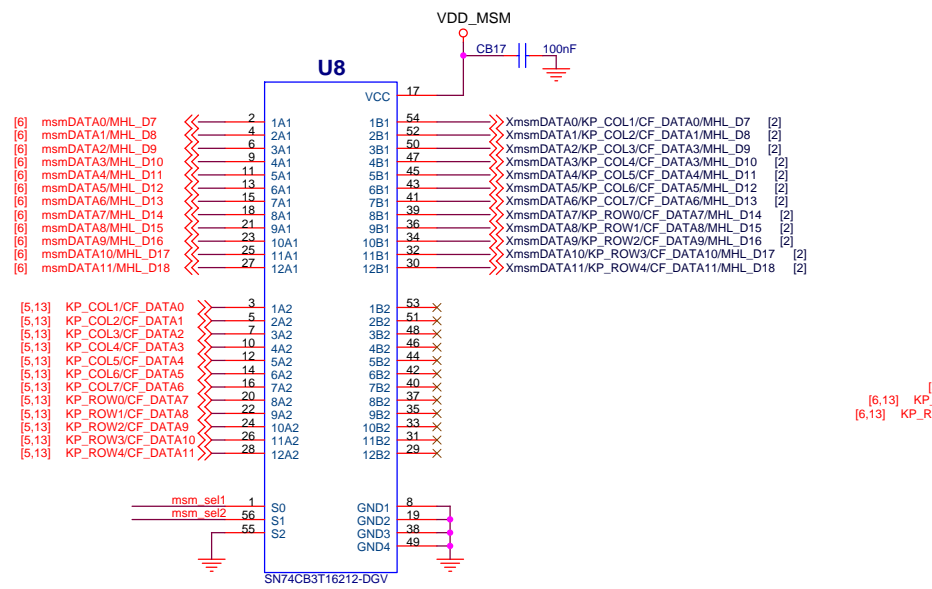
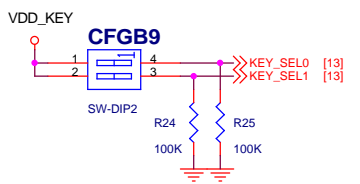
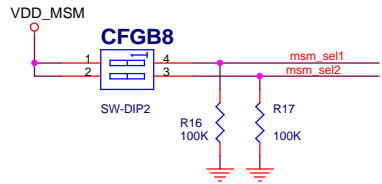
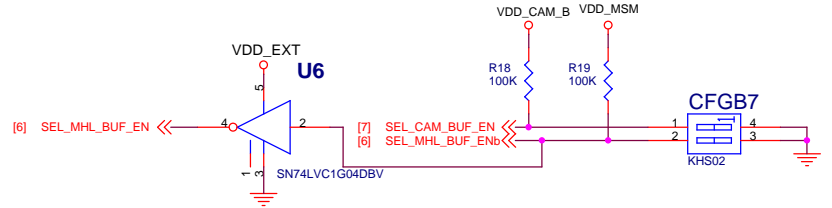


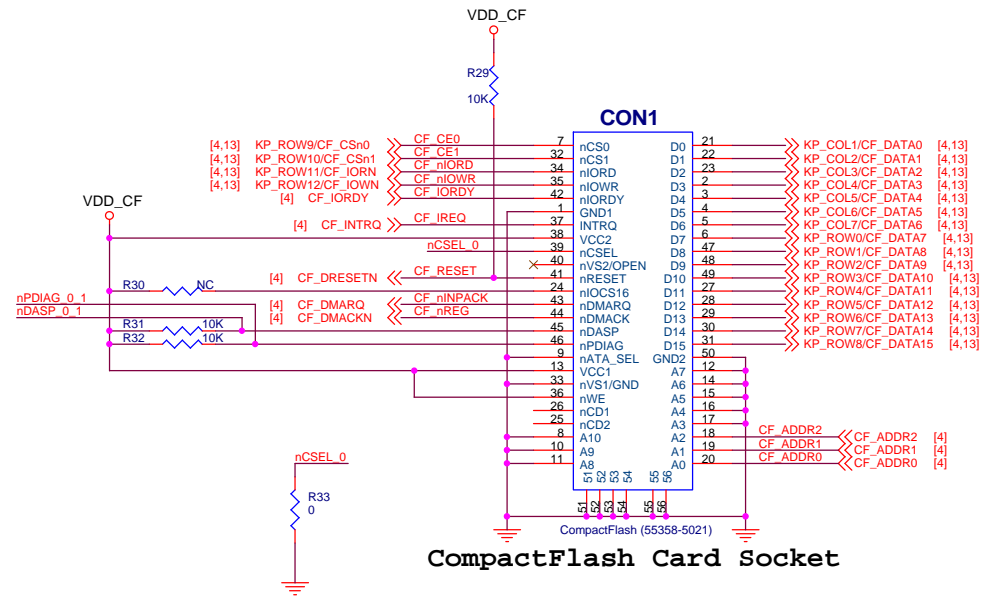
<silks>

	CFGB7		CFGB8		CFGB9	
	1	2	1	2	1	2
CF	OFF	OFF	ON	ON	OFF	OFF
SROM	OFF	OFF	ON	ON	OFF	OFF
MHL	OFF	ON	ON	OFF	OFF	OFF
MSM	OFF	OFF	ON	OFF	OFF	OFF
CAM	ON	OFF	OFF	OFF	OFF	OFF
KEY (MSM)	OFF	OFF	ON	ON	ON	ON
KEY (INT)					ON	OFF

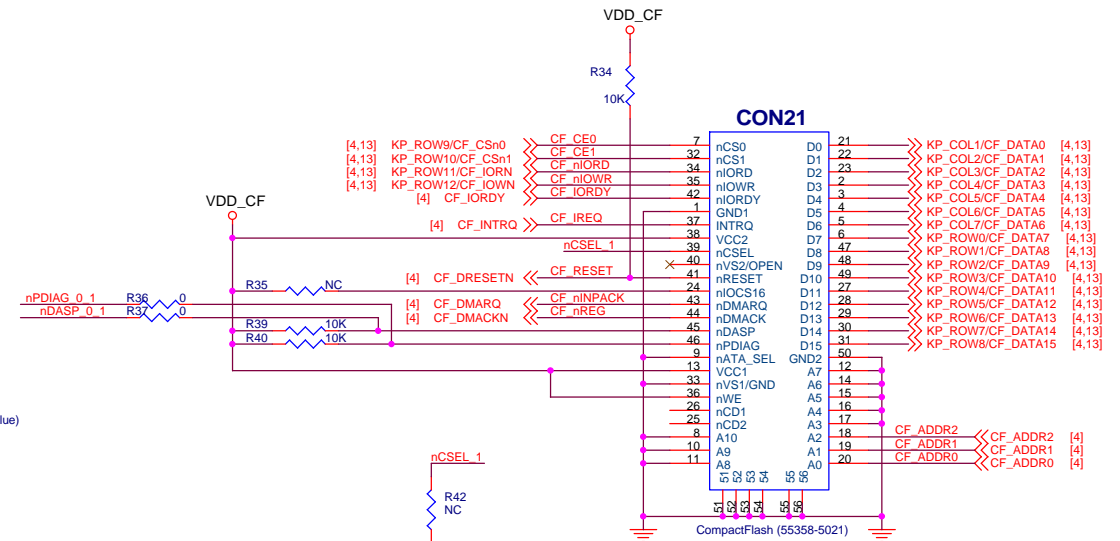
*KEY(MSM) case: Remove CF card & don't access SROM.
 *To use MSM,CAM,CF, CFG3.1 on CPU b'd should be OFF.

S2	S1	S0	
L	L	L	Disconnect
L	L	H	A1 = B1
L	H	H	A2 = B1

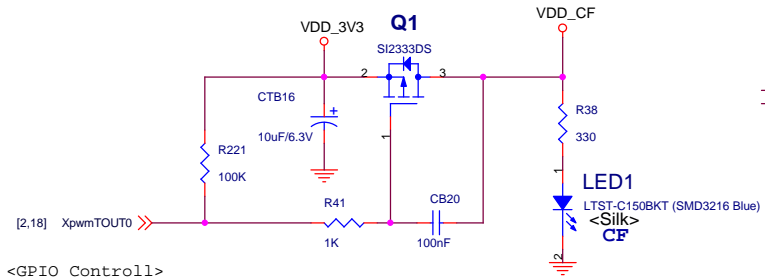
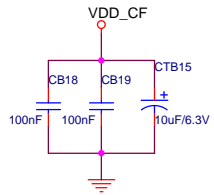




CompactFlash Card Socket

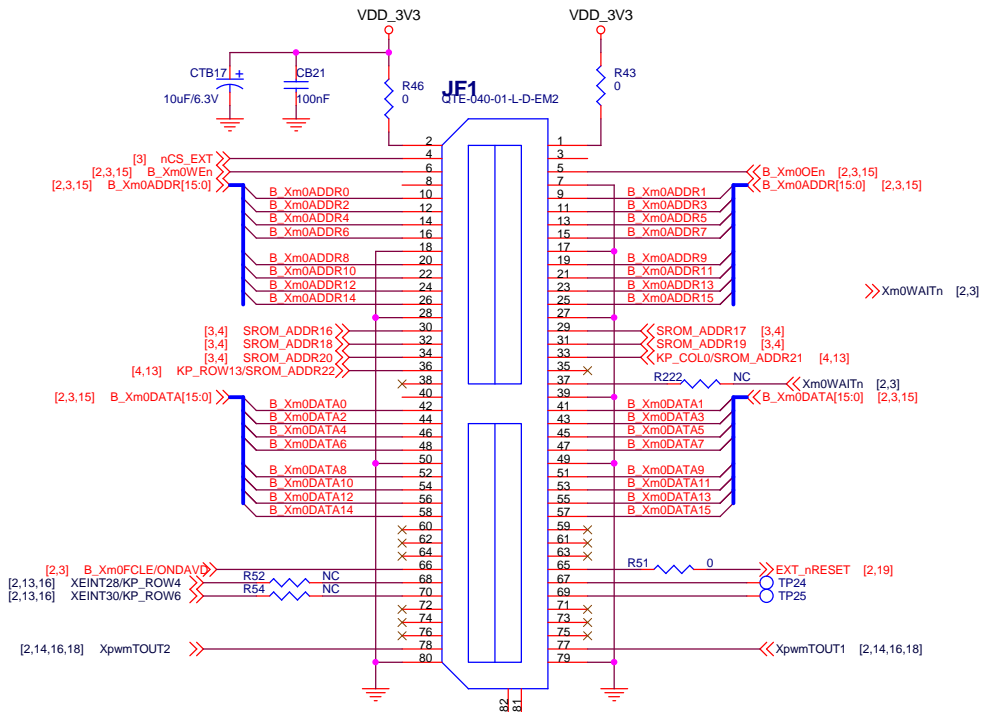


CompactFlash Card Socket

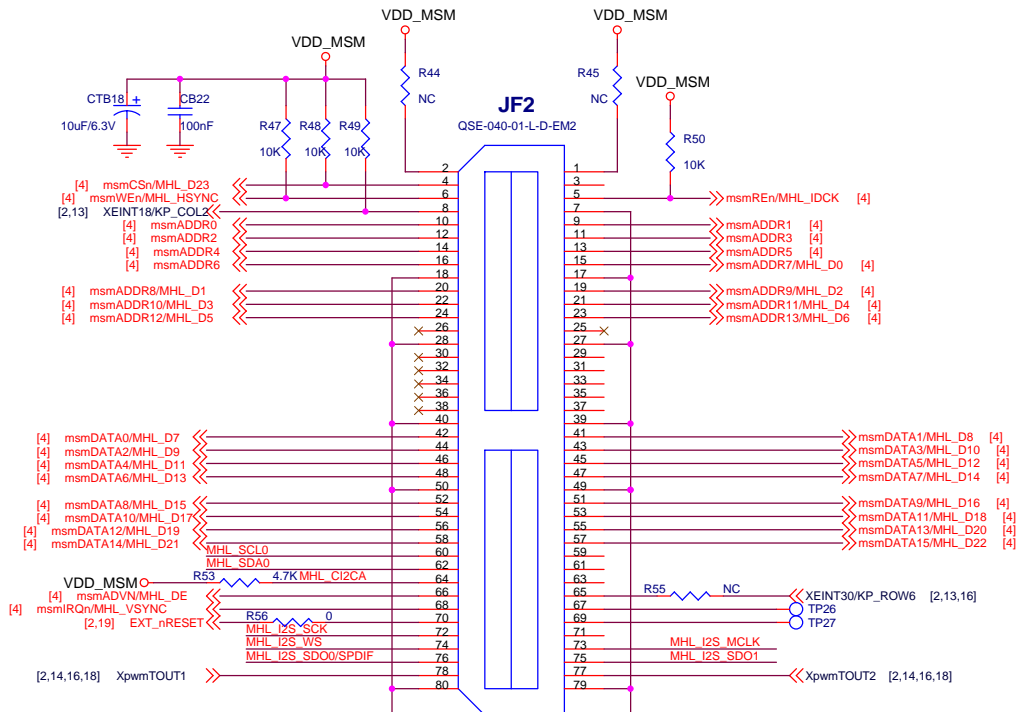


<GPIO Control>
 ON : Low
 OFF : Input & Pull up disable

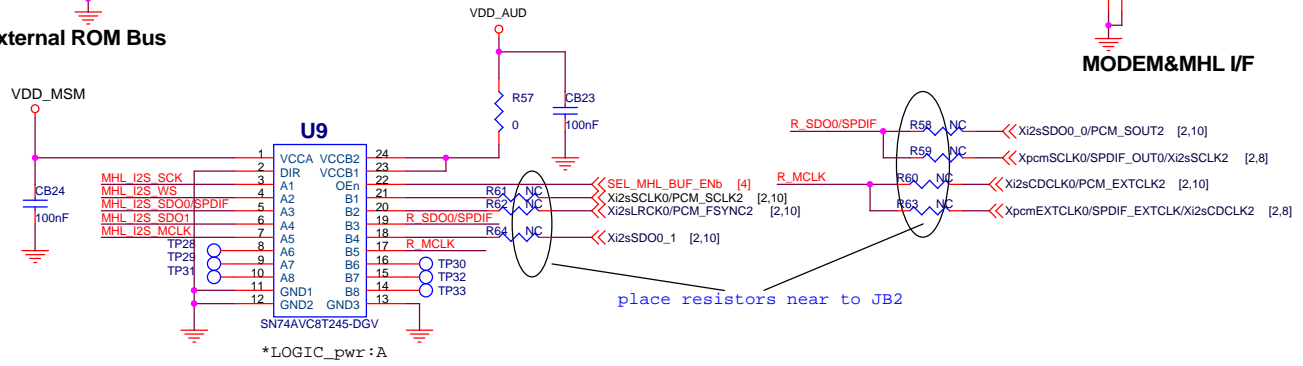
SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number Compact Flash Card Socket	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 5	of 19



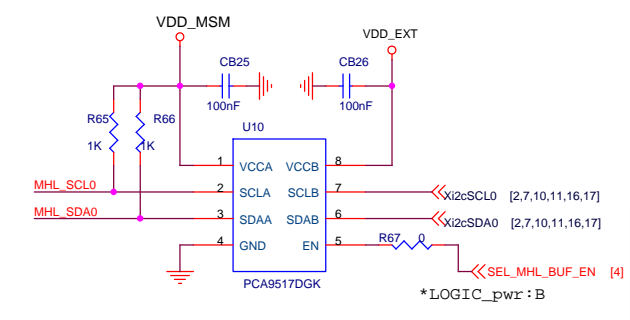
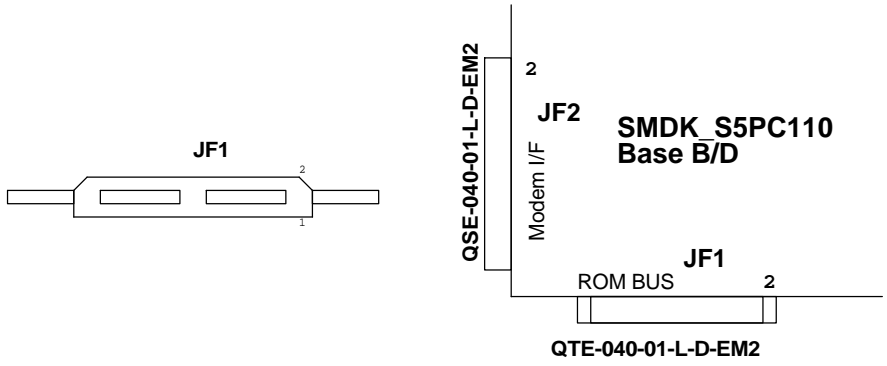
External ROM Bus



MODEM&MHL I/F

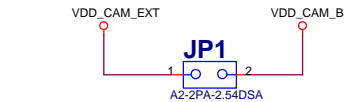
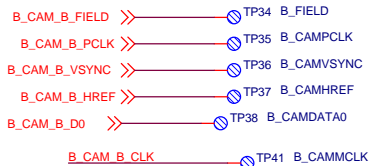
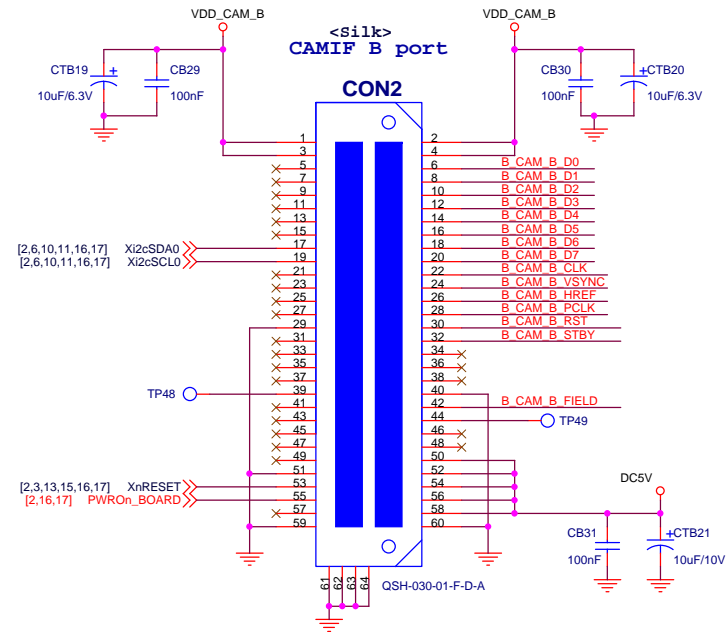


place resistors near to JB2



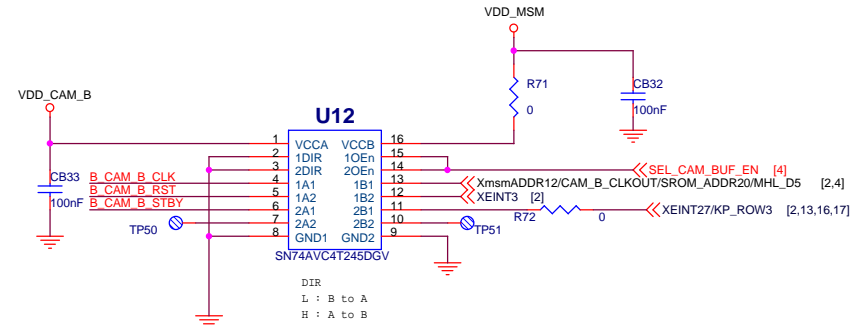
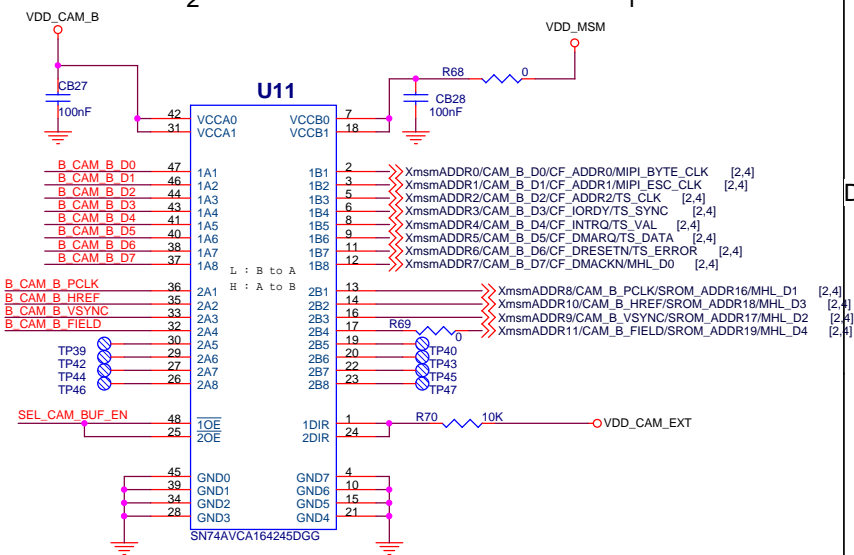
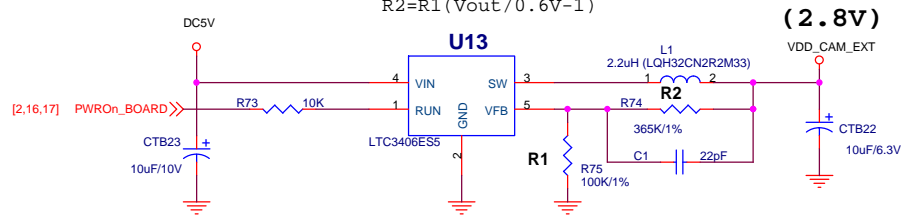
SAMSUNG ELECTRONICS CO., LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number Ext. ROM Bus/ Host_Modem I/F/MHL	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 6	of 19

CAM B

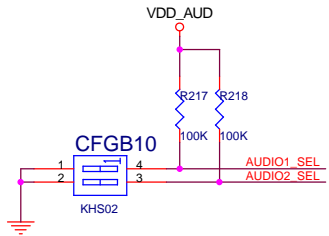


$$V_{out} = 0.6(1 + R2/R1)$$

$$R2 = R1(V_{out}/0.6V - 1)$$

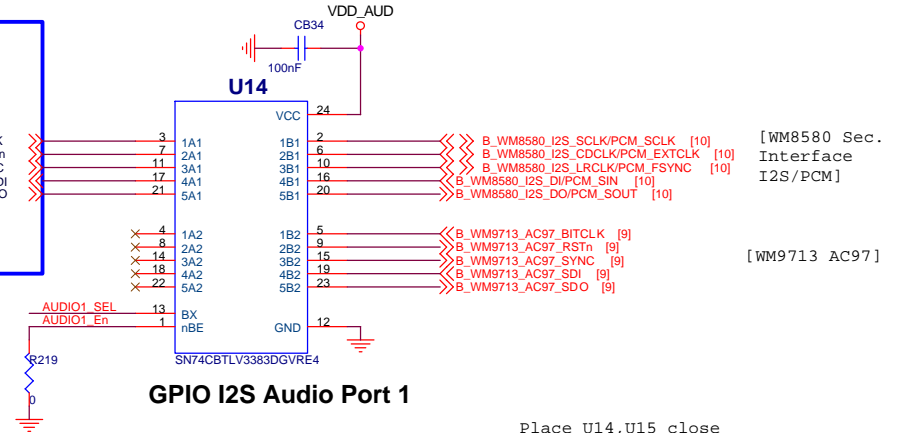
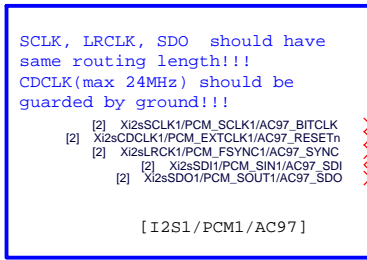


SAMSUNG ELECTRONICS CO.,LTD		
Title	SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)	
Size	Document Number	Rev
A3	Camera I/F B Port	0.1
Date:	Thursday, October 01, 2009	Sheet 7 of 19

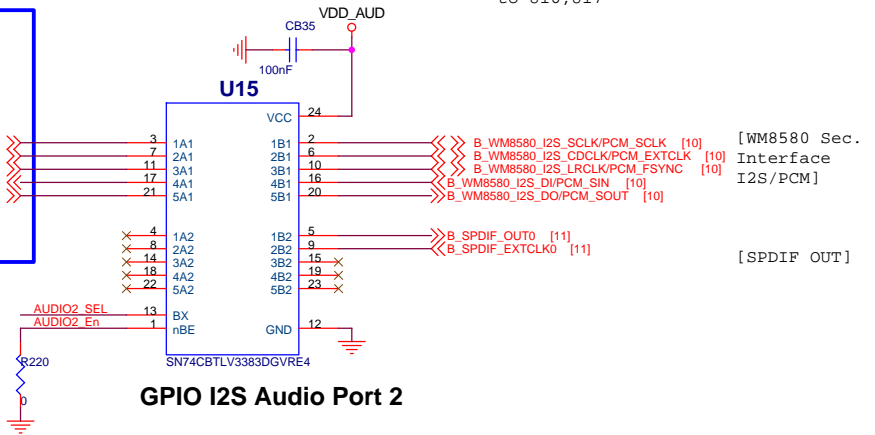
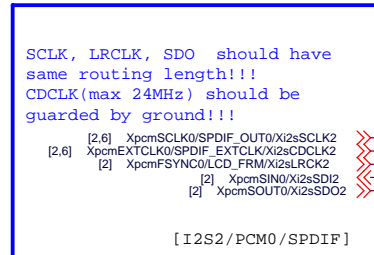


<Silk>

CFBG10	[1]	[2]
Off	Audio1: WM9713 AC97	Audio2: SPDIF OUT
On	Audio1: WM8580 IIS/PCM	Audio2: WM8580 IIS/PCM



Place U14,U15 close to U16,U17



SCLK, LRCLK, SDO should have same routing length!!!
CDCLK(max 24MHz) should be guarded by ground!!!

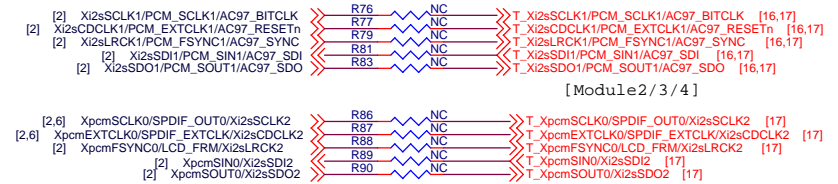


[I2S0/PCM2]

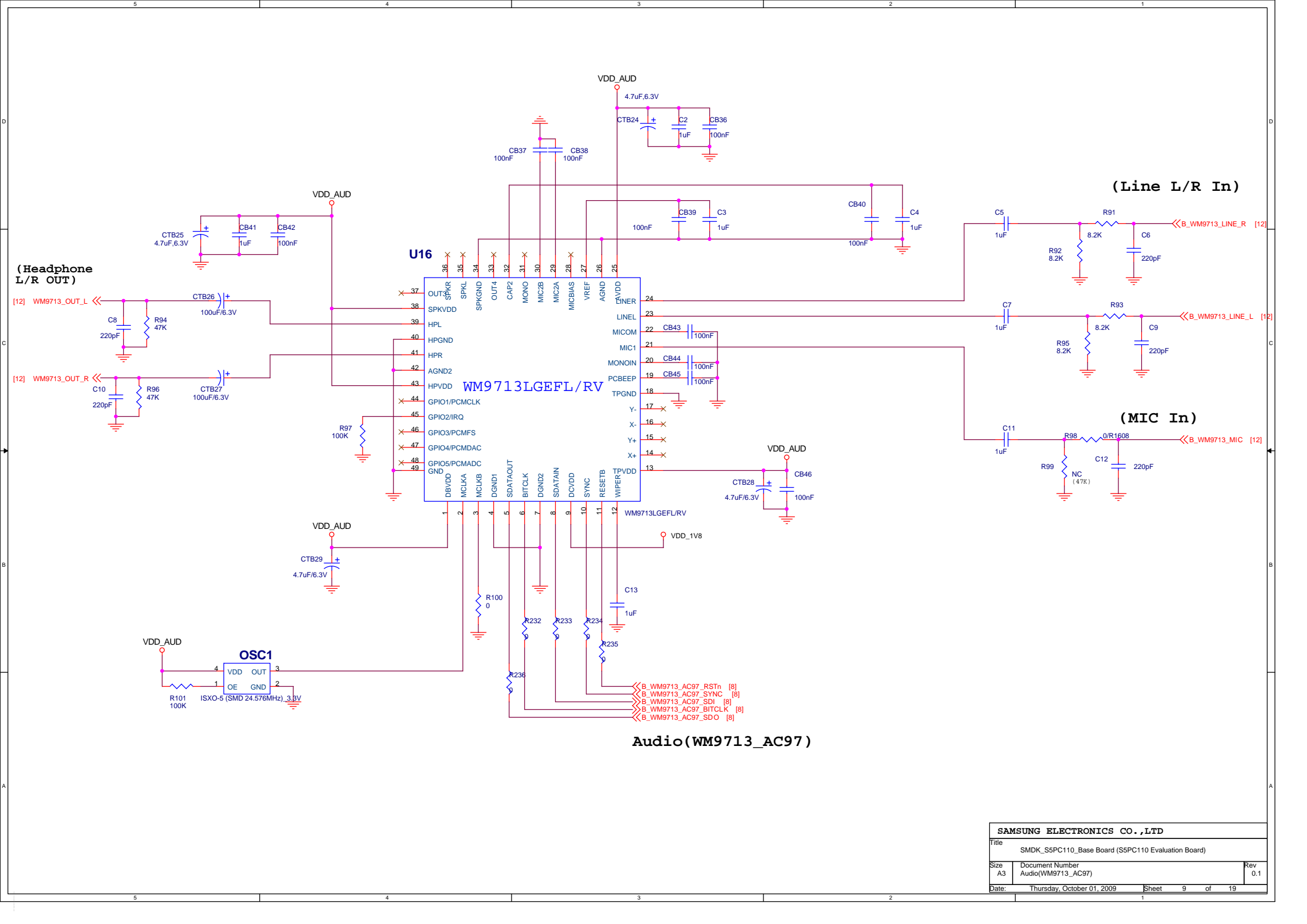
GPIO I2S Audio Port 0

[WM8580 Pri I2S/PCM]

[For isolate purpose only] - Since these are shared with other module



place resistors near to JB2

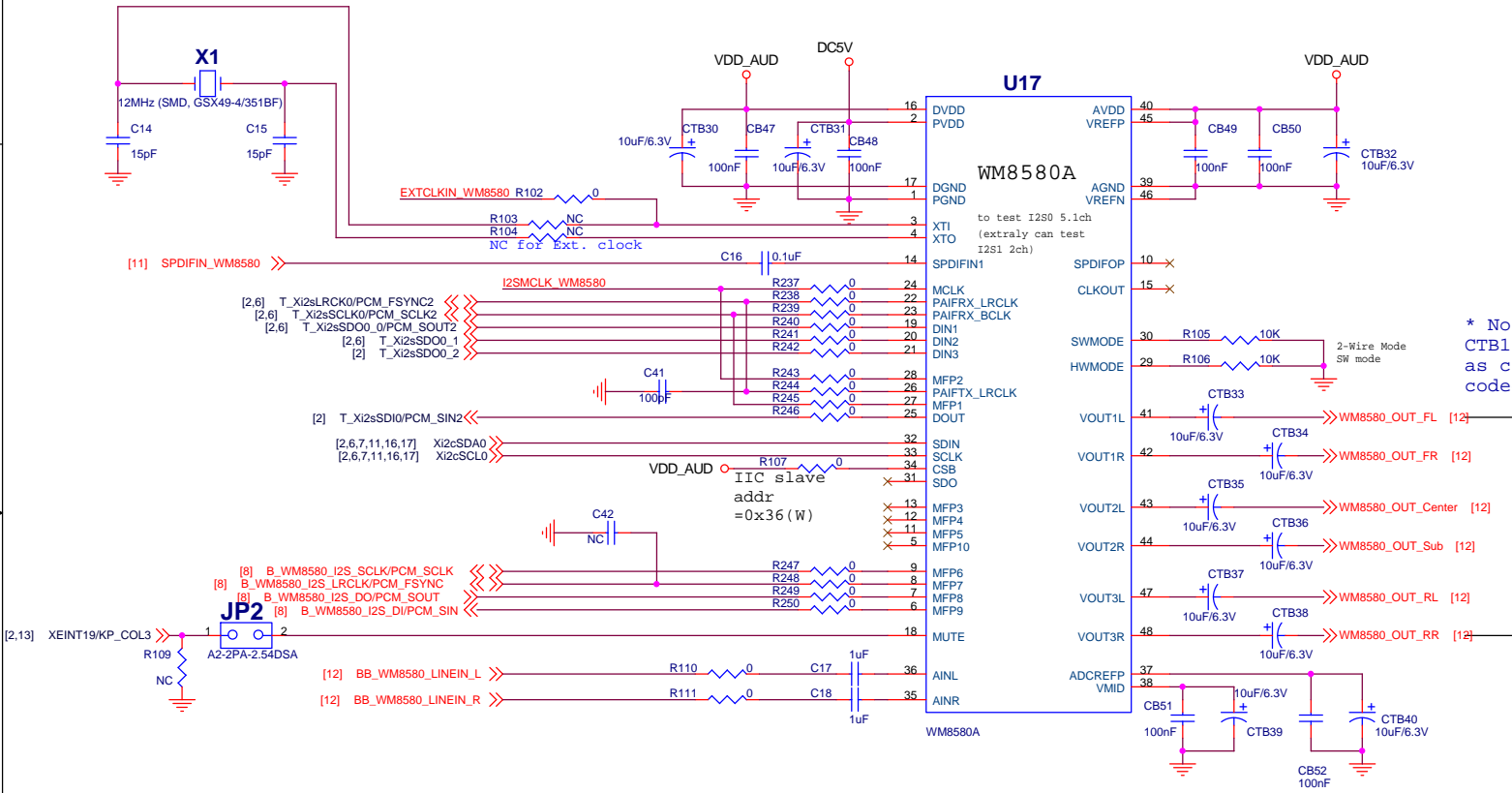


Audio(WM9713_AC97)

SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number Audio(WM9713_AC97)	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 9	of 19

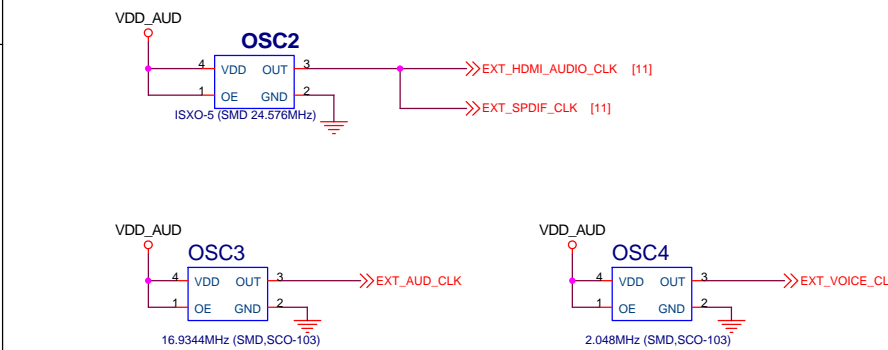
Audio(WM8580_PCM/IIS & 5.1CH)

Manufacturer : Gollodge
 Description : SM Crystal 12pF
 Package : HC49-4H SMD
 (12.9 x 4.8 x 4.3 mm)

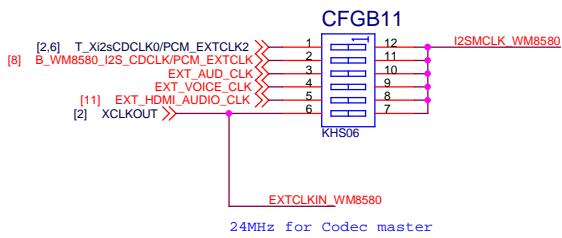


* Note:
 CTB19 ~ 24 should be placed
 as close as possible to the
 codec chip

**MultiCh.
 L/R Audio
 OUT**

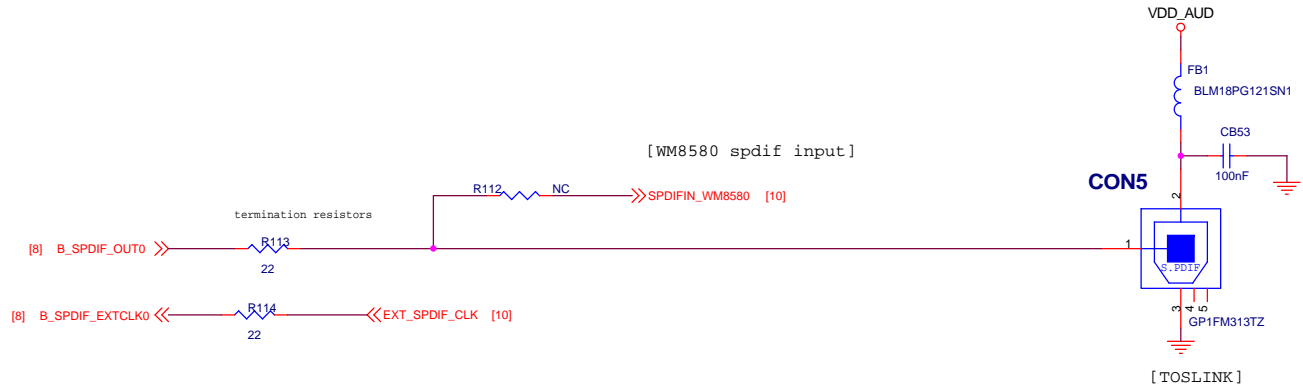


WM8580 MasterCLK Selection



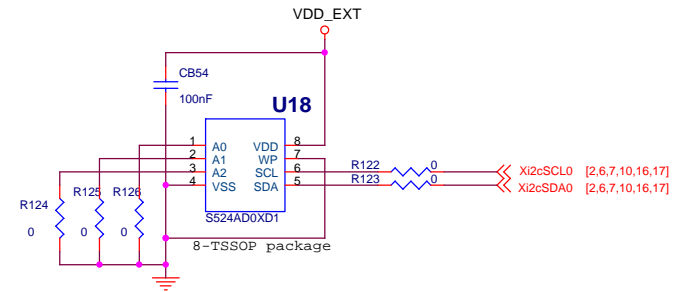
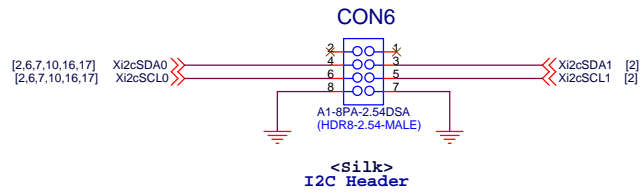
<Silk>

CFGB11	AUDIO MCLK SEL
[1]	I2S0 CDCLK
[2]	I2S1,2 CDCLK
[3]	External CLK
[4]	Voice Ext. CLK
[5]	HDMI Audio ExtCLK
[6]	AP_CLKOUTtoXTI



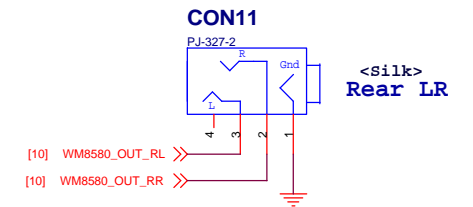
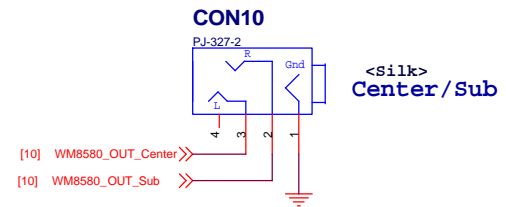
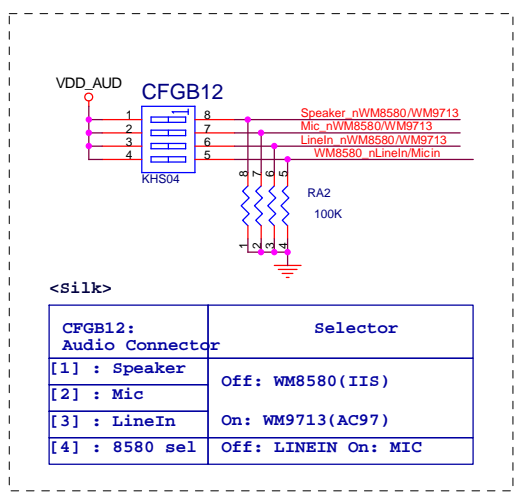
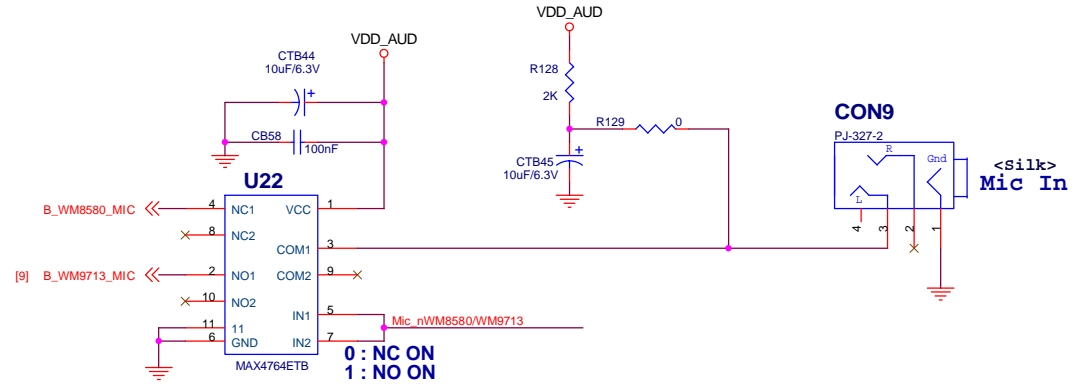
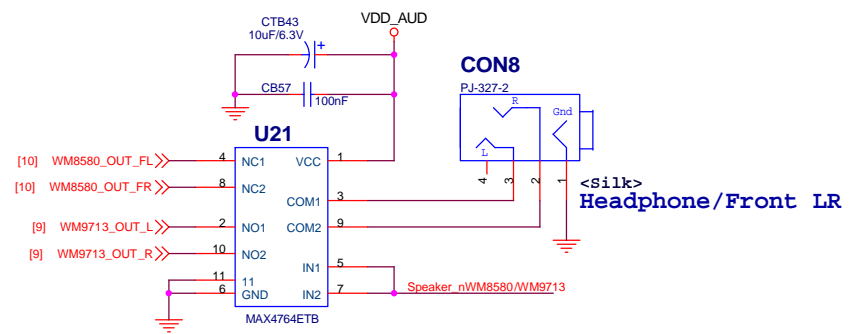
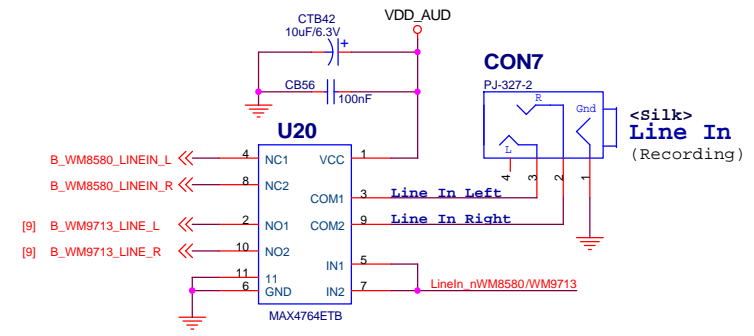
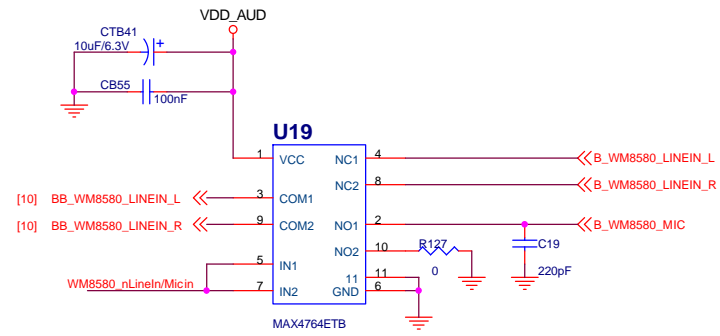
S/PDIF Audio Out

For Multi_Master I2C



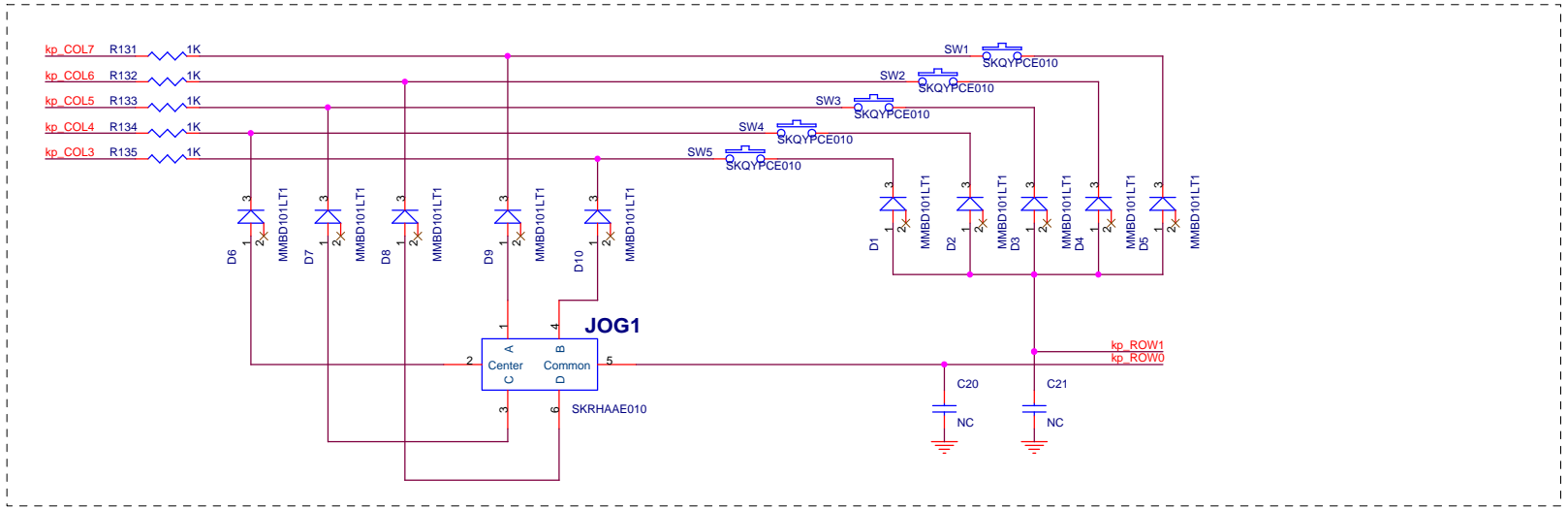
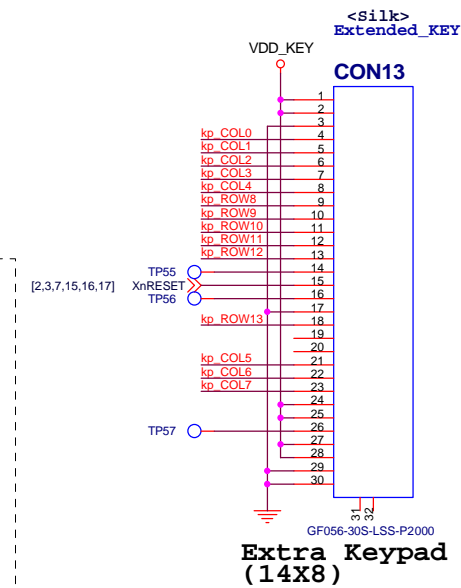
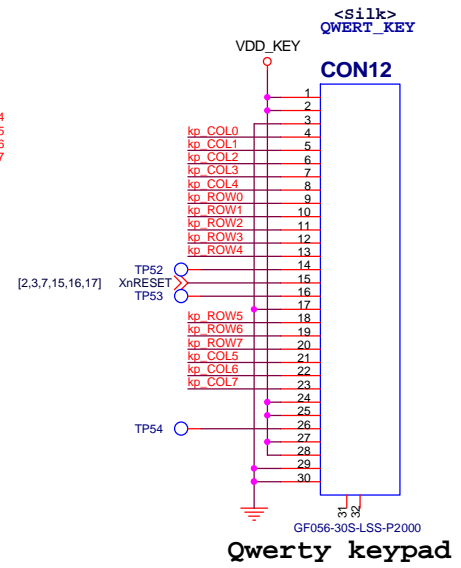
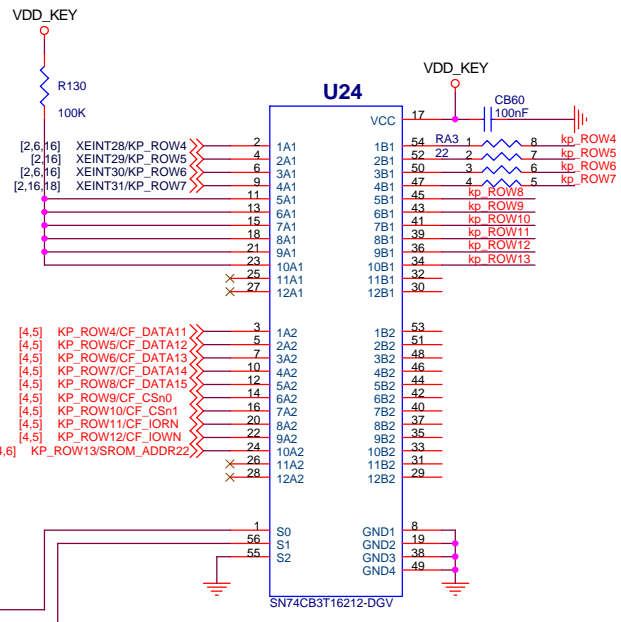
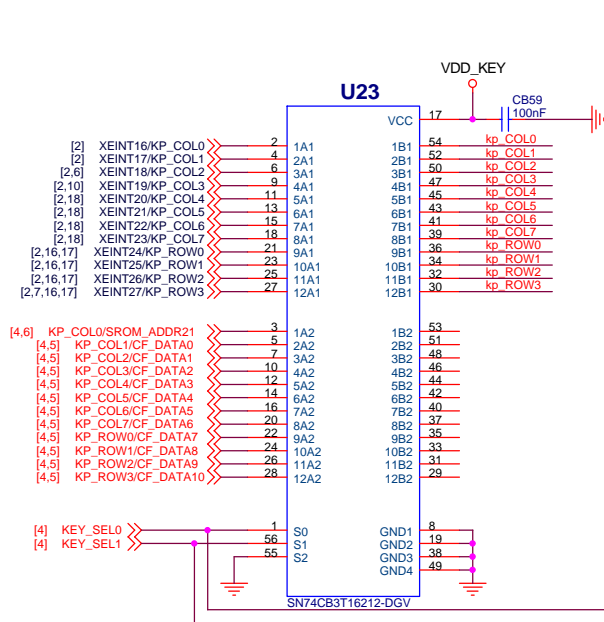
IIC E2PROM

SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number SPDIF Out / IIC EEPROM	Rev 0.1
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<Silk>

CFGB12: Audio Connector	Selector
[1] : Speaker	Off: WM8580 (IIS)
[2] : Mic	On: WM9713 (AC97)
[3] : LineIn	Off: LINEIN On: MIC
[4] : 8580 sel	

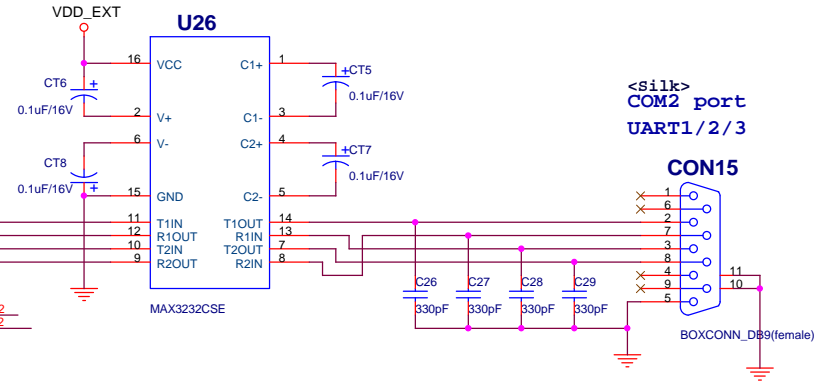
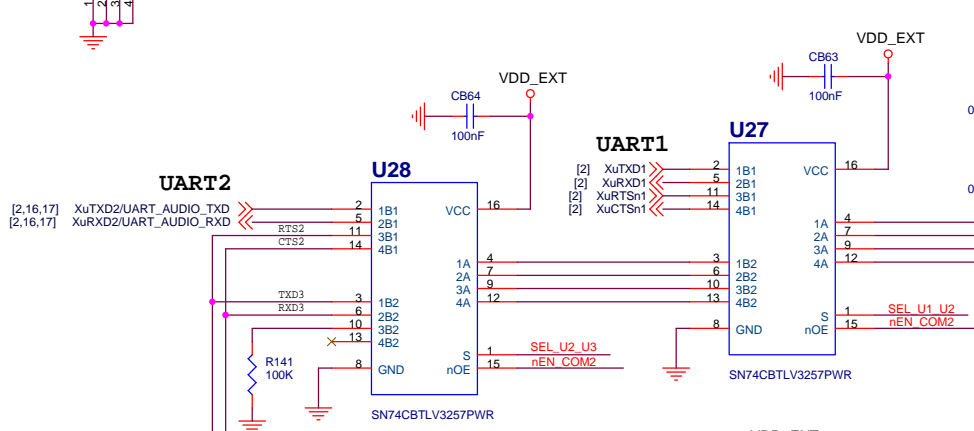
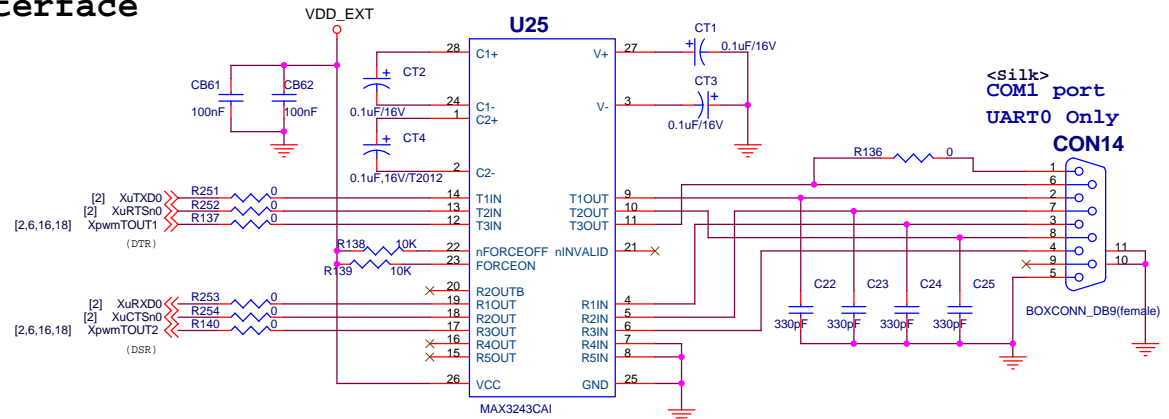
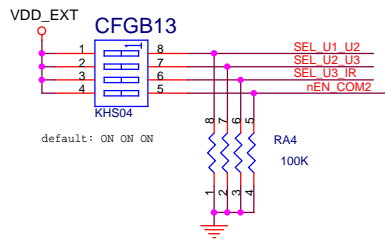


SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size: A3	Document Number: External Keypad	Rev: 0.1
Date: Thursday, October 01, 2009	Sheet: 13	of 19

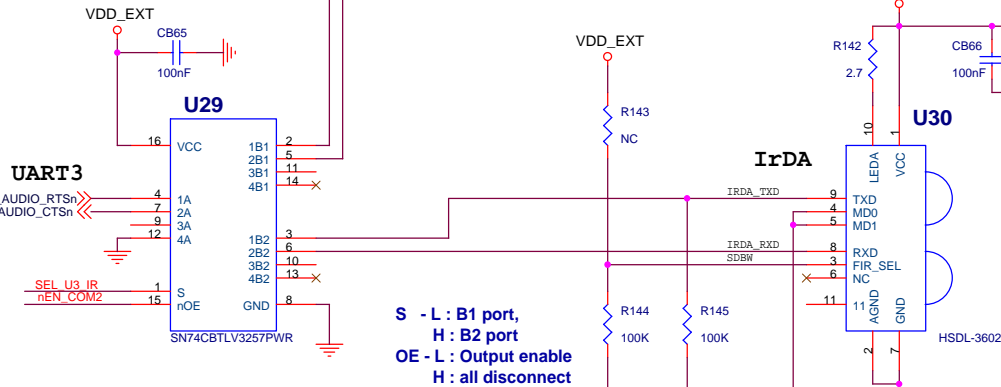
UART / IrDA Interface

<Silk>

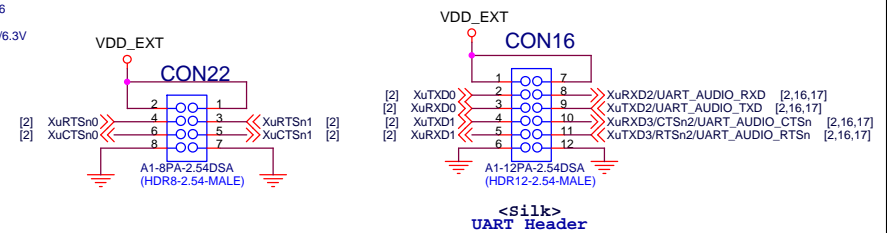
CFGB13:COM2	PIN1	PIN2	PIN3	PIN4
UART1	OFF	X	X	OFF
UART2	ON	OFF	X	OFF
UART3	ON	ON	OFF	OFF
IrDA (U2)	X	X	ON	OFF



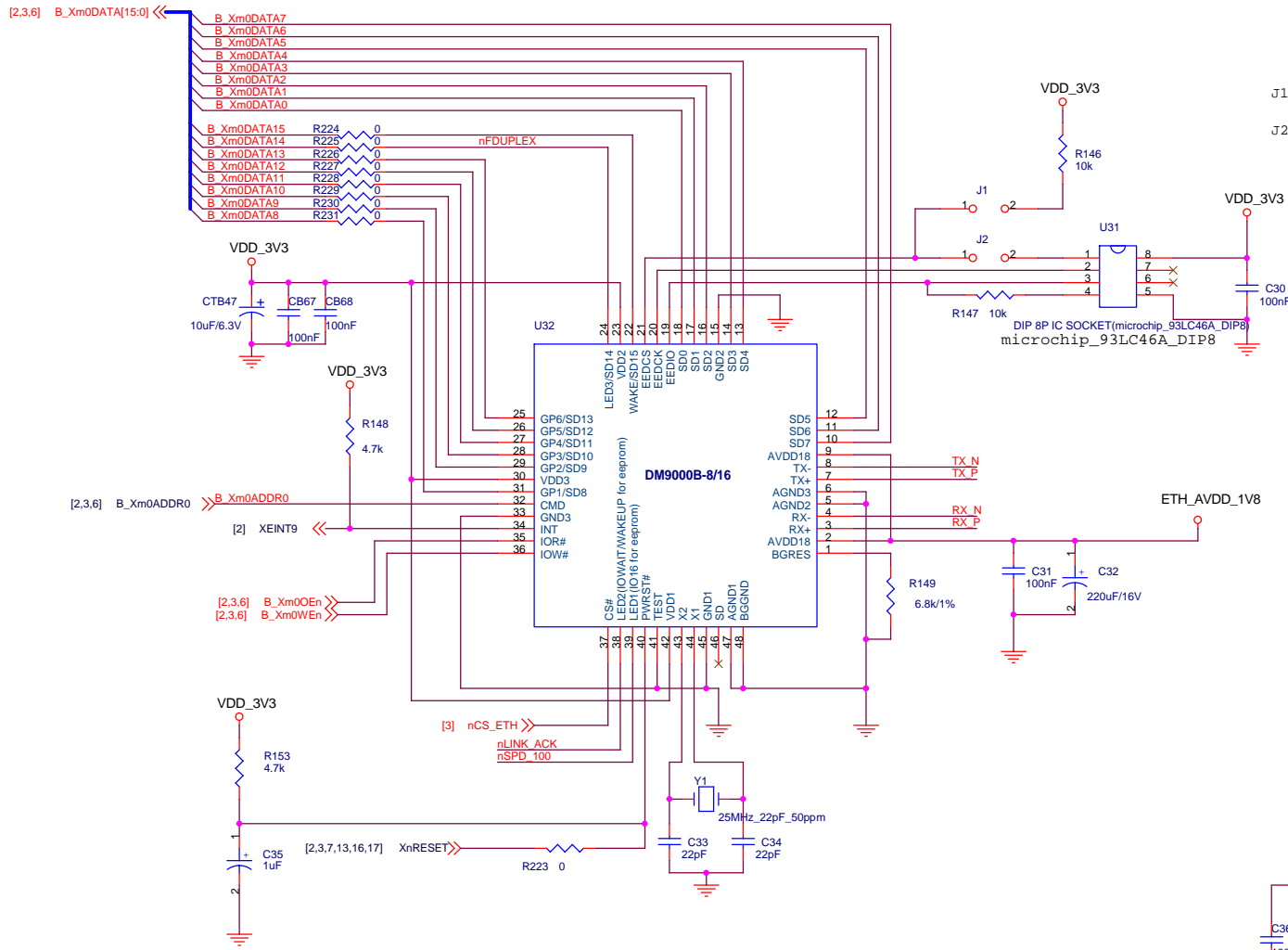
UART Header for High speed Test



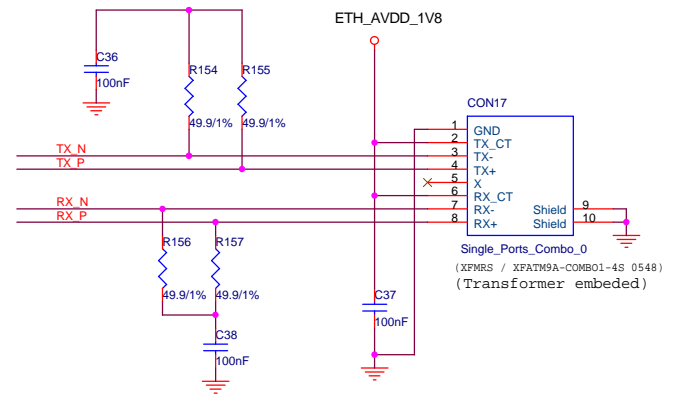
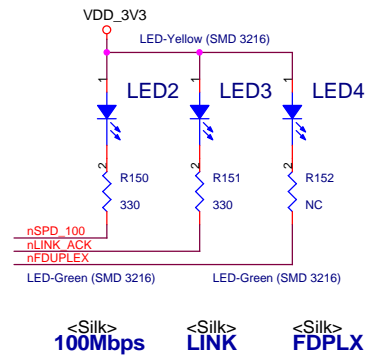
**S - L : B1 port,
H : B2 port
OE - L : Output enable
H : all disconnect**



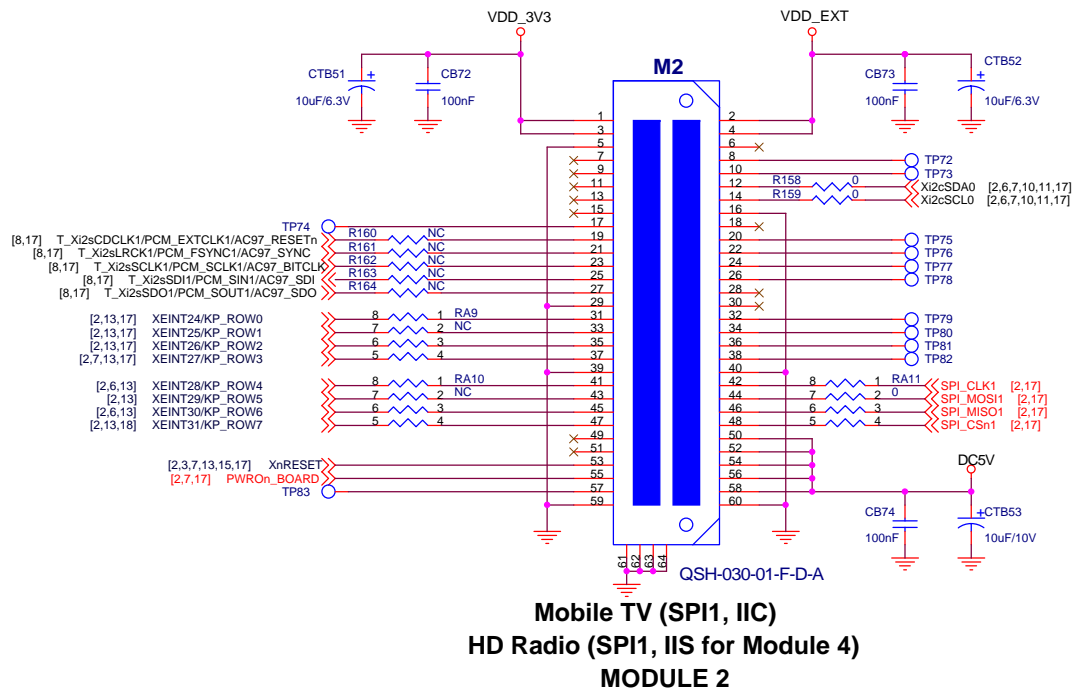
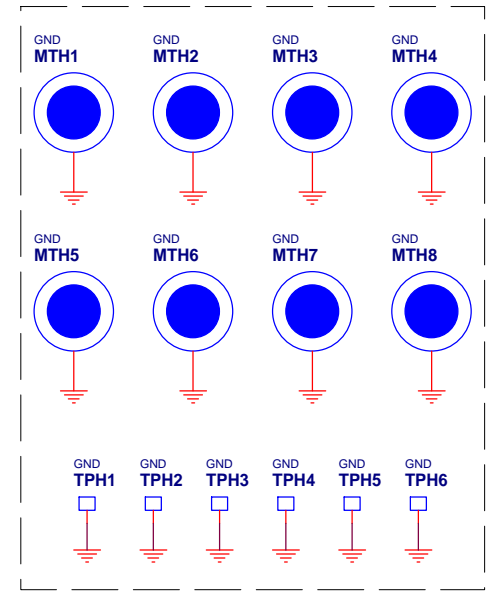
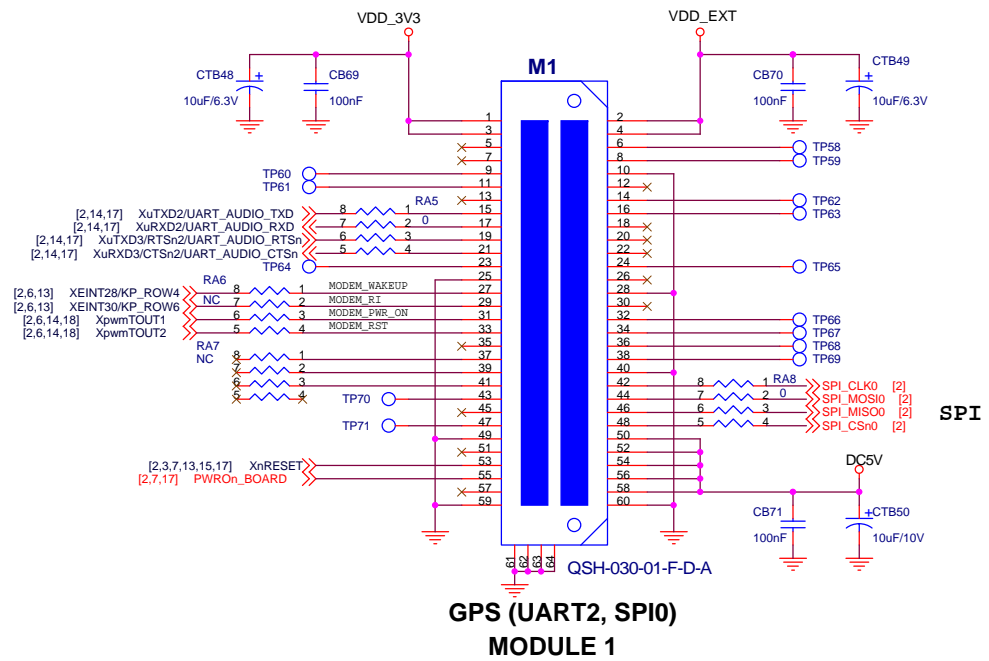
SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number UART/IrDA	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 14	of 19



J1 - ON : Use 8bit mode(&remove r224-r231)
 OFF : Use 16bit mode(&mount r224-r231&removeR152)
 J2 - ON : Use EEPROM
 OFF : Not Use EEPROM



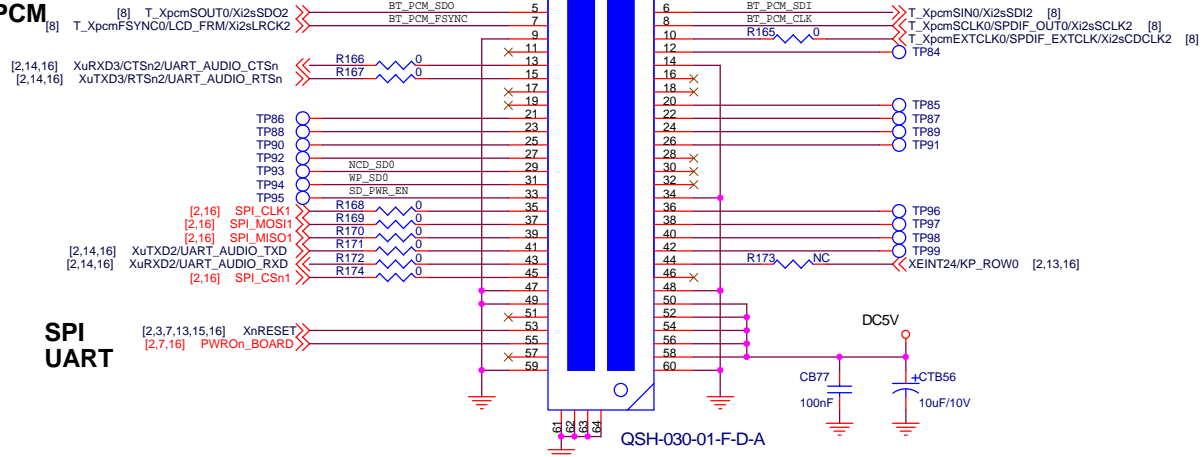
SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number Ethernet 100Mbps(DM9000)	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 15	of 19



SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number Module Connector1&2	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 16	of 19

Disable audio part MUXs using this module

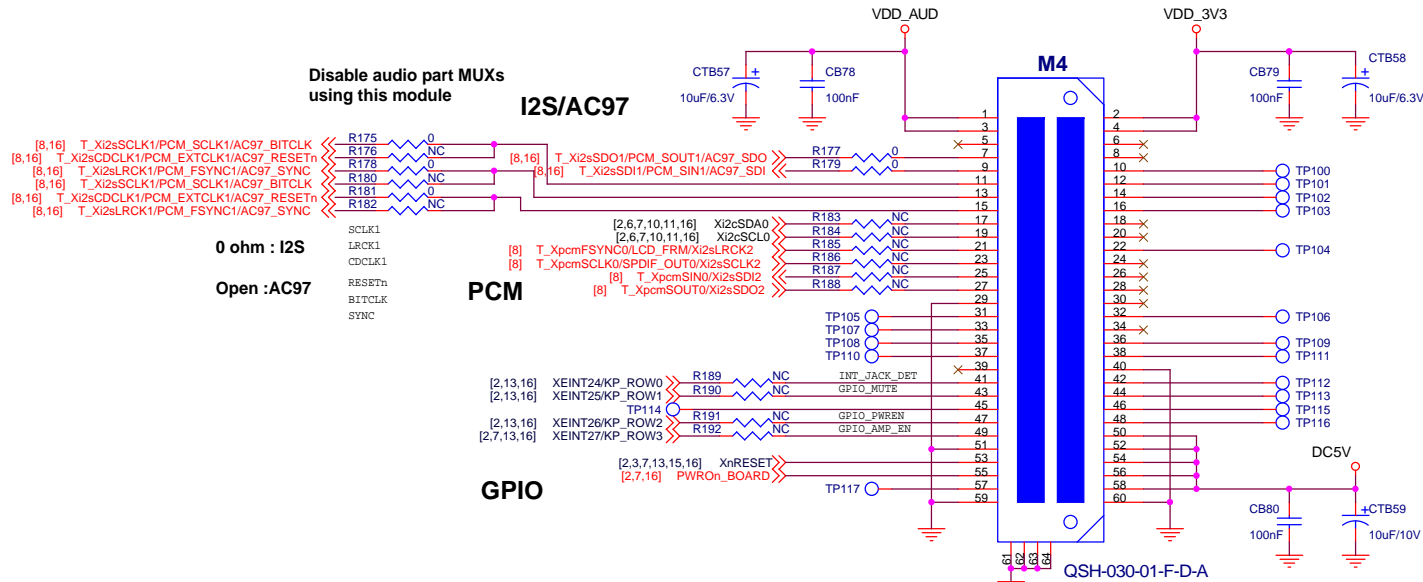
PCM



BT (UART2, PCM) MODULE 3

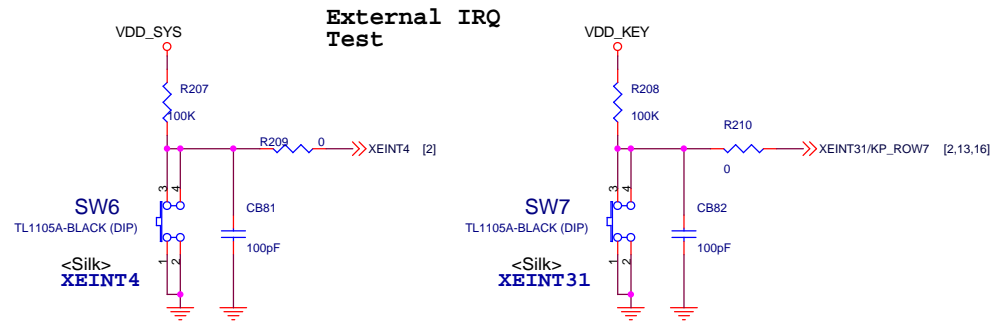
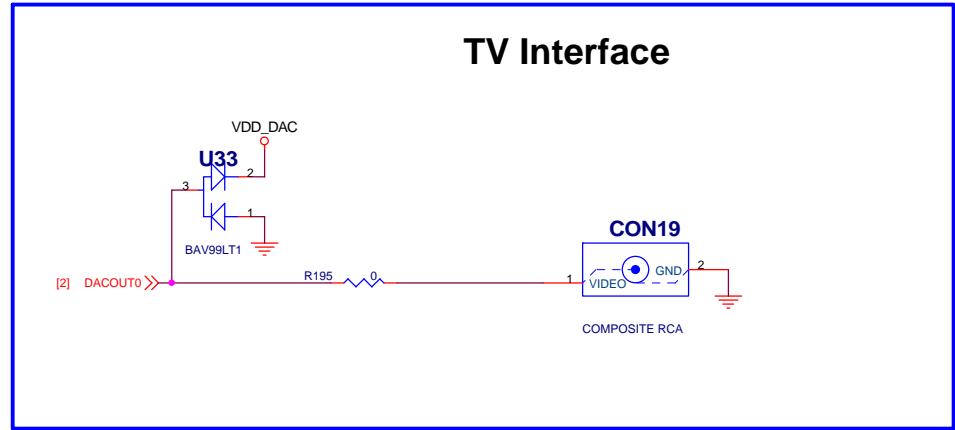
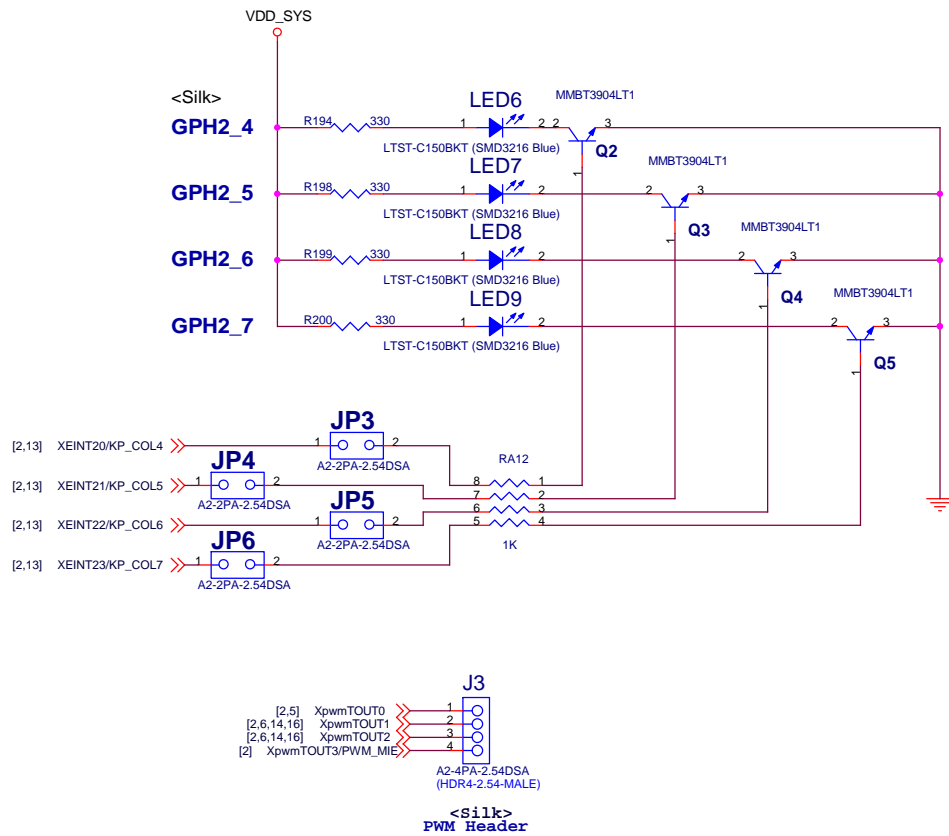
Disable audio part MUXs using this module

I2S/AC97

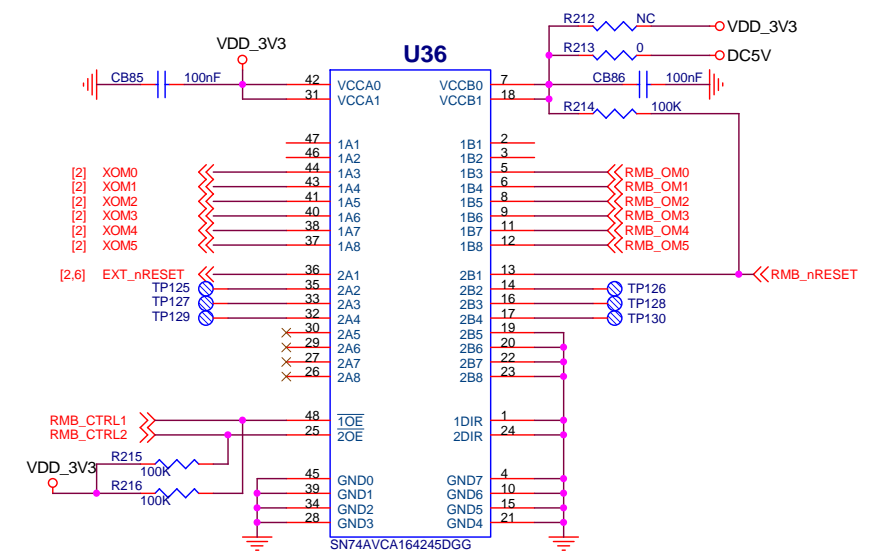
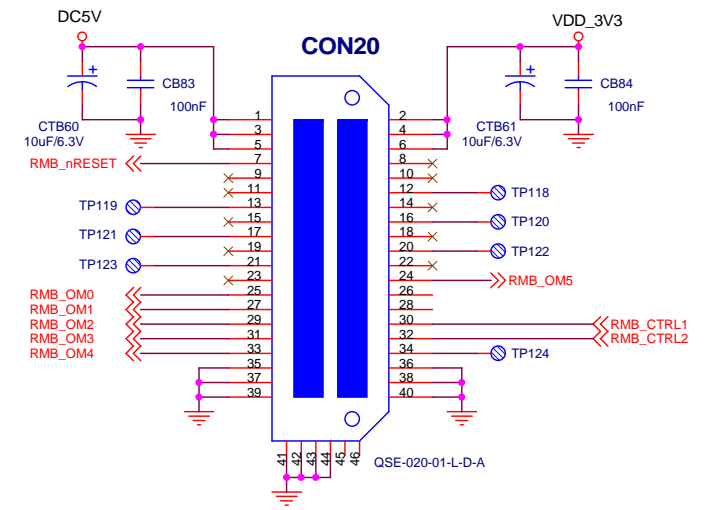


Audio (AC97, IIS, IIC) MODULE 4

SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number Module Connector3&4	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 17	of 19



SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size A3	Document Number TV Interface/ PWM/ LED/ EINT	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 18	of 19



For RMB Board I/F Connector

SAMSUNG ELECTRONICS CO.,LTD		
Title		
SMDK_S5PC110_Base Board (S5PC110 Evaluation Board)		
Size	Document Number	Rev
B	RMB b'd I/F(for SMDK b'd test)	0.1
Date:	Thursday, October 01, 2009	Sheet 19 of 19

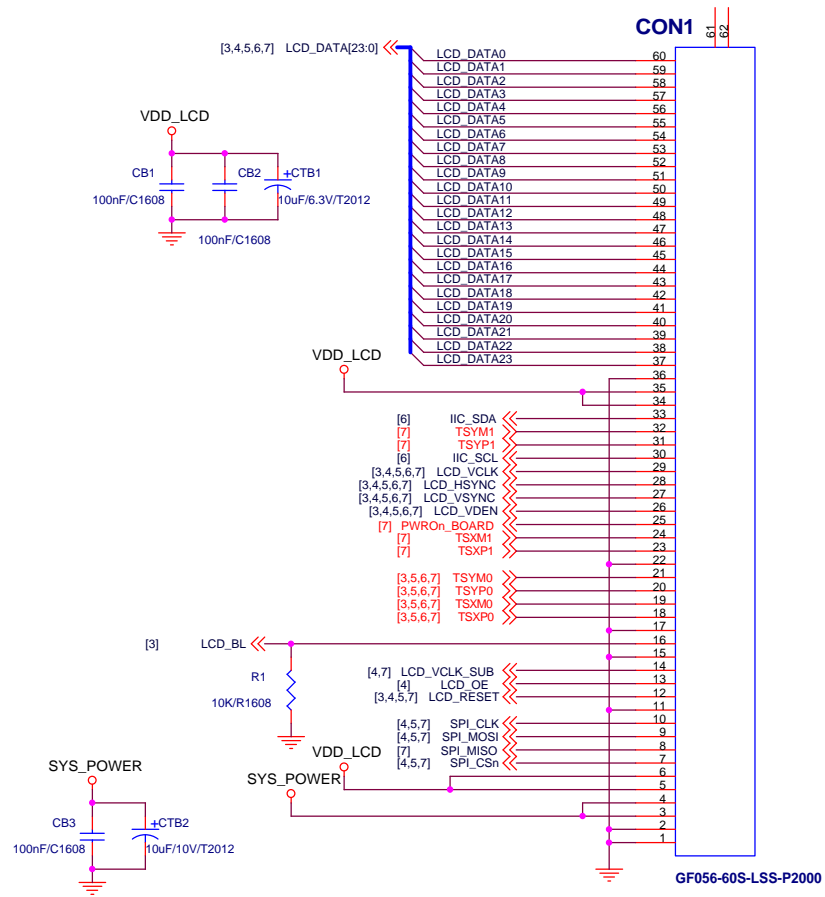
SMDK_S5PC110_LCD B'd (S5PC110 Evaluation Board) Schematics

Revision	Date	Description
Rev 0.0	2009.05.12	Preliminary Version
Rev 0.1		
Rev 0.2		

Table of Contents		Part Reference
Page	Function	<Component><Number>
01	Revision History	U : Component or Regurator IC
02	Connector To SMDK	C : Capacitor
03	4.8" WVGA(800 X 480) & BL	CB : Capacitor Bypass
04	3.1" WVGA(480 X 800)	CT : Capacitor Tantal
		CTB : Capacitor Tantal Bypass
		J : Jumper
		JB : CPU To Base connector
		JP : Jumper Power
		R : Resistor
		RA : Resistor Array
		RP : Resistor Power
		VR : Variable Resistor
		L : Inductor
		FB : Ferrite Bead
		OSC : Oscillator
		X : X-tal (Crystal)
		Q : Transistor or FET
		D : Diode
		ZD : Zener Diode
		LED : LED Diode
		SW : SWitch Tact/Push
		CON : CONnector
		CFG : ConFIGure switch (DIP/Slide)
		TP : Test Point (SMD)
		TPH : Test Point Hole (Through Hole)
		MTH: Mount Through Hole
		M (MOD) : MODule Interface connector

Title		
SMDK_S5PC110 LCD Board (S5PC110 Evaluation Board)		
Size	Document Number	Rev
A3	Revision History	0.1
Date: Thursday, October 01, 2009		Sheet 1 of 4

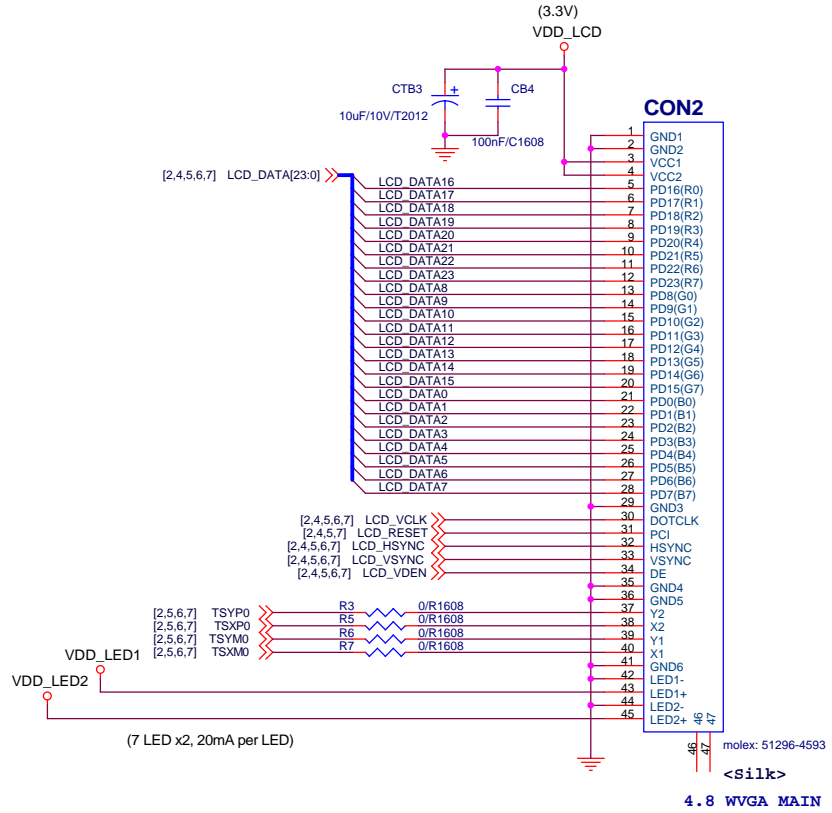
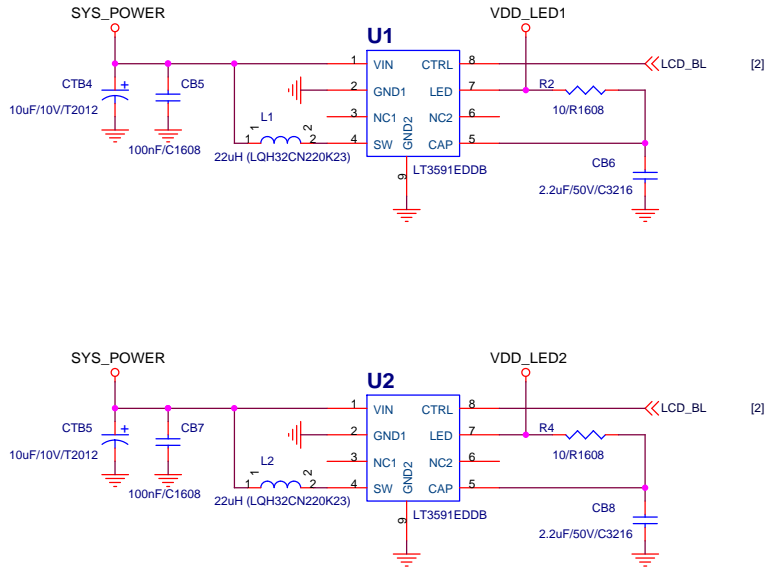
TFT LCD FPC Cable Interface From SMDK



SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110 LCD Board (S5PC110 Evaluation Board)		
Size A3	Document Number Connector to SMDK	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 2 of 4	

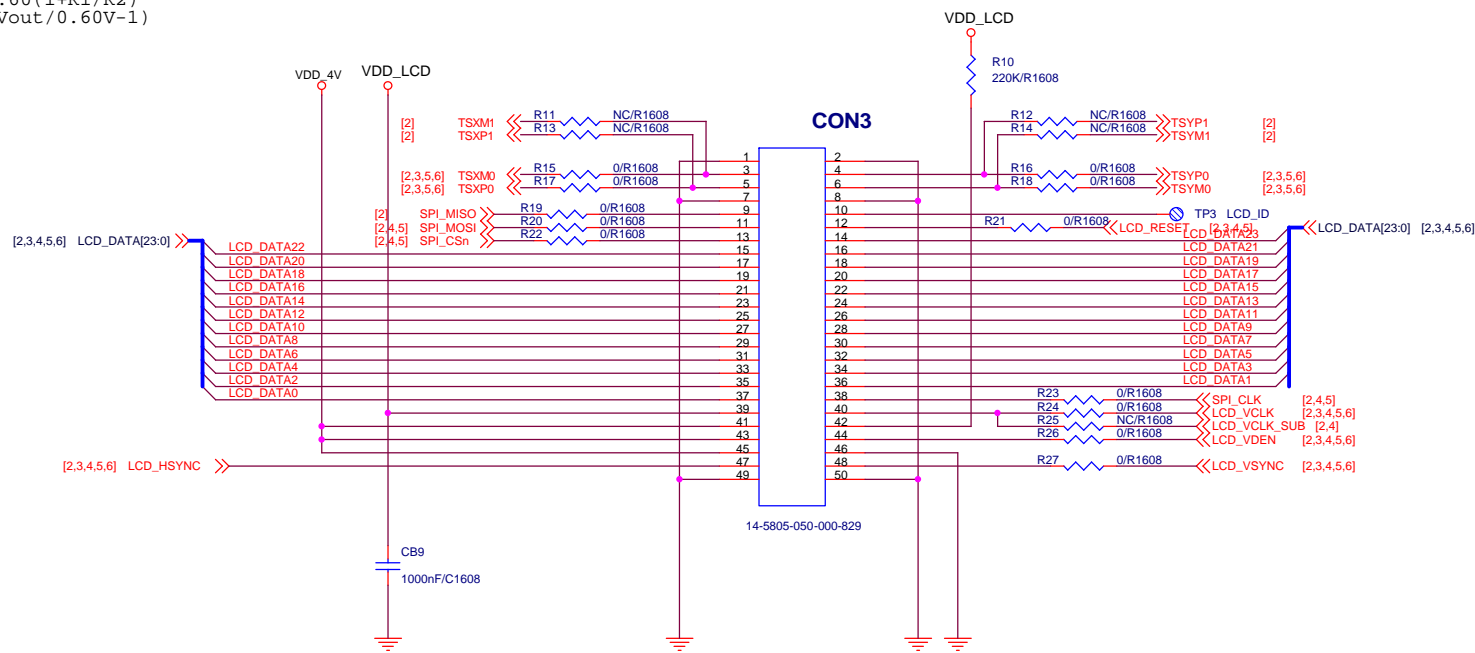
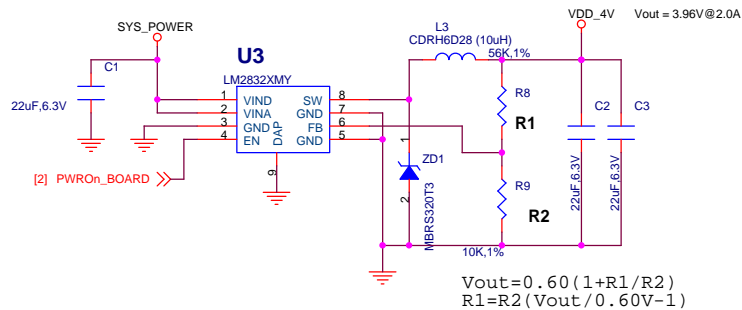
RGB(24Bit) Parallel Interface

LED drivers (Common)



**4.8inch WVGA(800x480)
LMS480KF02**

SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110 LCD Board (S5PC110 Evaluation Board)		
Size A3	Document Number 4.8inch WVGA(800x480)	Rev 0.1
Date: Thursday, October 01, 2009	Sheet 3 of 4	

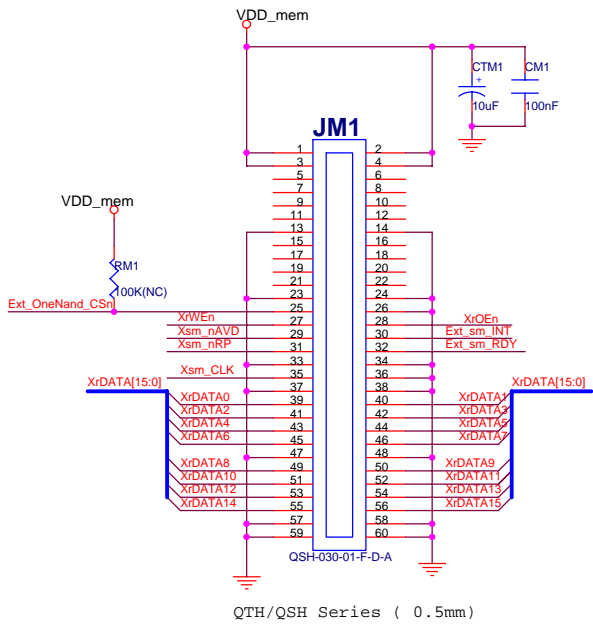


- [2,3,4,5,6] LCD_VCLK >> TP1 TP
- [2,4] LCD_VCLK_SUB >> TP2 TP
- [2,3,4,5,6] LCD_HSYNC >> TP4 TP
- [2,3,4,5,6] LCD_VSYNC >> TP5 TP
- [2,3,4,5,6] LCD_VDEN >> TP6 TP
- [2,3,4,5] LCD_RESET >> TP7 TP
- [2,3,4,5] LCD_OE >> TP8 TP

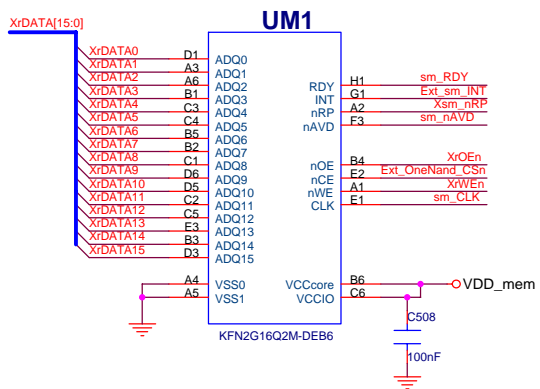
- [2,4,5] SPI_CSn >> TP9 TP
- [2,4,5] SPI_CLK >> TP10 TP
- [2,4,5] SPI_MOSI >> TP11 TP
- [2] SPI_MISO >> TP12 TP

- [2,3,4,5,6] LCD_DATA[23:0] >> LCD_DATA7 >> TP13 TP
- [2,3,4,5,6] LCD_DATA[23:0] >> LCD_DATA15 >> TP14 TP
- [2,3,4,5,6] LCD_DATA[23:0] >> LCD_DATA23 >> TP15 TP

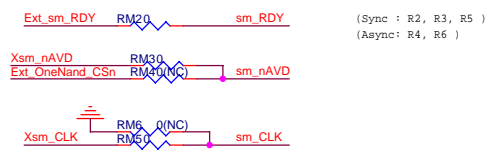
SAMSUNG ELECTRONICS CO.,LTD			
Title SMDK_S5PC110 LCD Board (S5PC110 Evaluation Board)			
Size A3	Document Number Portrait WVGA(800x480)	Rev 0.1	
Date: Thursday, October 01, 2009	Sheet 4	of 4	



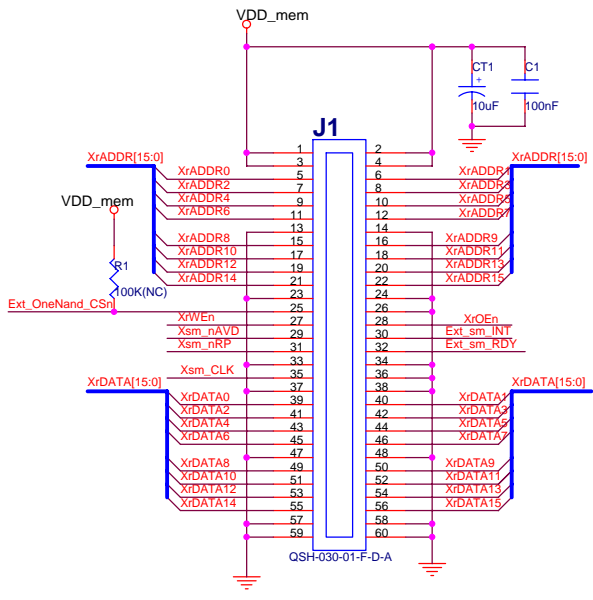
QTH/QSH Series (0.5mm)



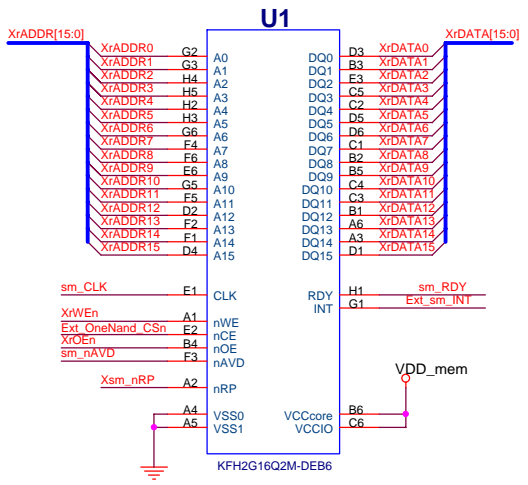
<Silk>
Mux OneNAND



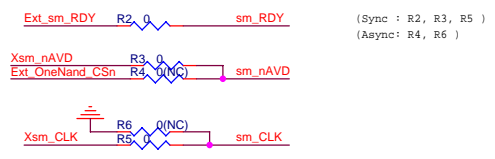
(Sync : R2, R3, R5)
(Async : R4, R6)

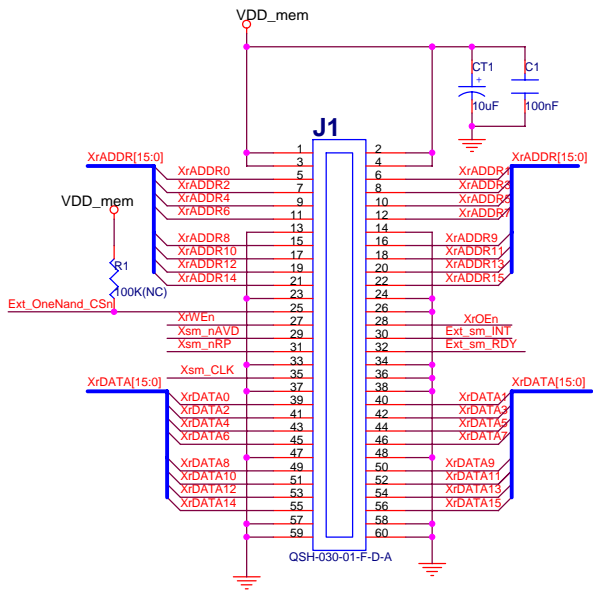


QTH/QSH Series (0.5mm)

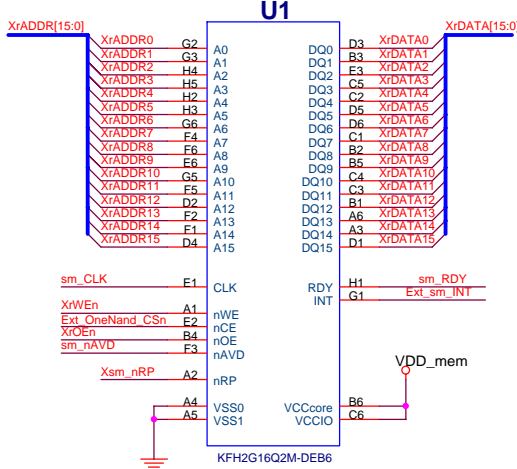


<silkscreen>
DeMux OneNAND

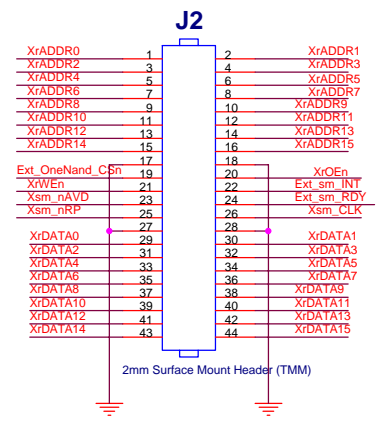




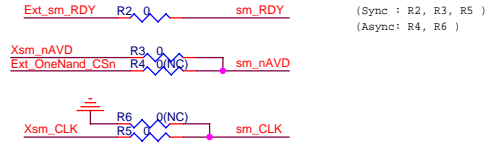
QTH/QSH Series (0.5mm)

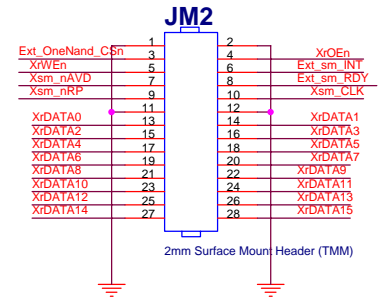
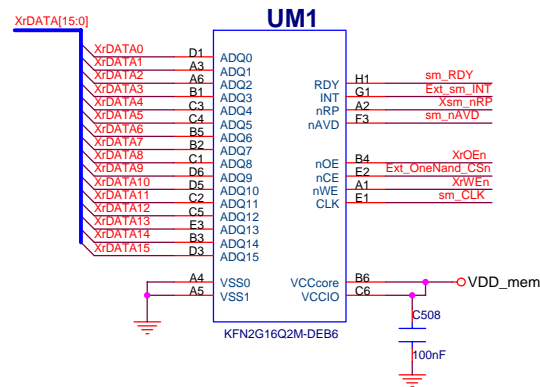
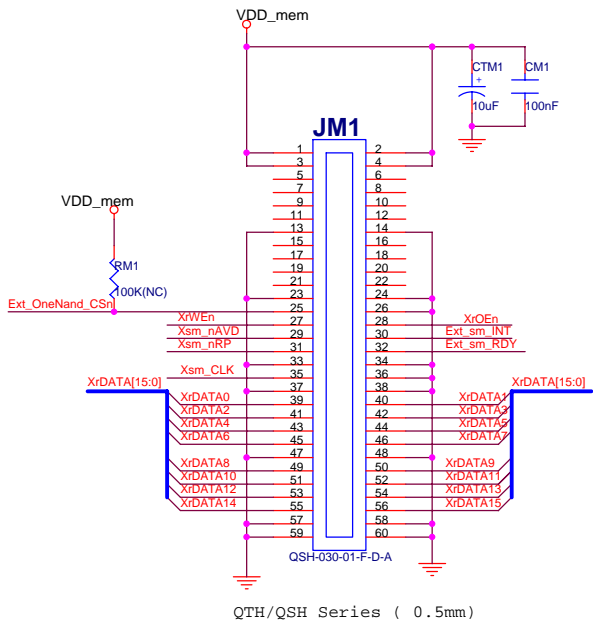


<silks>
DeMux OneNAND

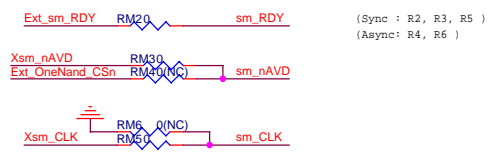


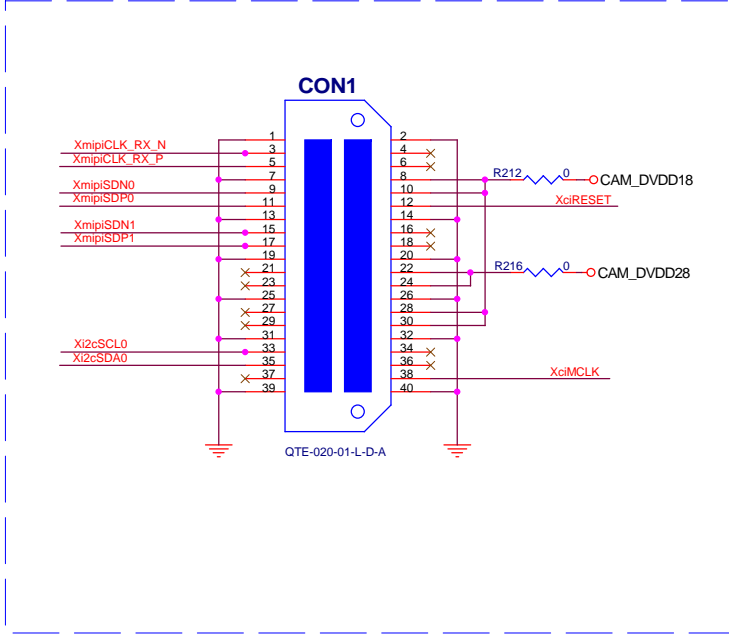
2mm Surface Mount Header (TMM)



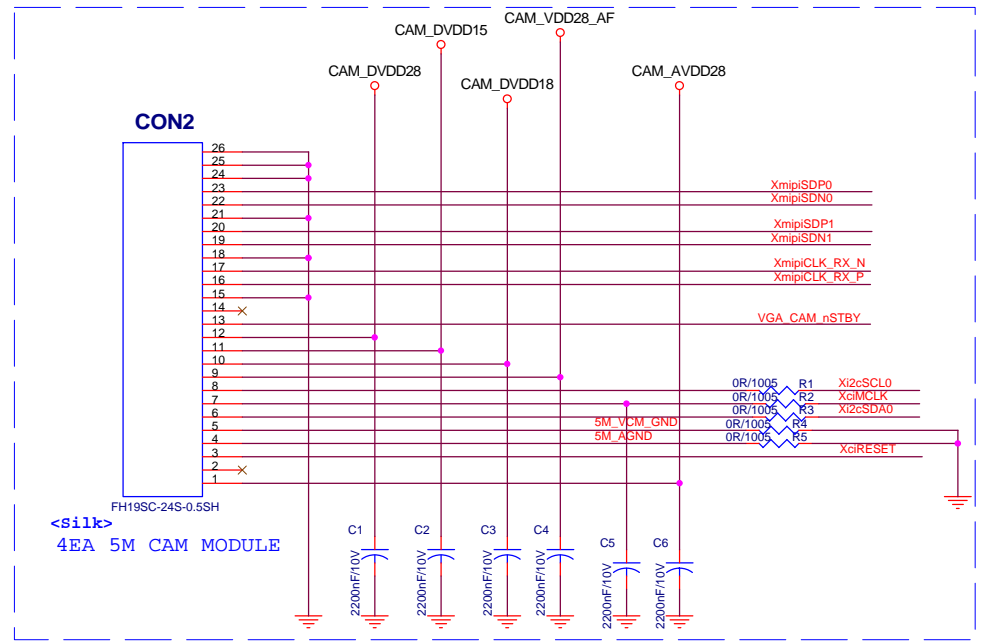


<Silk>
Mux OneNAND



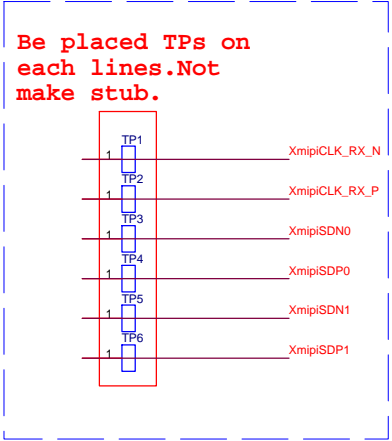


XmipiCLK_RX_N,
XmipiCLK_RX_P,
XmipiSDN0,
XmipiSDP0,
XmipiSDP1,
XmipiSDN1
위 signal은 직선으로 연결
(500Mhz differential
signal)

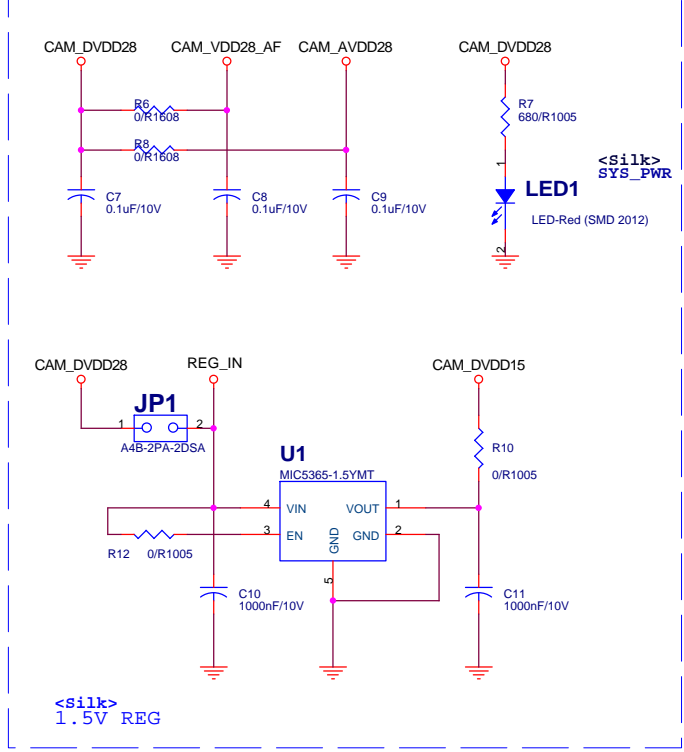


CON1

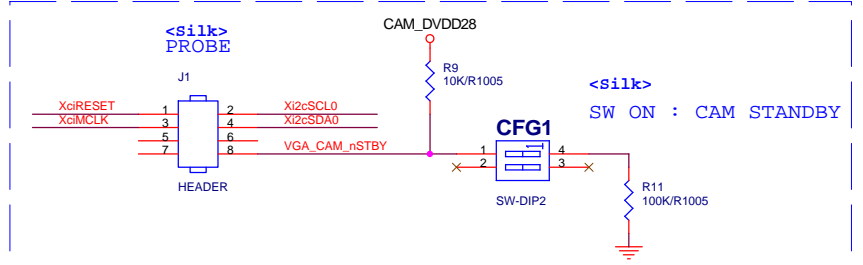
CON2



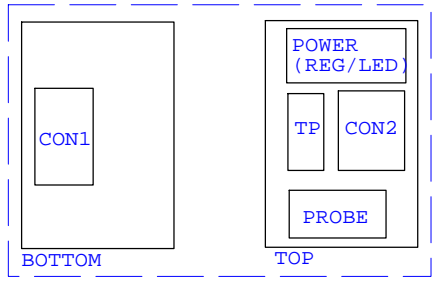
TP



POWER



PROBE



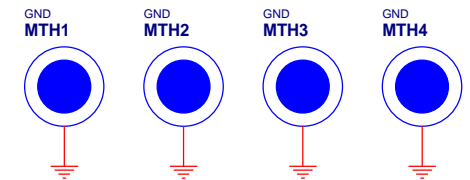
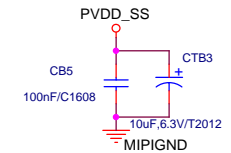
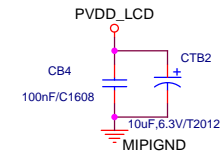
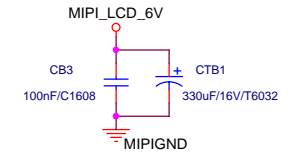
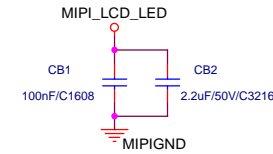
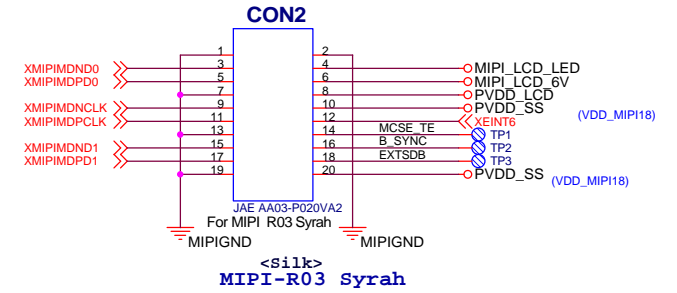
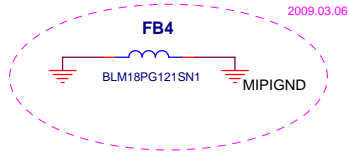
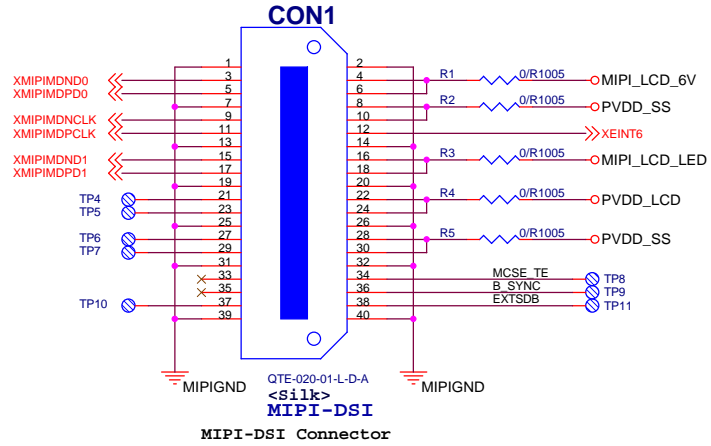
Replacement Diagram

SAMSUNG ELECTRONICS CO.,LTD		
Title SMDK_S5PC110_4EA Board (Daughter Board)		
Size A3	Document Number	Rev 0.0
Date: Thursday, May 21, 2009	Sheet 1	of 1

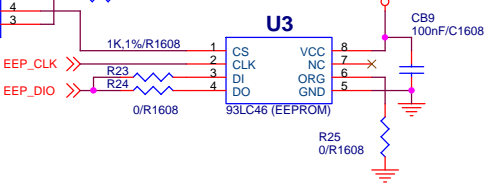
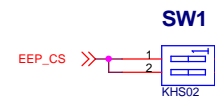
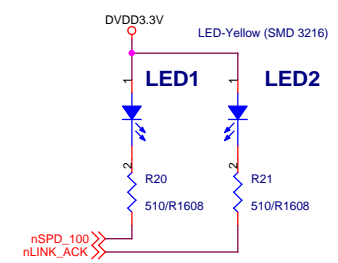
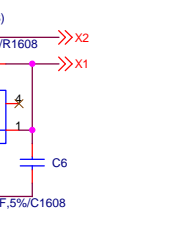
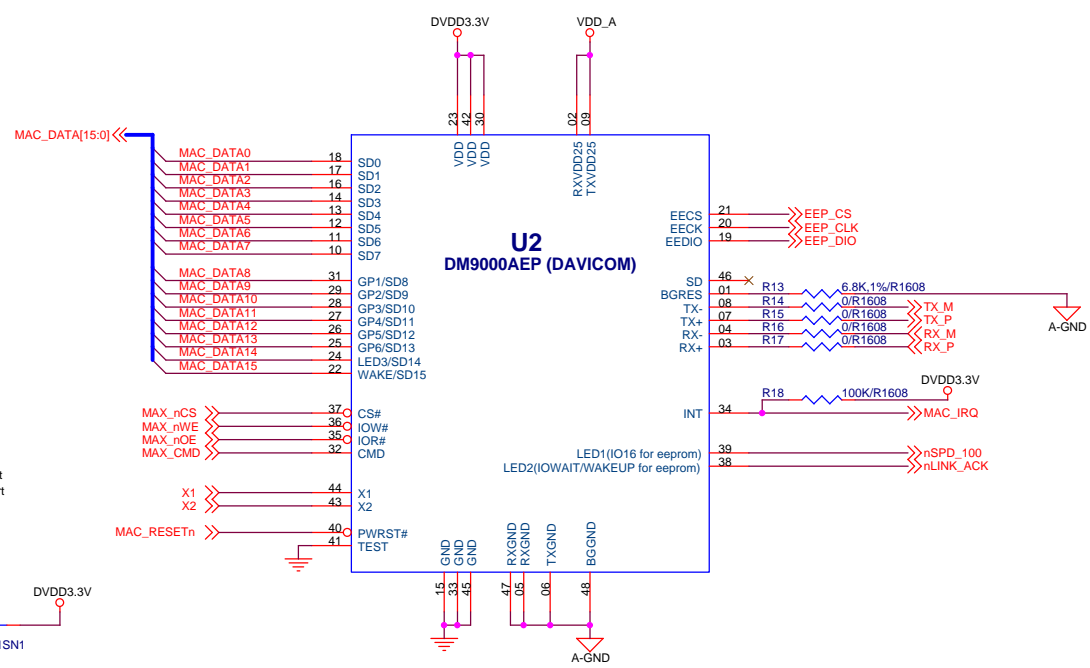
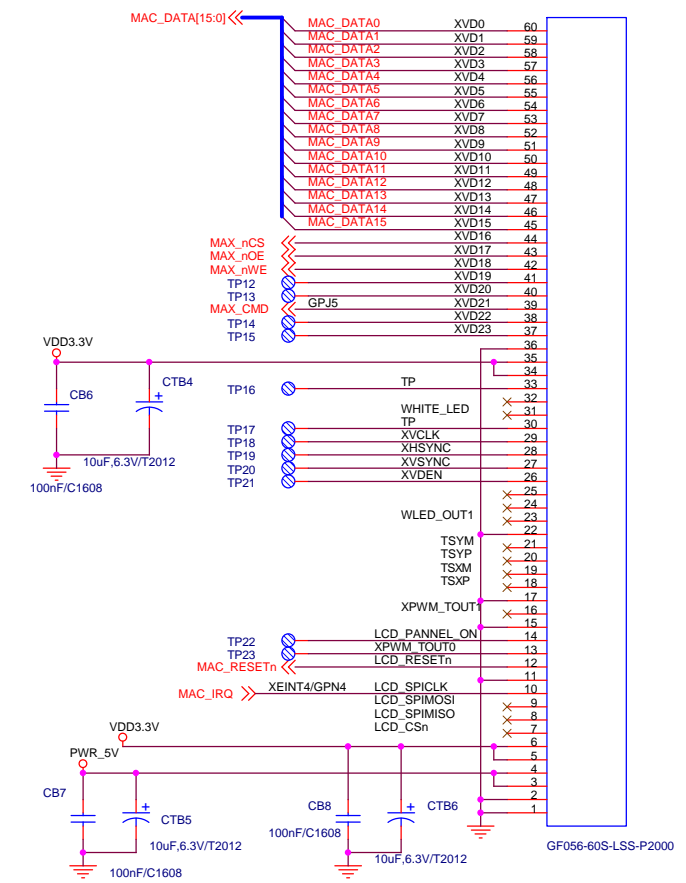
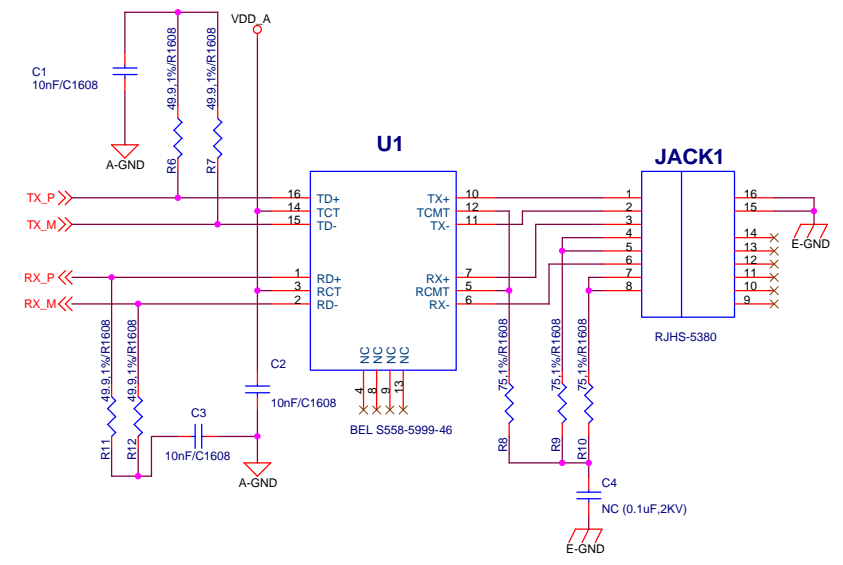
MIPI-LCM&LAN Module B'd Schematics (for SMDK6440)

Revision	Date	Description
Rev 0.0	2009.03.06 (2009.02.17)	First Version

Table of Contents		Part Reference	
Page	Function	<Component><Number>	<Component><Number>
01	Revision History	U : Component or Regurator IC	TP : Test Point (SMD)
02	MIPI-LCM	C : Capacitor	TPH : Test Point Hole (Through Hole)
03	LAN DM9000	CB : Capacitor Bypass	MTH: Mount Through Hole
		CT : Capacitor Tantal	MOD : MODule Interface connector
		CTB : Capacitor Tantal Bypass	
		CP : Capacitor return Path on power plane	
		J : Jumper	
		JB : CPU or Base connector	
		JP : Jumper Power	
		R : Resistor	
		RA : Resistor Array	
		RP : Resistor Power	
		VR : Variable Resistor	
		L : Inductor	
		FB : Ferrite Bead	
		OSC : Oscillator	
		X : X-tal (Crystal)	
		Q : Transistor or FET	
		D : Diode	
		ZD : Zener Diode	
		LED : LED Diode	
		SW : SWitch Tact/Push	
		CON : CONnector	
		CFG : ConFiGure switch (DIP/Slide)	



SAMSUNG ELECTRONICS CO.,LTD			
Title MIPI-LCM&LAN Module B'd (for SMDK6440)			
Size A3	Document Number MIPI-LCM	Rev 0.0	
Date: Friday, March 06, 2009	Sheet 1	of 2	3



SW?	ON	OFF
1	Use EEPROM	Not Use EEPROM
2	8-bit Mode	16-bit Mode

* Note :
 1. Use decal on SMDK6410 Base board.
 2. Placement on Bottom Side.

SAMSUNG ELECTRONICS CO.,LTD

Title: MIPI-LCM&LAN Module B'd (for SMDK6440)

Size: A3 | Document Number: LAN DM9000 | Rev: 0.0

Date: Tuesday, February 17, 2009 | Sheet: 3 of 3