Elektronische Bauelemente

SMG2325

0.45A , 250V , $R_{DS(ON)}$ 1.7Ω
N-Channel Enhancement Mode MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

The SMG2325 is the N-Channel logic enhancement mode power filed effect transistors are produced using high Cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state Resistance

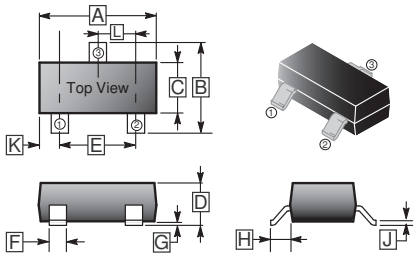
FEATURES

- Simple Drive Requirement
- Small Package Outline

MARKING

2325

SC-59

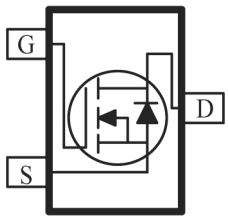


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0.10 REF.	
B	2.25	3.00	H	0.40 REF.	
C	1.30	1.70	J	0.10	0.20
D	1.00	1.40	K	0.45	0.55
E	1.70	2.30	L	0.85	1.15
F	0.35	0.50			

PACKAGE INFORMATION

Package	MPQ	Leader Size
SC-59	3K	7 inch

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

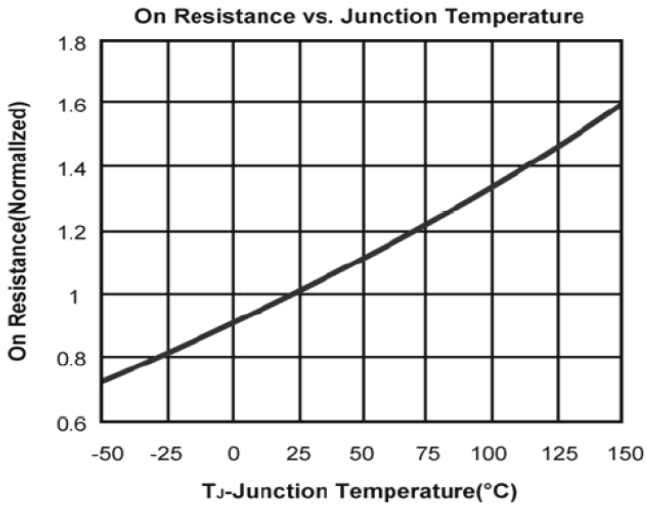
Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	250	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1], V_{GS}@10V	T_A=25℃	I_D	0.45	A
	T_A=70℃		0.35	
Pulsed Drain Current [2]		I_{DM}	1.4	A
Power Dissipation [3]	T_A=25℃	P_D	0.8	W
Operating Junction and Storage Temperature Range		T_j, T_{stg}	-55~150	℃
Thermal Resistance Rating				
Maximum Junction to Ambient [1]		$R_{\theta JA}$	156	℃ / W

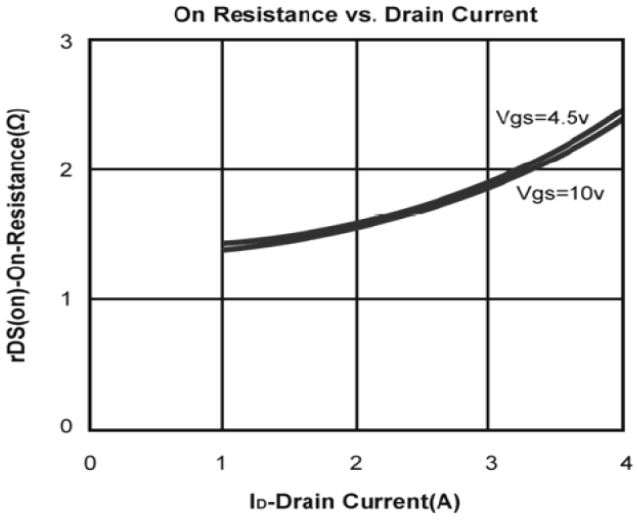
ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

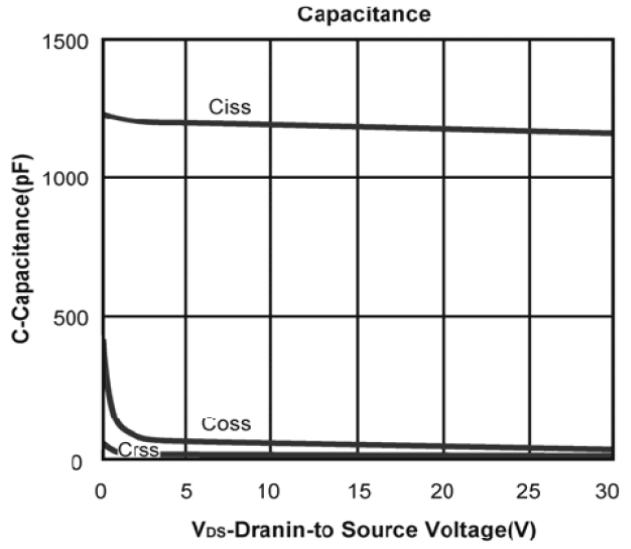
Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	250	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage	$V_{GS(th)}$	1.5	-	3.5	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Body Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	V_{DS}=250V, V_{GS}=0
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	1.7	Ω	V_{GS}=10V, I_D=0.45A
		-	-	1.9		V_{GS}=4.5V, I_D=0.35A
Diode Forward Voltage[1]	V_{SD}	-	-	1.2	V	I_S=0.45A, V_{GS}=0
Dynamic						
Total Gate Charge	Q_g	-	30	-	nC	V_{DS}=200V,V_{GS}=10V, I_D=0.45A
Total Gate Charge	Q_g	-	17	-		V_{DS}=200V, V_{GS}=4.5V, I_D=0.45A
Gate-Source Charge	Q_{gs}	-	3	-		
Gate-Drain (“Miller”) Charge	Q_{gd}	-	12	-		
Turn-on Delay Time[1]	$T_{d(on)}$	-	19	-	nS	V_{DD}=125V, V_{GS}=10V, R_G=6Ω, R_L=125Ω, I_D=0.45A
Rise Time	T_r	-	4	-		
Turn-off Delay Time	$T_{d(off)}$	-	48	-		
Fall Time	T_f	-	13	-		
Input Capacitance	C_{iss}	-	1170	-	pF	V_{GS}=0, V_{DS}=15V, f=1.0MHz
Output Capacitance	C_{oss}	-	36	-		
Reverse Transfer Capacitance	C_{rss}	-	10	-		

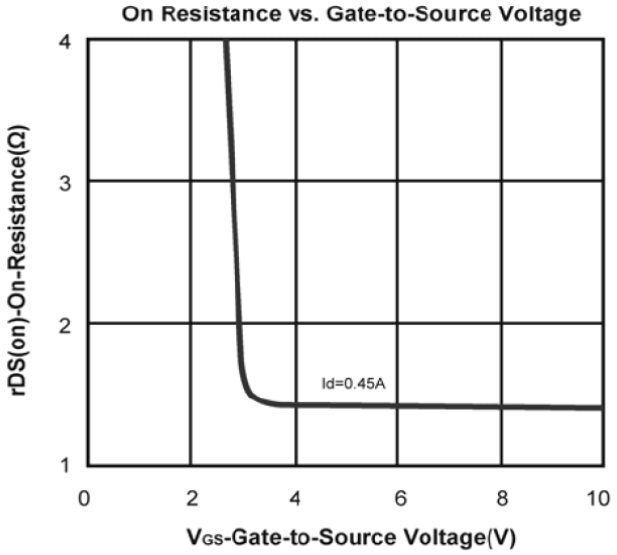
Notes:
1. Surface mounted on a 1 inch2 FR-4 board with 2OZ copper. ;270℃ /W when mounted on min. copper pad.
2. The data tested by pulsed , pulse width ≦300us , duty cycle ≦2%
3. The power dissipation is limited by 150℃ juncti on temperature
4. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

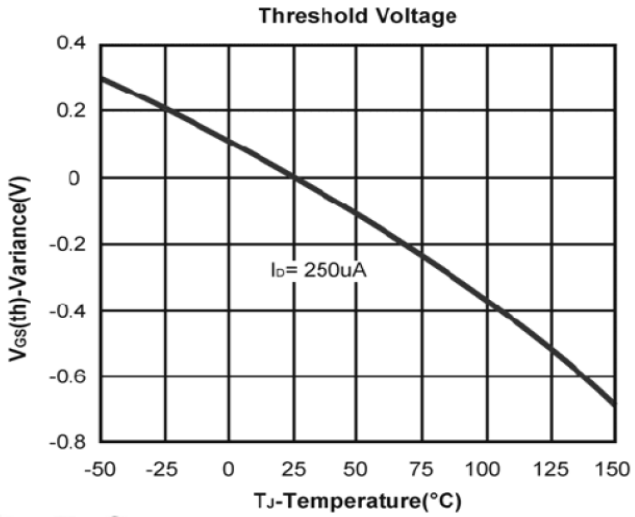
CHARACTERISTIC CURVES

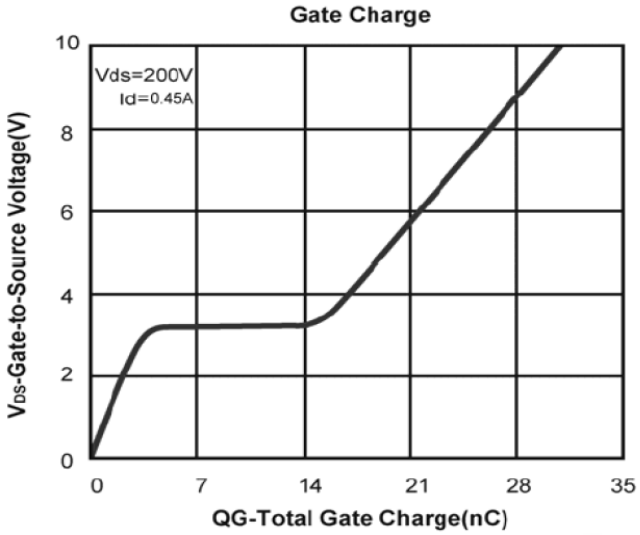












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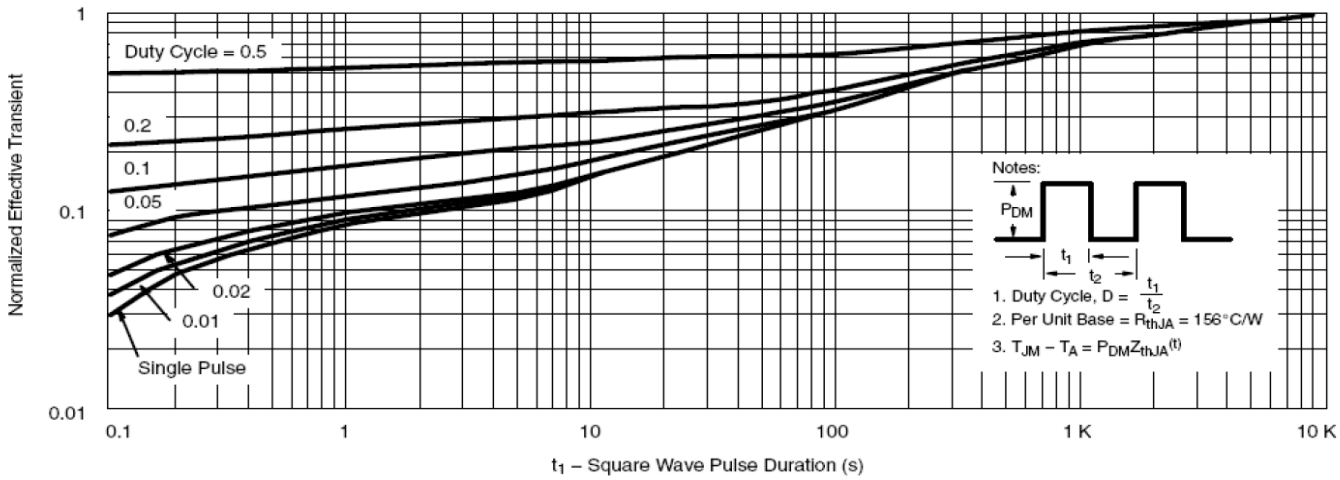

Normalized Thermal Transient Impedance, Junction-to-Ambient