

RoHS Compliant Product
 A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

The SMG2329S provide the designer with best combination of fast switching, low on-resistance and cost-effectiveness. The SMG5409 is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

FEATURES

- Simple Drive Requirement
- Small Package Outline

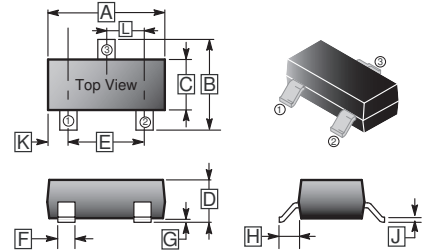
MARKING

2329S

PACKAGE INFORMATION

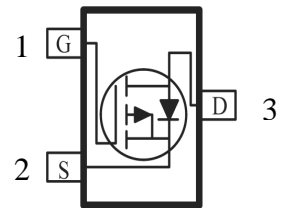
Package	MPQ	Leader Size
SC-59	3K	7 inch

SC-59



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0.10	REF.
B	2.25	3.00	H	0.40	REF.
C	1.30	1.70	J	0.10	0.20
D	1.00	1.40	K	0.45	0.55
E	1.70	2.30	L	0.85	1.15
F	0.35	0.50			

TOP VIEW



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}=10\text{V}$ ¹	I_D	$T_A=25^\circ\text{C}$	-1.2
		$T_A=70^\circ\text{C}$	-1
Pulsed Drain Current ²	I_{DM}	-5	A
Power Dissipation ³	P_D	1	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating			
Maximum Junction to Ambient ³	$R_{\theta JA}$	125	$^\circ\text{C} / \text{W}$
Maximum Junction to Case ¹	$R_{\theta JC}$	80	$^\circ\text{C} / \text{W}$

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	-100	-	-	V	$V_{GS}=0, I_D = -250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-2.5	V	$V_{DS}=V_{GS}, I_D = -250\mu\text{A}$
Gate-Body Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$
Drain-Source Leakage Current	I_{DSS}	-	-	-10	μA	$V_{DS} = -80\text{V}, V_{GS}=0, T_J=25^\circ\text{C}$
		-	-	-100		$V_{DS} = -80\text{V}, V_{GS}=0, T_J=55^\circ\text{C}$
Drain-Source On-Resistance ²	$R_{DS(ON)}$	-	-	650	m Ω	$V_{GS} = -10\text{V}, I_D = -1\text{A}$
		-	-	700		$V_{GS} = -4.5\text{V}, I_D = -0.5\text{A}$
Forward Transconductance	g_{fs}	-	3	-	S	$V_{DS} = -5\text{V}, I_D = -1\text{A}$
Dynamic						
Total Gate Charge	Q_g	-	9.3	-	nC	$V_{DS} = -50\text{V},$ $V_{GS} = -10\text{V},$ $I_D = -1\text{A}$
Gate-Source Charge	Q_{gs}	-	1.75	-		
Gate-Drain ("Miller") Change	Q_{gd}	-	1.25	-		
Turn-on Delay Time	$T_{d(on)}$	-	2	-	nS	$V_{DS} = -50\text{V},$ $V_{GS} = -10\text{V},$ $R_G=3.3\Omega,$ $I_D = -0.5\text{A}$
Rise Time	T_r	-	18.4	-		
Turn-off Delay Time	$T_{d(off)}$	-	19.6	-		
Fall Time	T_f	-	19.6	-		
Input Capacitance	C_{iss}	-	513	-	pF	$V_{GS}=0,$ $V_{DS} = -15\text{V},$ $f=1.0\text{MHz}$
Output Capacitance	C_{oss}	-	29	-		
Reverse Transfer Capacitance	C_{rss}	-	17	-		
Source-Drain Diode						
Diode Forward Voltage ²	V_{SD}	-	-	-1.2	V	$I_S = -1\text{A}, V_{GS}=0$
Continuous Source Current ^{1,4}	I_S	-	-	-1.2	A	$V_G=V_D=0\text{V}$, Force Current
Pulsed Source Current ^{2,4}	I_{SM}	-	-	-5	A	
Reverse Recovery Time	T_{RR}	-	27	-	ns	$I_S = -1\text{A}, dI/dt=100\text{A}/\mu\text{s}, T_J=25^\circ\text{C}$
Reverse Recovery Charge	Q_{RR}	-	36	-	nC	

Notes:

1. surface mounted on a 1 inch² FR-4 board with 2OZ copper. , 270 $^\circ\text{C}/\text{W}$ when mounted on Min. copper pad.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
4. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

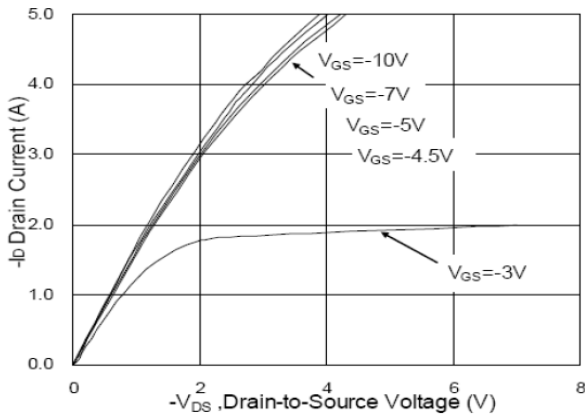


Fig 1. Typical Output Characteristics

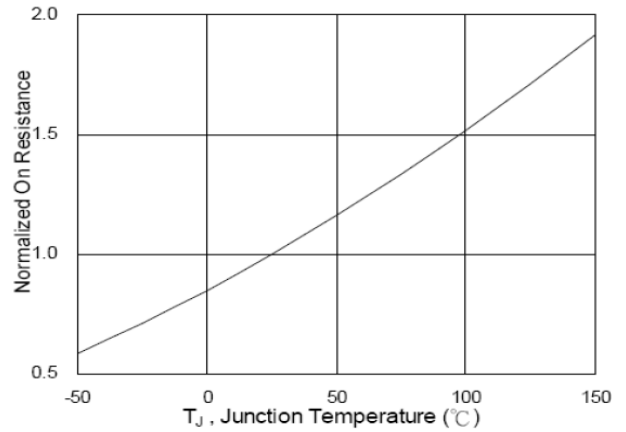


Fig 2. On-Resistance vs. Junction Temperature

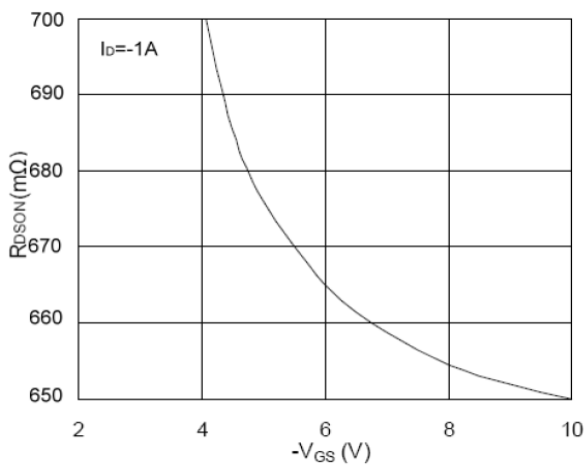


Fig 3. On-Resistance vs. Gate-Source Voltage

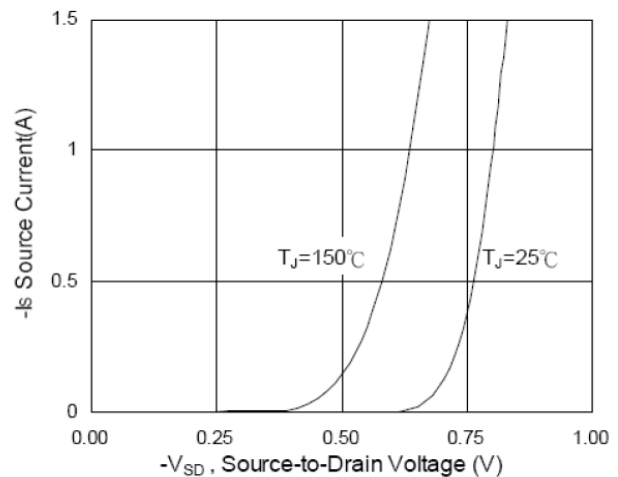


Fig 4. Body Diode Characteristics

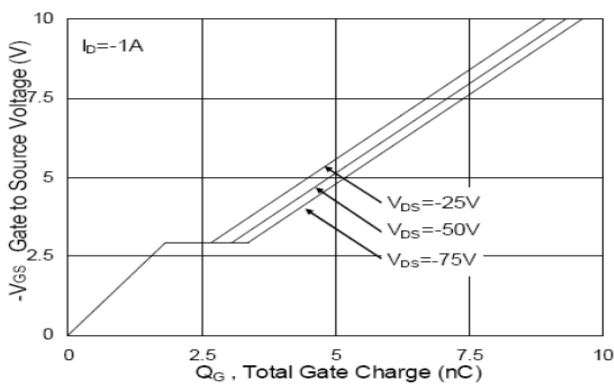


Fig 5. Gate Charge Characteristics

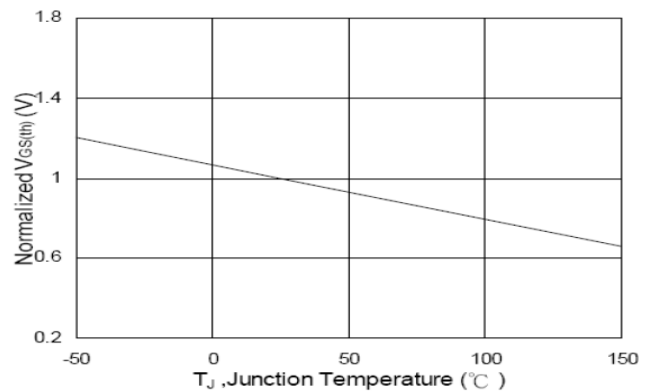


Fig 6. Threshold Voltage vs. Junction Temperature

CHARACTERISTIC CURVES

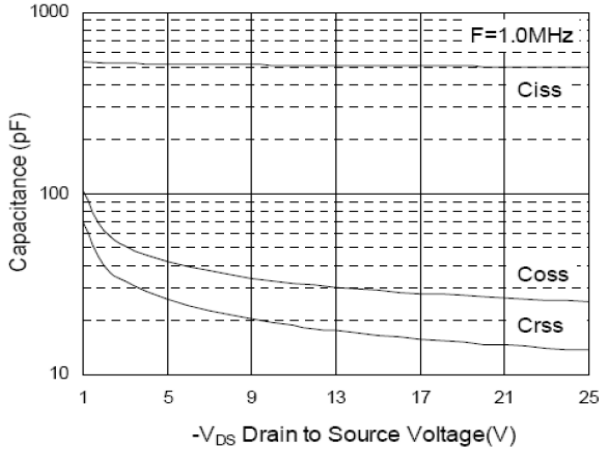


Fig 7. Typical Capacitance Characteristics

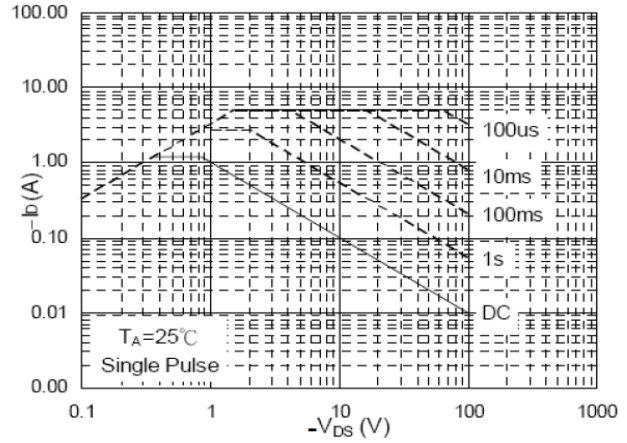


Fig 8. Safe Operating Area

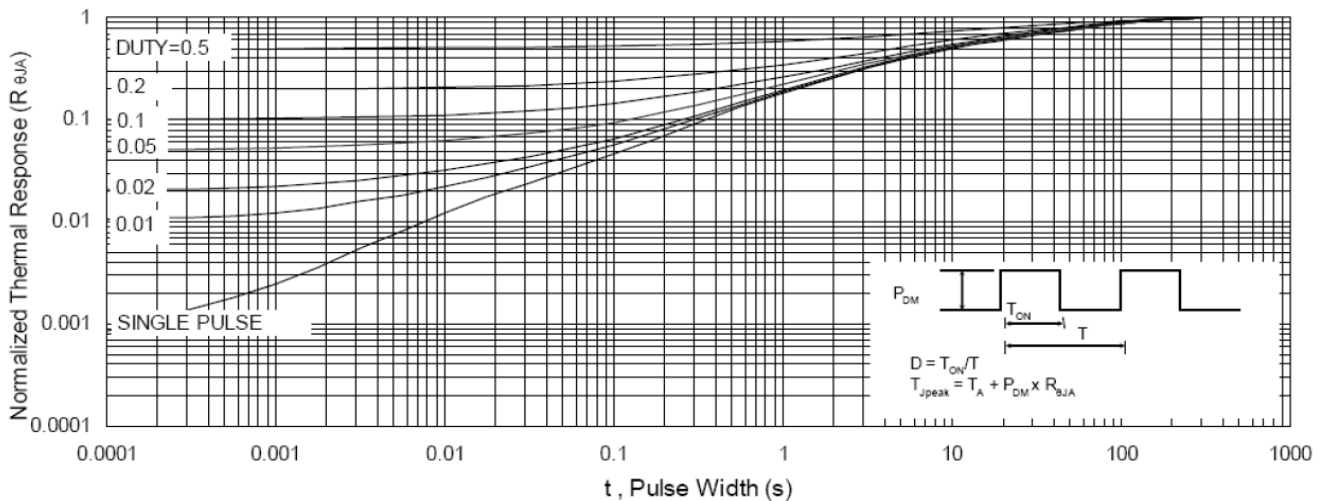


Fig 9. Normalized Maximum Transient Thermal Impedance

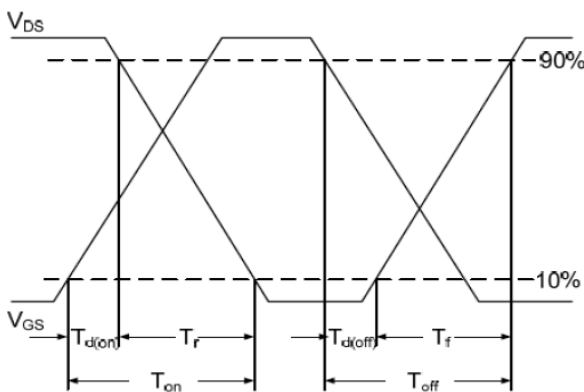


Fig 10. Switching Time Waveform

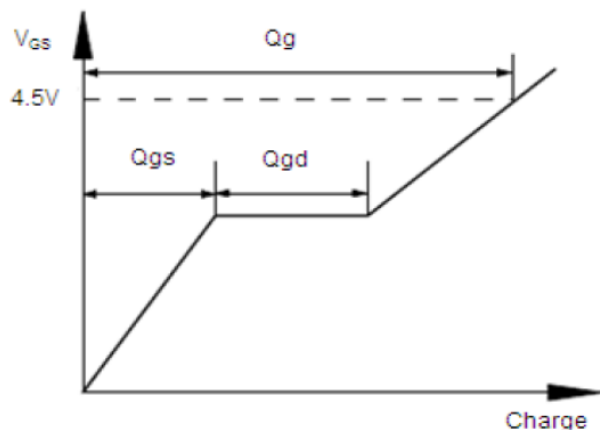


Fig 11. Gate Charge Waveform