

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

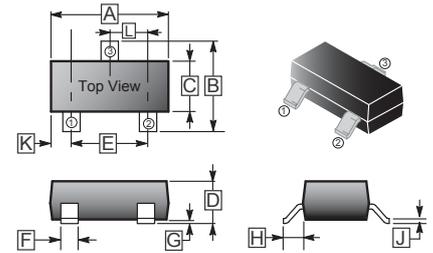
SC-59

DESCRIPTION

The miniature surface mount MOSFETs utilize a high cell density process. Low $R_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are lower voltage application, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

FEATURES

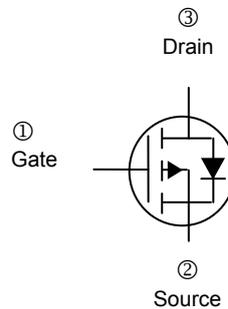
- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Fast Switch.
- Low Gate Charge.
- Miniature SC-59 surface mount package saves board space.



PRODUCT SUMMARY

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$V_{DS}(V)$	$R_{DS(on)} (\Omega)$	$I_D(A)$
-30	$0.057@V_{GS} = -4.5V$	-3.6
	$0.089@V_{GS} = -2.5V$	-2.8

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0.10	REF.
B	2.25	3.00	H	0.40	REF.
C	1.30	1.70	J	0.10	0.20
D	1.00	1.40	K	0.45	0.55
E	1.70	2.30	L	0.85	1.15
F	0.35	0.50			



ABSOLUTE MAXIMUM RATINGS AND THERMAL DATA ($T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^A	I_D	$T_A = 25^\circ C$	± 3.6
		$T_A = 70^\circ C$	± 2.9
Pulsed Drain Current ^B	I_{DM}	± 10	A
Continuous Source Current (Diode Conduction) ^A	I_S	0.4	A
Power Dissipation ^A	P_D	$T_A = 25^\circ C$	1.25
		$T_A = 70^\circ C$	0.8
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	$^\circ C$
THERMAL RESISTANCE DATA			
Maximum Junction to Ambient ^A	$R_{\theta JA}$	$t \leq 5 \text{ sec}$	100
		Steady-State	150

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-0.80	-	-	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0\text{V}, V_{GS} = \pm 12\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -24\text{V}, V_{GS} = 0\text{V}$
		-	-	-10		$V_{DS} = -24\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$
On-State Drain Current ^A	$I_{D(ON)}$	-2	-	-	A	$V_{DS} = -5\text{V}, V_{GS} = -4.5\text{V}$
Drain-Source On-Resistance ^A	$R_{DS(ON)}$	-	-	57	m Ω	$V_{GS} = -4.5\text{V}, I_D = -3.6\text{A}$
		-	-	89		$V_{GS} = -2.5\text{V}, I_D = -2.8\text{A}$
Forward Transconductance ^A	g_{FS}	-	2	-	S	$V_{DS} = -5\text{V}, I_D = -3.6\text{A}$
Diode Forward Voltage	V_{SD}	-	-0.70	-	V	$I_S = -0.4\text{A}, V_{GS} = 0\text{V}$
Dynamic ^b						
Total Gate Charge	Q_g	-	25	-	nC	$I_D = -3.6\text{A}$
Gate-Source Charge	Q_{gs}	-	2.4	-		$V_{DS} = -10\text{V}$
Gate-Drain Charge	Q_{gd}	-	3.9	-		$V_{GS} = -5\text{V}$
Turn-On Delay Time	$T_{d(ON)}$	-	7.6	-	nS	$V_{DS} = -15\text{V}$
Rise Time	T_r	-	6.8	-		$I_D = -1\text{A}$
Turn-Off Delay Time	$T_{d(OFF)}$	-	33.6	-		$V_{GEN} = -10\text{V}$
Fall Time	T_f	-	23.2	-		$R_G = 50\Omega$

Notes

- a. Pulse test : $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.