

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

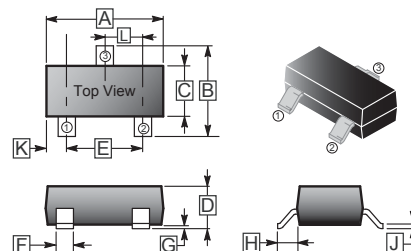
SC-59

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SC-59 saves board space.
- Fast switching speed.
- High performance trench technology.



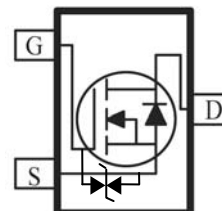
PACKAGE INFORMATION

Package	MPQ	LeaderSize
SC-59	3K	7' inch

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0.10	REF.
B	2.25	3.00	H	0.40	REF.
C	1.30	1.70	J	0.10	0.20
D	1.00	1.40	K	0.45	0.55
E	1.70	2.30	L	0.85	1.15
F	0.35	0.50			



ESD
Protection
Diode
2KV



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	I_D	$T_A=25^\circ\text{C}$	5.2
		$T_A=70^\circ\text{C}$	4.1
Pulsed Drain Current ²	I_{DM}	30	A
Continuous Source Current (Diode Conduction) ¹	I_S	1.6	A
Power Dissipation ¹	P_D	$T_A=25^\circ\text{C}$	1.3
		$T_A=70^\circ\text{C}$	0.8
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	$^\circ\text{C}$
Thermal Resistance Data			
Maximum Junction to Ambient ¹	$R_{\theta JA}$	$t \leq 5$ sec	100
		Steady-State	166

Notes

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	-	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0\text{V}, V_{GS} = 20\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}$
		-	-	25		$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}, T_J=55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(ON)}$	20	-	-	A	$V_{DS} = 5\text{V}, V_{GS} = 10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	86	m Ω	$V_{GS} = 10\text{V}, I_D = 5.2\text{A}$
		-	-	128		$V_{GS} = 4.5\text{V}, I_D = 3.7\text{A}$
Forward Transconductance ¹	g_{FS}	-	40	-	S	$V_{DS} = 15\text{V}, I_D = 5.2\text{A}$
Diode Forward Voltage	V_{SD}	-	0.7	-	V	$I_S = 2.3\text{A}, V_{GS} = 0\text{V}$
Dynamic ²						
Total Gate Charge	Q_g	-	4.0	-	nC	$I_D = 5.2\text{A}$ $V_{DS} = 15\text{V}$ $V_{GS} = 4.5\text{V}$
Gate-Source Charge	Q_{gs}	-	1.1	-		
Gate-Drain Charge	Q_{gd}	-	1.4	-		
Turn-On Delay Time	$T_{d(ON)}$	-	16	-	nS	$I_D = 1\text{A}, V_{DD} = 25\text{V}$ $V_{GEN} = 10\text{V}$ $R_L = 25\Omega$
Rise Time	T_r	-	5	-		
Turn-Off Delay Time	$T_{d(OFF)}$	-	23	-		
Fall Time	T_f	-	3	-		

Notes

1. Pulse test : $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.