

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

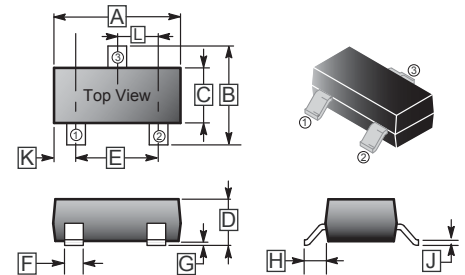
DESCRIPTION

These miniature surface mount MOSFETs utilize a High Cell Density trench process to provide Low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printer, PCMCIA cards, cellular and cordless telephones.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SC-59 saves board Space.
- Fast switching speed.
- High performance trench technology.

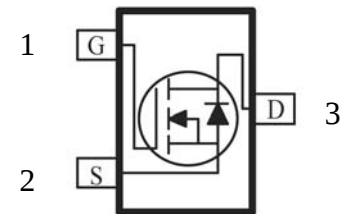
SC-59



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0.10	REF.
B	2.25	3.00	H	0.40	REF.
C	1.30	1.70	J	0.10	0.20
D	1.00	1.40	K	0.45	0.55
E	1.70	2.30	L	0.85	1.15
F	0.35	0.50			

PACKAGE INFORMATION

Package	MPQ	LeaderSize
SC-59	3K	7' inch



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	$I_D @ T_A=25^\circ\text{C}$	1.8	A
Pulsed Drain Current ²	I_{DM}	± 10	A
Continuous Source Current (Diode Conduction) ¹	I_S	1.1	A
Power Dissipation ¹	$P_D @ T_A=25^\circ\text{C}$	1.3	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 ~ 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Typ	Max	Unit
Maximum Junction to Ambient ¹	$R_{\theta JA}$	93	110	$^\circ\text{C} / \text{W}$
		130	150	

Notes

- 1 Surface Mounted on 1" x 1" FR4 Board.
- 2 Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1.0	-	-	V	$V_{DS}=V_{GS}$, $I_D = 250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0\text{V}$, $V_{GS} = \pm 8\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
		-	-	10		$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(on)}$	10	-	-	A	$V_{DS} = 5\text{V}$, $V_{GS} = 10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	280	m Ω	$V_{GS} = 10\text{V}$, $I_D = 1.8\text{A}$
		-	-	355		$V_{GS} = 5.5\text{V}$, $I_D = 1.6\text{A}$
Forward Transconductance ¹	g_{fs}	-	11.3	-	S	$V_{DS} = 10\text{V}$, $I_D = 1.8\text{A}$
Diode Forward Voltage	V_{SD}	-	0.75	-	V	$I_S = 1.6\text{A}$, $V_{GS} = 0\text{V}$
Dynamic ²						
Total Gate Charge	Q_g	-	7.0	-	nC	$V_{DS} = 10\text{V}$, $V_{GS} = 5.5\text{V}$, $I_D = 1.8\text{A}$
Gate-Source Charge	Q_{gs}	-	1.1	-		
Gate-Drain Charge	Q_{gd}	-	2.0	-		
Turn-on Delay Time	$T_{d(on)}$	-	8	-	nS	$V_{DD} = 10\text{V}$, $V_{GEN} = 4.5\text{V}$, $R_L = 15\Omega$, $I_D = 1\text{A}$
Rise Time	T_r	-	24	-		
Turn-off Delay Time	$T_{d(off)}$	-	35	-		
Fall Time	T_f	-	10	-		

Notes

- 1 Pulse test : $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- 2 Guaranteed by design, not subject to production testing.