

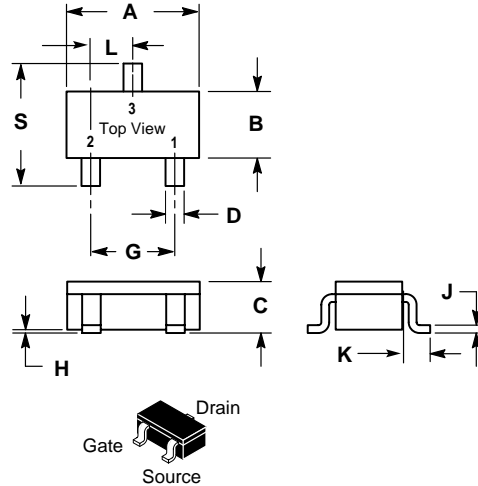
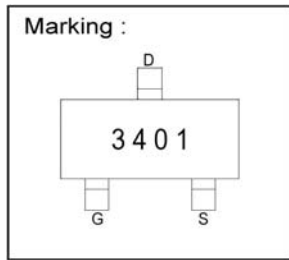
A suffix of "-C" specifies halogen & lead-free

## Description

The SMG3401 uses advanced trench technology to provide excellent on-resistance extremely efficient and cost-effectiveness device. The SMG3401 is universally used for all commercial-industrial applications.

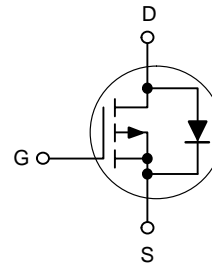
## Features

- \* Small Package Outline
- \* Lower Gate Charge
- \* RoHS Compliant



SC-59		
Dim	Min	Max
A	2.70	3.10
B	1.40	1.60
C	1.00	1.30
D	0.35	0.50
G	1.70	2.10
H	0.00	0.10
J	0.10	0.26
K	0.20	0.60
L	0.85	1.15
S	2.40	2.80

All Dimension in mm



## Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current <sup>3</sup>	$I_D @ T_A=25^\circ C$	-4.2	A
Continuous Drain Current <sup>3</sup>	$I_D @ T_A=70^\circ C$	-3.5	A
Pulsed Drain Current <sup>1,2</sup>	$I_{DM}$	30	A
Total Power Dissipation	$P_D @ T_A=25^\circ C$	1.38	W
Linear Derating Factor		0.01	W/°C
Operating Junction and Storage Temperature Range	$T_j, T_{stg}$	-55~+150	°C

## Thermal Data

Parameter	Symbol	Ratings	Unit
Thermal Resistance Junction-ambient <sup>3</sup>	Max. $R_{thj-a}$	90	°C/W

**Electrical Characteristics( T<sub>j</sub>=25 °C Unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.7	-	-1.3	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA
Gate-Source Leakage Current	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±12V
Drain-Source Leakage Current (T <sub>j</sub> =25°C)	I <sub>DSS</sub>	-	-	-1	uA	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0
Drain-Source Leakage Current (T <sub>j</sub> =55°C)		-	-	-5	uA	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	-	-	50	mΩ	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4.2A
		-	-	65		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4.0A
		-	-	120		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-1.0A
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	-	9.4	-	nC	I <sub>D</sub> =-4A V <sub>DS</sub> =-15V V <sub>GS</sub> =-4.5V
Gate-Source Charge	Q <sub>gs</sub>	-	2	-		
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>	-	3	-		
Turn-on Delay Time <sup>2</sup>	T <sub>d(ON)</sub>	-	6.3	-	nS	V <sub>DS</sub> =-15V V <sub>GS</sub> =-10V R <sub>G</sub> =6 Ω R <sub>L</sub> =3.6 Ω
Rise Time	T <sub>r</sub>	-	3.2	-		
Turn-off Delay Time	T <sub>d(OFF)</sub>	-	38.2	-		
Fall Time	T <sub>f</sub>	-	12	-		
Input Capacitance	C <sub>iss</sub>	-	954	-	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =-15V f=1.0MHz
Output Capacitance	C <sub>oss</sub>	-	115	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	77	-		
Gate Resistance	R <sub>g</sub>	-	6	-	Ω	f=1.0MHz

**Source-Drain Diode**

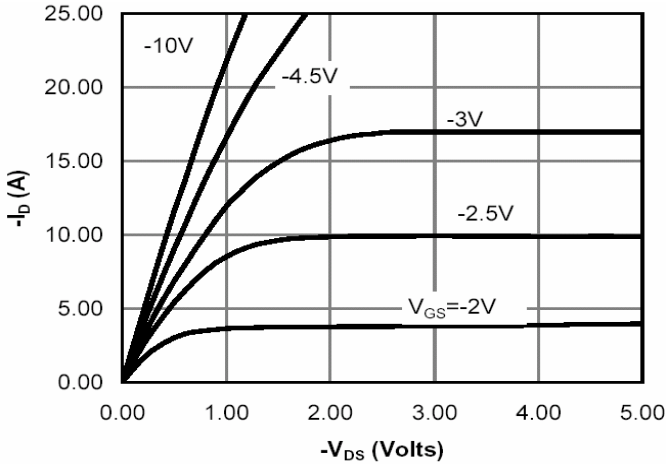
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage <sup>2</sup>	V <sub>SD</sub>	-	-	-1.0	V	I <sub>S</sub> =-1.0A, V <sub>GS</sub> =0V.
Reverse Recovery Time <sup>2</sup>	T <sub>rr</sub>	-	20.2	-	nS	I <sub>S</sub> =-4A, V <sub>GS</sub> =0 dI/dt=100A/uS
Reverse Recovery Charge	Q <sub>rr</sub>	-	11.2	-	nC	
Continuous Source Current (Body Diode)	I <sub>S</sub>	-	-	-2.2	A	V <sub>D</sub> =V <sub>G</sub> =0V, V <sub>S</sub> =-1.0V

Notes: 1.Pulse width limited by Max. junction temperature.

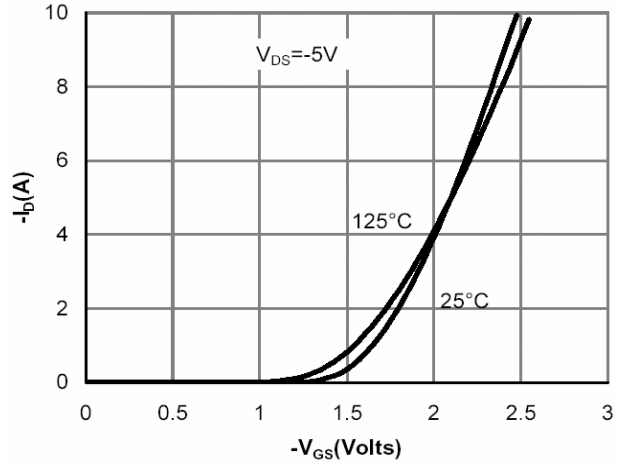
2.Pulse width ≤300us, dutycycle ≤2%.

3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board; 270°C/W when mounted on min. copper pad.

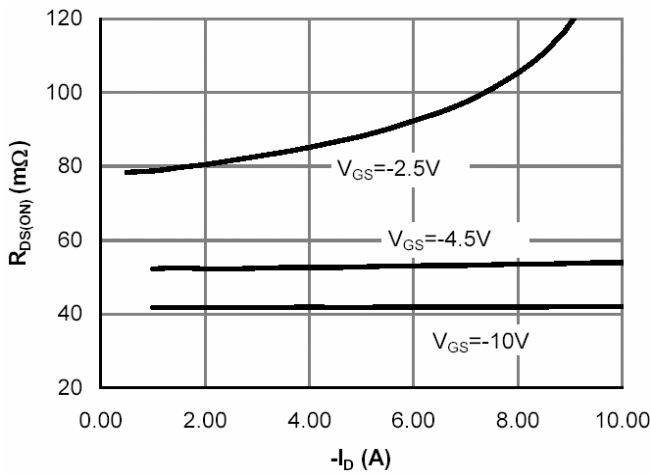
**Characteristics Curve**



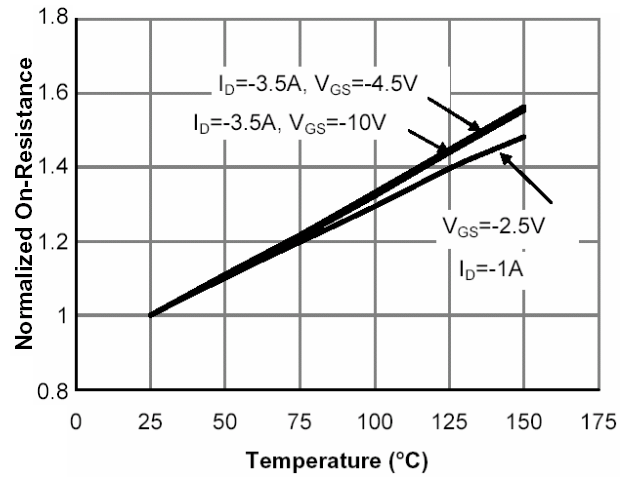
**Fig 1. Typical Output Characteristics**



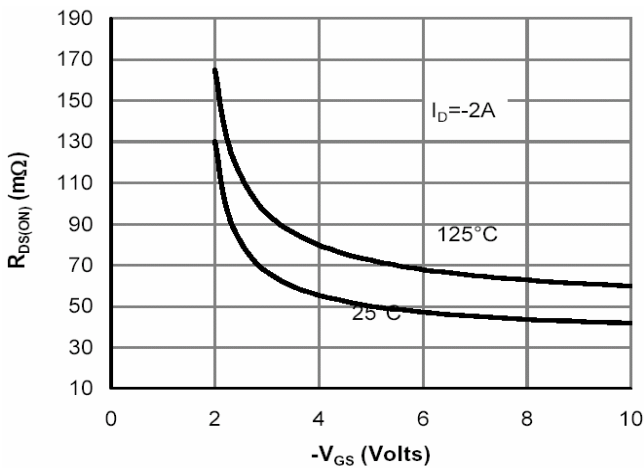
**Fig 2. Typical Output Characteristics**



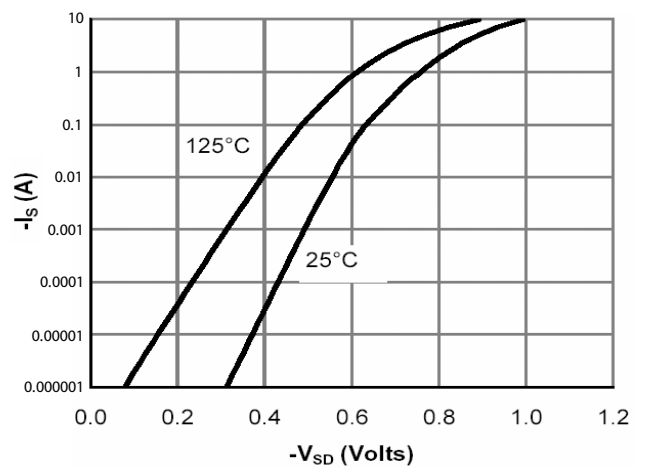
**Fig 3. On-Resistance v.s. Gate Voltage**



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



**Fig 5. Forward Characteristics of Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**

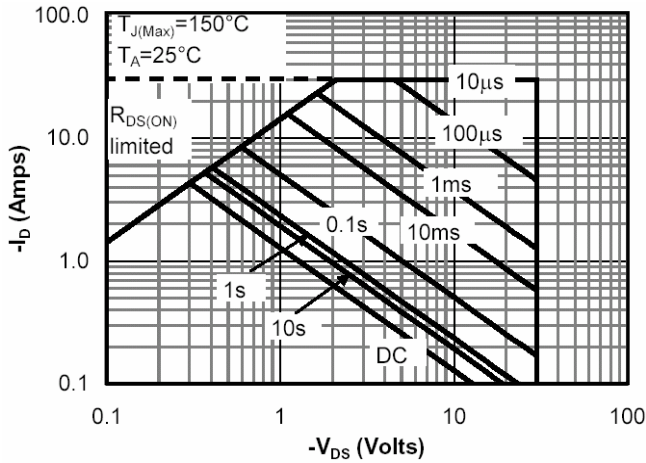


Fig 7. Gate Charge Characteristics

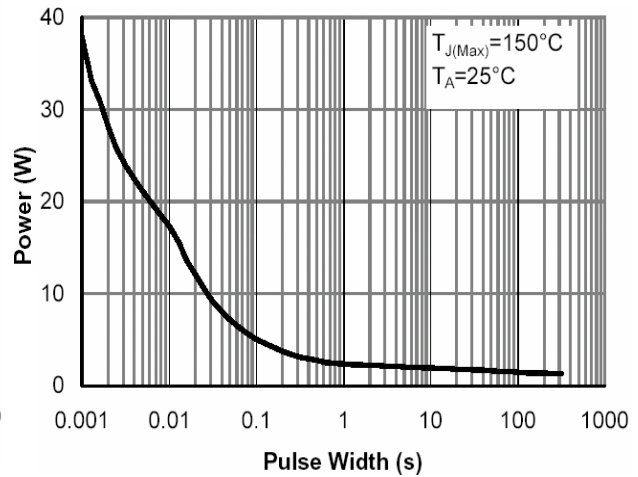


Fig 8. Typical Capacitance Characteristics

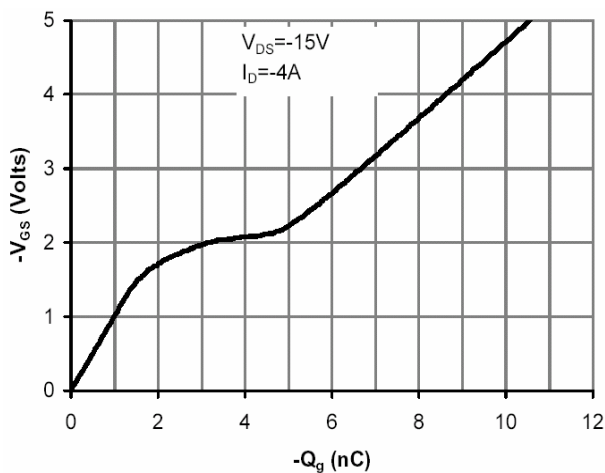


Fig 9. Maximum Safe Operating Area

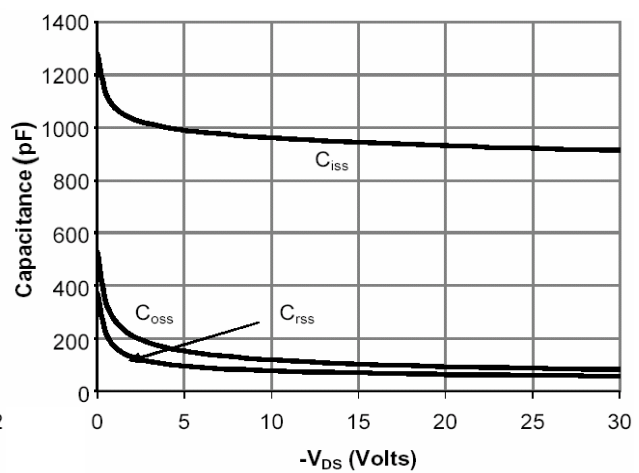


Fig 10. Effective Transient Thermal Impedance

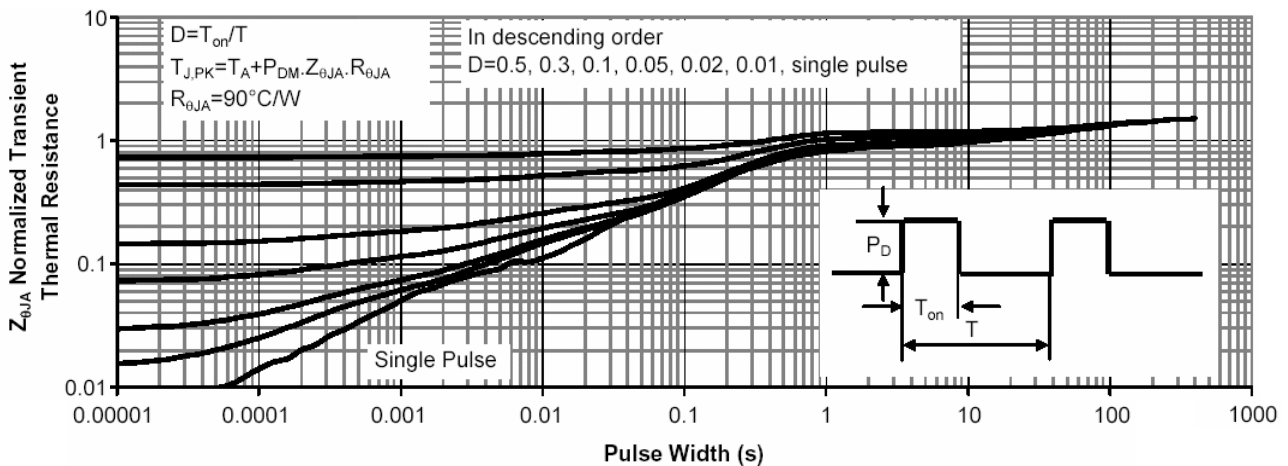


Fig 11. Normalized Maximum Transient Thermal Impedance