Preliminary Information [1] *(See Last Page)*

Hot-Swap, Active DC Output Control (ADOC™) Power Manager with I²C Interface

FEATURES & APPLICATIONS

- **Full voltage Control for hot-swap applications**
  - **Add-in Card insertion detection**
  - **Platform voltage detection**
- **Universal FPGA configuration I/O pins**
- **High Voltage and logic level enable outputs**
- **Active control (ADOC™) for three downstream DC/DC converters with ±0.5% accuracy**
- **Margining of three DC/DC converters**
- **Power-up sequencing of all supply voltages**
- **Power-down sequencing in Forward or Reverse**
- **UV and OV sensors per channel with programmable reset and interrupt**
- **Programmable glitch filter for all channels**
- **Configuration may be locked**
- **Auto monitoring of all channels and Ext Temp**
- **I²C™ serial bus interface**
- **Programmable slew rate control**
- **Integrated 2K EEPROM**

Applications

- **Monitor/Control Distributed and POL Supplies**
- **Multi-voltage Processors, DSPs, ASICs used in Telecom or server systems**

INTRODUCTION

The SMH4046 is an all-inclusive power management controller that integrates hot swap protection of three positive-voltage supplies (+12V or less). In addition to hot swapping three bus voltages, it provides sequencing and Active DC Output Control (ADOC™) of three on-card DC-DC converters as used in blade servers and Telecom systems. It can also upload configuration code from the host to on-card FPGAs.

All six channels can cascade-sequence during power-up in any order as set by either hardware or firmware; and sequence down in forward or reverse order. ADOC™ control of the three DC/DC converters maintains their accuracy to within ±0.5% of the set point using an internal voltage reference. ADOC™ is also included during "margining" to allow card-by-card performance evaluation during production with arbitrary setting within ±10% in any combination.

A full set of monitoring and control features are included, with user programmability that can be locked. The SMH4046 uses the I²C bus interface for programming and FPGA configuration.

TYPICAL APPLICATIONS DRAWING

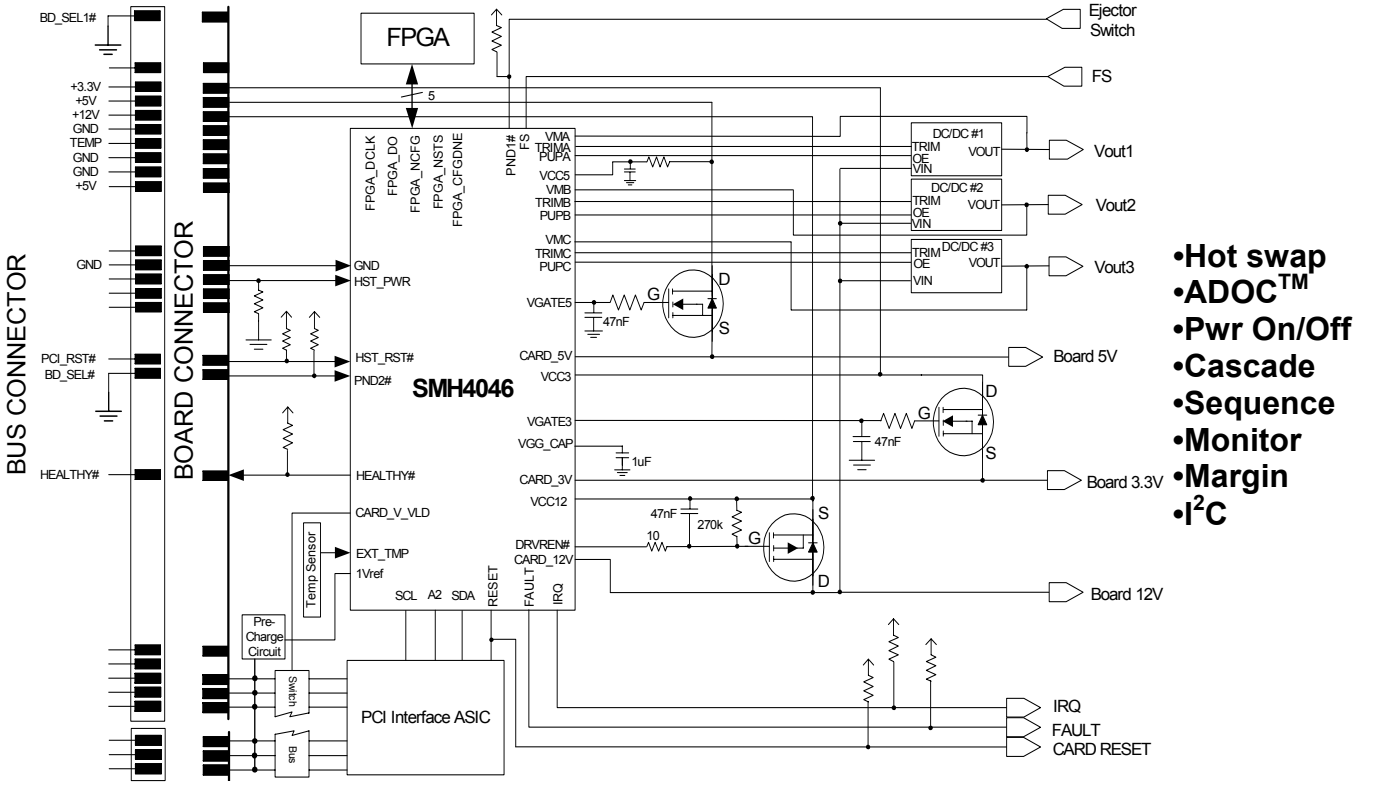


Figure 1 – Applications Schematic using the SMH4046 Controller to hot swap and actively control the output levels of three DC/DC Converters while providing power on/off, cascade sequencing and output margining.

Note: This is an applications example only. Some pins, components and values are not shown.

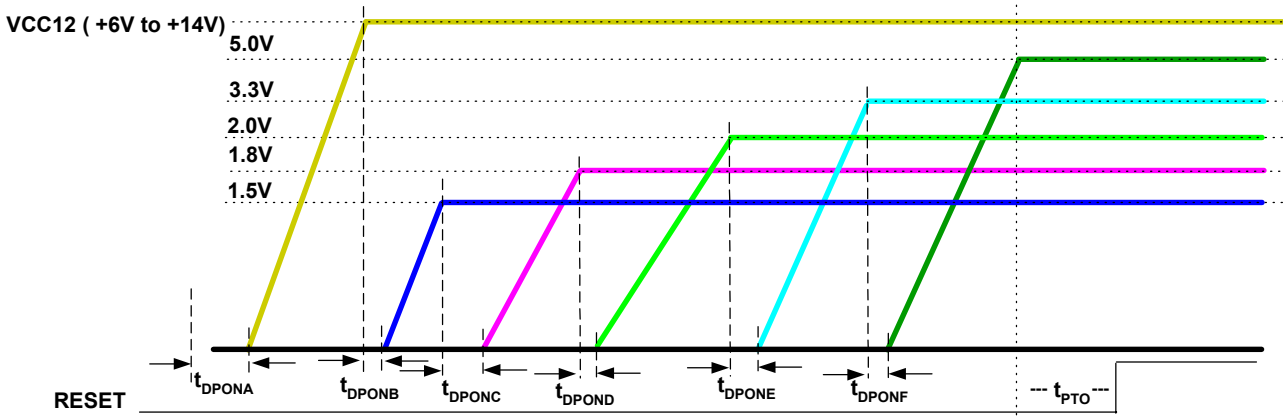


Figure 2 – Example Power Supply Cascade Sequencing and System Initialization Using the SMH4046

GENERAL DESCRIPTION

The SMH4046 is a fully integrated hot swap controller intended for use on add-in cards that are hot swapped from powered-on host platforms. The SMH4046 performs a variety of tasks starting with the validation of proper card insertion and the presence of "in-spec" voltages at the host platform interface.

Once the SMH4046 switches power on, it continues to monitor the back-end power to the add-in card and the host power supply. When programmed to do so, the SMH4046 immediately asserts the RESET outputs and powers-down the add-in card when the 12V, 5V or 3.3V supplies drop below a programmable UV or above an OV threshold.

In addition to the power control for the add-in card, the SMH4046 provides status signals that can be employed by the host for the control of bus interface components.

On-chip EEPROM memory can be used to store serial ID numbers or other pertinent information for the individual card or as general-purpose memory. The FPGA configuration-interface provides a direct interface for simplified access to the add-in card's FPGAs using the I^2C interface.

The SMH4046 has the ability to monitor and sequence up to six power supplies (Figure 1). The SMH4046 can monitor the 12V input and the internal and external temperature sensors. The SMH4046 has four operating modes: Power-on sequencing mode, monitor and control mode using Active DC Output Control (ADOC), supply margining mode using ADOC, and Power-off sequencing mode.

Power-on sequencing can be initiated via the HST_PWR pin or through the serial interface. In this mode, the SMH4046 sequences the power supply channels on in any order by activating the PUPx, VGATE and DRVREN# outputs while monitoring the respective converter and host voltages to ensure correct cascading of the supplies. Cascade-sequencing is the ability to hold off the next sequenced supply until the previous supply reaches a programmed threshold voltage (See Figure 2). A programmable sequence termination timer can be set to disable all channels if the power-on sequence stalls. During this mode, the HEALTHY# output remains inactive and the RESET output remains active. When the HEALTHY# output is true and RESET is false, that signals the end of power-on sequencing mode.

Once the Power-on sequencing mode is complete, the SMH4046 enters monitor control mode. Once all supplies have sequenced on and the voltages are above the UV settings, the Active DC Output Control (ADOC), if enabled, brings the three DC-DC converter supply output voltages to their programmed nominal settings and adjusts the output voltage under all load conditions. This feature is especially useful for supplies without sense lines as the monitor VMx pins can be routed and sense variations at the load. Typical converters have ±2 to ±5% accuracy output voltage ratings. The Active DC Output Control feature of the SMH4046 increases the accuracy to ±0.5%.

GENERAL DESCRIPTION (CONTINUED)

The device also triggers outputs by monitoring fault conditions. The 10-bit ADC cycles through all channels every 2 ms and checks the conversions against the programmed threshold limits. The results can be used to trigger the RESET, HEALTHY# and FAULT outputs as well as to trigger a power-off or a force- shutdown operation.

While the SMH4046 is in monitoring mode, a serial interface command to margin the supply voltages can bring the part into margining mode. In margining mode the SMH4046 can margin the three supply voltages in any combination of nominal, high or low voltage settings using the ADOC feature, all to within ±0.5%. The margin high and margin low voltage settings can range from 0.9V to the overvoltage limit of the DC-DC converters and depends on the margin range of the converters. During this mode the HEALTHY# output is always active and the RESET output is always inactive regardless of the voltage threshold limit settings and triggers. Furthermore, the triggers for power-off and force-shutdown are temporarily disabled.

The power-off sequencing mode can only be entered while the SMH4046 is in the monitoring mode. It can be initiated by either bringing the HST_PWR pin inactive, through the serial interface control, or triggered by a channel exceeding its programmed thresholds. Once power-off is initiated, active DC control is disabled, and the PUP outputs are sequenced off in either the same or reverse order as power-on sequencing. Monitoring of the supply voltages continues to ensure cascading of the supplies as they turn off. The sequence termination timer can be programmed to immediately disable all channels if the power-off sequencing stalls. The RESET output remains active throughout this mode while the HEALTHY# output remains inactive.

The CARD_3V and CARD_5V monitor pins are also used to detect overcurrents on the card side 3V and 5V supply. The FAULT pin is a programmable active high/low open drain fault output that is asserted by the SMH4046 when a programmed fault condition occurs on the internal/external temperature sensor. If programmed to do so, FAULT is asserted whenever an over-current condition is detected. Fault will be released at the same time that the VGATE outputs are turned back on after a reset from the host on the HST_PWR pin. Programming is accomplished by using the I^2C serial bus interface.

INTERNAL FUNCTIONAL BLOCK DIAGRAM

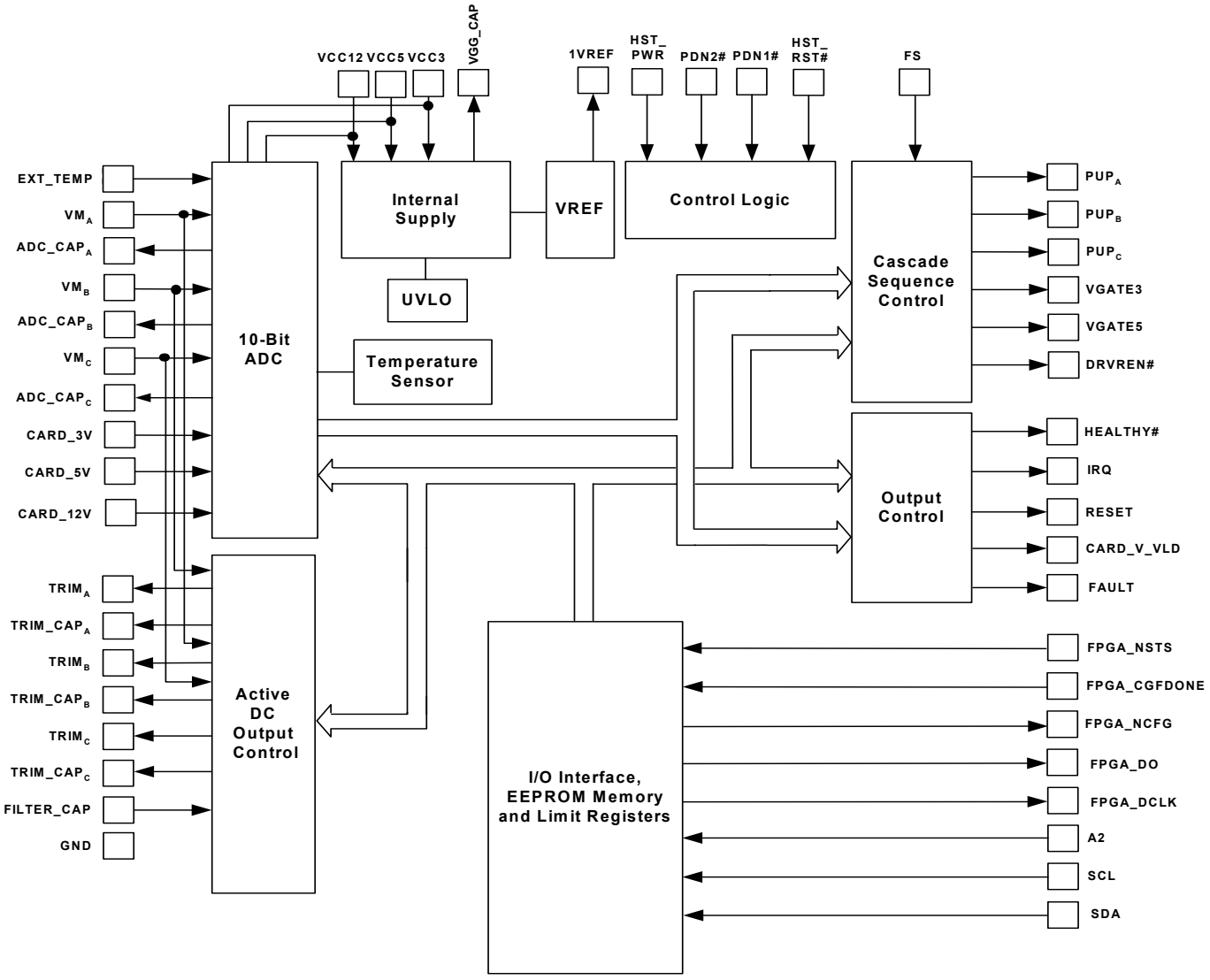


Figure 3 – Internal Functional Block Diagram

PIN DESCRIPTIONS

Symbol	Pin	Type	Description
SCL	1	I	The I^2C serial bus clock.
A2	2	I	An external address bit for I^2C.
HST_RST	3	I	Host reset. This input is the reset signal from the host interface. Asserting this pin causes a reset sequence to be performed on the card. Programmable polarity.
HST_PWR	4	I	Host power-up enable. This input provides the host system with active control over the sequencing of the power up operation. When de-asserted, the SMH4046 holds the add-in card in reset and blocks all power to the back-end logic. When HST_PWR is asserted, the power sequencing begins immediately and the reset output is driven active after the time tPURST. Programmable polarity.
FS	5	I	Force Shutdown. This programmable active high/low input is used to immediately turn off all converter enable signals and external FETs.
EXT_TEMP	6	I	This input can be used to sense a voltage generated from an external temperature monitoring device.
IRQ#	7	O	Active low Interrupt output. Generated by the SMH4046 on an error condition. This signal can be used by external logic to interrupt the host.
RESET (RST)	8	O	RESET is a programmable active high/low open drain output that is asserted by the SMH4046 when a programmed reset condition occurs.
FAULT	9	O	FAULT is a programmable active high/low open drain fault output that is asserted by the SMH4046 when a programmed fault condition occurs.
HEALTHY	10	O	Healthy is a programmable active high/low open drain output that is asserted by the SMH4046 when all programmed healthy conditions are met.
GND	11	PWR	Ground.
PND1#	12	I	Pin detect 1 is an active low CMOS level input. In conjunction with PND2#, this signal indicates proper card insertion when taken low. This pin must be connected to ground on the host side of the connector. PND1# and PND2# should be placed on opposite corners of the connector and will preferably be staggered shorter than the power connector pins. Board insertion is assumed when PND1# and PND2# are low.
PND2#	13	I	Pin detect 2 is an active low CMOS level input. In conjunction with PND1#, this signal indicates proper card insertion when taken low. This pin must be connected to ground on the host side of the connector. PND1# and PND2# should be placed on opposite corners of the connector and will preferably be staggered shorter than the power connector pins. Board insertion is assumed when PND1# and PND2# are low.
CARD_V_VLD	14	O	Card voltage valid. This open drain output indicates that the card side voltages are at or above their respective trip levels. Active high.
VMA	15	I	Positive converter sense line for DC/DC converter A
TRIMA	16	O	Output voltage used to control the output of DC/DC converter A.
TRIM_CAPA	17	I	External sample and hold capacitor input used to set the voltage on the TRIMA pin.

PIN DESCRIPTIONS (CONTINUED)

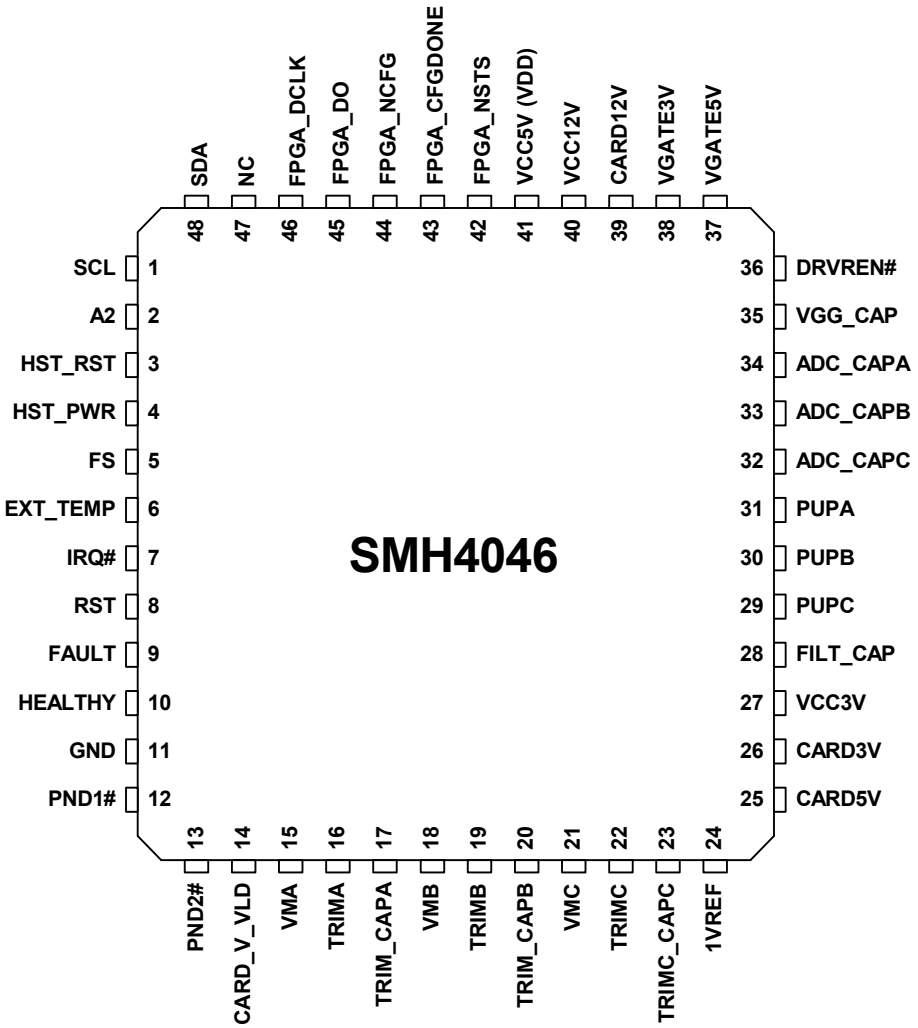
Symbol	Pin	Type	Description
VMB	18	I	Positive converter sense line for DC/DC converter B
TRIMB	19	O	Output voltage used to control the output of DC/DC converter B.
TRIM_CAPB	20	I	External sample and hold capacitor input used to set the voltage on the TRIMB pin.
VMC	21	I	Positive converter sense line for DC/DC converter C
TRIMC	22	O	Output voltage used to control the output of DC/DC converter C.
TRIM_CAPC	23	I	External sample and hold capacitor input used to set the voltage on the TRIMC pin.
1VREF	24	O	This output provides a 1V reference for pre-charging the CompactPCI bus signal pins.
CARD_5V	25	I	5V card side supply input. This input is monitored for power integrity. If it falls below the 5V sense threshold, the CARD_V_VLD signal is de-asserted.
CARD_3V	26	I	3.3V monitor input from the line card. This input is monitored for power integrity. If it falls below the 3.3V sense threshold, the CARD_V_VLD signal is de-asserted.
VCC3V	27	I	3.3V host side supply input. This input is monitored for power integrity.
FILT_CAP	28	I	External capacitor input used to filter VMX inputs
PUPC	29	O	Programmable active high/low open drain converter enable output for DC/DC converter C.
PUPB	30	O	Programmable active high/low open drain converter enable output for DC/DC converter B.
PUPA	31	O	Programmable active high/low open drain converter enable output for DC/DC converter A.
ADC_CAPC	32	I	External capacitor input used to filter the VMC input to the 10-bit ADC.
ADC_CAPB	33	I	External capacitor input used to filter the VMB input to the 10-bit ADC.
ADC_CAPA	34	I	External capacitor input used to filter the VMA input to the 10-bit ADC.
VGG_CAP	35	O	This pin supplies power for the high-side drivers. An external 1uF ceramic charge pump capacitor should be connected to VGG_CAP. VGG_CAP is a charge storage connection for the internal charge pump of the SMH4046. This capacitor should be of sufficient size to provide current to the VGATE outputs high side drivers under varying load conditions. For most applications this can be tied to a 1.0 μF ceramic capacitor.
DRVREN#	36	O	High-side driver enable used to switch on the 12V supply. Pulldown current of 100μA when on.
VGATE5V	37	O	5V gate output. Slew rate limited high side driver output for the 5V external Power FET gate. Alternatively this can be used as a PUP output.
VGATE3V	38	O	3.3V gate output. Slew rate limited high side driver output for the 3.3V external Power FET gate. Alternatively, this can be used as a PUP output.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Pin	Type	Description
CARD_12V	39	I	12V card side supply input. This input is monitored for power integrity. If it falls below the 12V sense threshold, the CARD_V_VLD signal is de-asserted.
VCC12	40	I	Bus-side 12V input
VCC5V (VDD)	41	PWR	This pin supplies power to the SMH4046 and is monitored for power integrity.
FPGA_NSTS	42	I	FPGA configuration status input pin
FPGA_CFGDONE	43	I	FPGA_CFGDONE indicates completion of the configuration process.
FPGA_NCFG	44	O	FPGA_NCFG is a configuration control output. A low transition resets the target device; a low-to-high transition begins configuration.
FPGA_DO	45	O	FPGA_DO provides preamble and configuration data to downstream devices in a daisy-chain.
FPGA_DCLK	46	O	FPGA Configuration clock output. Clock output used to clock configuration data using pin FPGA_DO.
NC	47	NC	No Connect
SDA	48	I/O	The bidirectional I^2C serial data line.

PACKAGE AND PIN CONFIGURATION

48 LEAD TQFP



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to 125°C

Storage Temperature..... -65°C to 150°C

Terminal Voltage with Respect to GND:

- VCC3/5 Supply Voltage .....-0.3V to 6.0V
- VCC12 Supply Voltage .....-0.3V to 15.0V
- Open Drain Outputs..…….…. GND to 15.0V
- All Others .....V_{DD} + 0.7V

Output Short Circuit Current 100mA

Reflow Solder Temperature (30 secs)..... 240°C

Lead Solder Temperature (10 secs) ……300°C

Junction Temperature.....…….....…...150°C

ESD Rating per JEDEC……..……..……..2000V

Latch-Up testing per JEDEC……..……...…±100mA

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial).....–40°C to +85°C

(Commercial) .....0°C to +70°C

VCC3V Supply Voltage..... 2.7V to 5V

VCC5V Supply Voltage..... 2.7V to 6V

VCC12V Supply Voltage… ……..…....6.0V to 14.0V

VIN ..... GND to VCC5

VOUT ..... GND to 15.0V

Package Thermal Resistance (θ_{JA})

48 Lead TQFP……..…80°C/W

Moisture Classification Level 1 (MSL 1) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention……..….100 Years

Endurance……100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
VCC3	Supply Voltage Monitor	Not a supply input	2.7	3.3	5.0	V
VCC5	Supply Voltage	VCC5 must be higher then any other input except VCC12 and CARD12V	2.7	5.0	6.0	V
VCC12	Supply Voltage Monitor	Not a supply input	6	12	14	V
VMx	Positive sense voltage for VMA, VMB and VMC		-0.3		VCC5V	
I_{DD}	Power Supply Current	All TRIM pins floating		3	5	mA
I_{TRIM}	TRIMA, TRIMB, TRIMC current	TRIMx pin sourcing current	1.5			mA
		TRIMx pin sinking current	1.5			mA
V_{TRIM}	Margin Control and ADOC Range	I_{TRIM} ±1.5mA, Depends on Trim range of DC-DC Converter	GND		VCC5V	V
V_{IH}	Input High Voltage	VCC5V = 2.7V	0.9xVCC5V		VCC5V	V
		VCC5V = 5.0V	0.7xVCC5V		VCC5V	V
V_{IL}	Input Low Voltage	VCC5V = 2.7V			0.1xVCC5V	V
		VCC5V = 5.0V			0.3xVCC5V	V
V_{OL}	Programmable Open Drain Outputs	I_{SINK} = 1mA		0.2		V

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
VGATE	VGATE3/5 Outputs			12		V
V_{SENSE}	Positive Sense Voltage	VM pin	+0.3		VCC5V	V
$V_{Monitor}$	Monitor Threshold Step Size	VM pins		5		mV
$T_{Monitor}$	Temperature Threshold Step Size	Internal Temp Sensor		1		°C
T_{SA}	Internal Temperature Sensor Accuracy	Commercial Temp Range	-3		+3	°C
		Industrial Temp Range	-5		+5	°C
$1V_{REF}$	$1V_{REF}$ Output Voltage	Optional data bus pre-charge output	0.95	1.00	1.05	V
V_{REF} ACC	Internal V_{REF} Accuracy		-0.4		+0.4	%
$ADOC_{ACC}$	ADOC/Margin Accuracy	$V_{SENSE} \leq 3.5V$	-0.5	±0.3	+0.5	%
		$V_{SENSE} \geq 3.5V$	-1	±0.8	+1	%
UVLO	Under Voltage Lockout Threshold[1]	VDD_CAP Rising		2.6		V
		VDD_CAP Falling		2.5		V
Note 1 - (100mV typ Hysteresis)						
ADC characteristics						
N	Resolution		10			Bits
MC	Missing Codes	Minimum resolution for which no missing codes are guaranteed	10			Bits
S/N	Signal-to-Noise Ratio	Conversion rate = 500Hz		72		db
DNL	Differential Non-Linearity		-1/2		+1/2	LSB
INL	Integral Non-Linearity		-1		+1	LSB
GAIN	Positive full scale gain error		-0.5		+0.5	%
Offset	Offset Error		-1		+1	LSB
ADC_TC	Full Scale Temperature Coefficient			±15		PPM/°C
IM_{ADC}	Analog ADC Input Impedance	EXT_TEMP		10		MΩ

The formula for the total ADC inaccuracy is: [((ADC read voltage) +/- INL)*(range of gain error)]+range of offset error

AC OPERATING CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND. See Figure 5A and 5B Timing diagrams.

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{DOCT}	Programmable Over Current Trip Delay Time	t_{DOCT} = 5.5 µs	-15	t_{DOCT}	+15	%
		t_{DOCT} = 8.5 µs				
		t_{DOCT} = 11.5 µs				
		t_{DOCT} = 14.5 µs				
		t_{DOCT} = 17.5 µs				
		t_{DOCT} = 20.5 µs				
		t_{DOCT} = 23.5 µs				
		t_{DOCT} = 26.5 µs				
		t_{DOCT} = 29.5 µs				
		t_{DOCT} = 32.5 µs				
		t_{DOCT} = 35.5 µs				
		t_{DOCT} = 38.5 µs				
		t_{DOCT} = 41.5 µs				
		t_{DOCT} = 44.5 µs				
		t_{DOCT} = 47.5 µs				
		t_{DOCT} = 50.5 µs				
t_{DPON}	Programmable Power-on delay from VM_X out-of-fault to PUP_Y active	t_{DPON} = 1 ms	-15	t_{DPON}	+15	%
		t_{DPON} = 20 ms				
		t_{DPON} = 40 ms				
		t_{DPON} = 75 ms				
t_{DPOFF}	Programmable Power-off delay from VM_X off to PUP_Y inactive	t_{DPOFF} = 1 ms	-15	t_{DPOFF}	+15	%
		t_{DPOFF} = 20 ms				
		t_{DPOFF} = 40 ms				
		t_{DPOFF} = 75 ms				
t_{PRTO}	Programmable Reset Time-Out Period	t_{PRTO} = 1 ms	-15	t_{PRTO}	+15	%
		t_{PRTO} = 40 ms				
		t_{PRTO} = 150 ms				
		t_{PRTO} = 300 ms				
t_{STT}	Programmable Sequence Termination Timer	t_{STT} = 40 ms	-15	t_{STT}	+15	%
		t_{STT} = 75 ms				
		t_{STT} = 150 ms				
		t_{STT} = 300 ms				
t_{ADC}	10-bit ADC sampling period	Time for ADC conversion of all 11 channels		2		ms
$t_{DC\_CONTROL}$	Active DC Control sampling period	Update period for Active DC Control of channels A – C		1.7		ms
T_{MARGIN}	Margin Time from Nominal	Slow Margin, ± 10% change in voltage with 0.1% ripple TRIM_CAP=1µF		850		ms
		Fast Margin, ± 10% change in voltage with 0.1% ripple TRIM_CAP=1µF		85		ms

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS – 100kHz

Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND. See Figure 4 Timing Diagram.

Symbol	Description	Conditions	100kHz			
			Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency		0		100	KHz
t_{LOW}	Clock Low Period		4.7			µs
t_{HIGH}	Clock High Period		4.0			µs
t_{BUF}	Bus Free Time	Before New Transmission - Note 1/	4.7			µs
$t_{SU:STA}$	Start Condition Setup Time		4.7			µs
$t_{HD:STA}$	Start Condition Hold Time		4.0			µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7			µs
t_{AA}	Clock Edge to Data Valid	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data Output Hold Time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA Rise Time	Note 1/			1000	ns
t_F	SCL and SDA Fall Time	Note 1/			300	ns
$t_{SU:DAT}$	Data In Setup Time		250			ns
$t_{HD:DAT}$	Data In Hold Time		0			ns
TI	Noise Filter SCL and SDA	Noise suppression		100		ns
t_{WR_CONFIG}	Write Cycle Time Config	Configuration Registers			10	ms
t_{WR_EE}	Write Cycle Time EE	Memory Array			5	ms

Note: 1/ - Guaranteed by Design.

TIMING DIAGRAMS

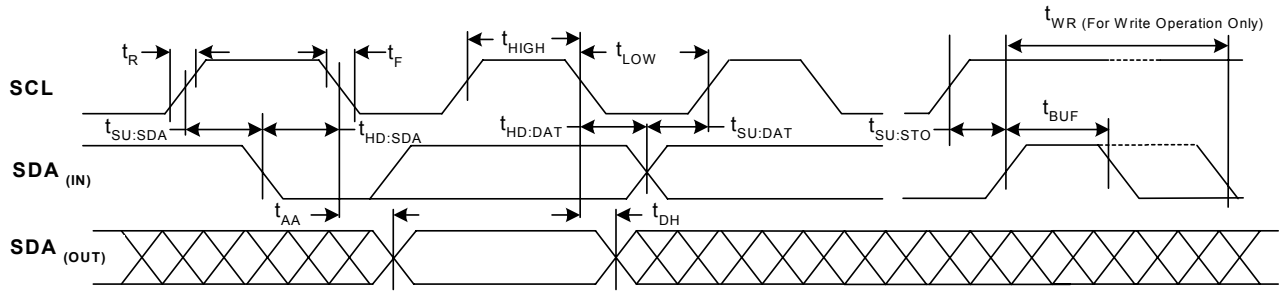


Figure 4 - Basic I²C Serial Interface Timing

TIMING DIAGRAMS (CONTINUED)

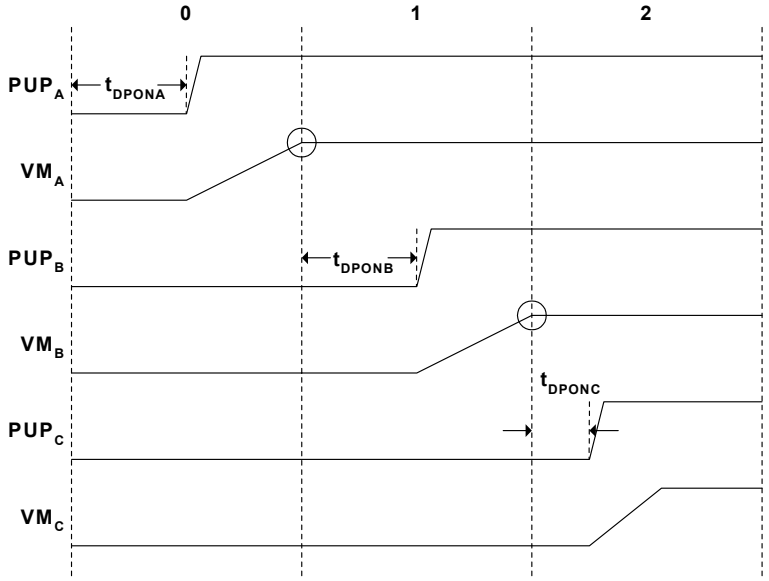


Figure 5A - Cascade Sequencing the Supplies On and then Monitoring for Fault Conditions

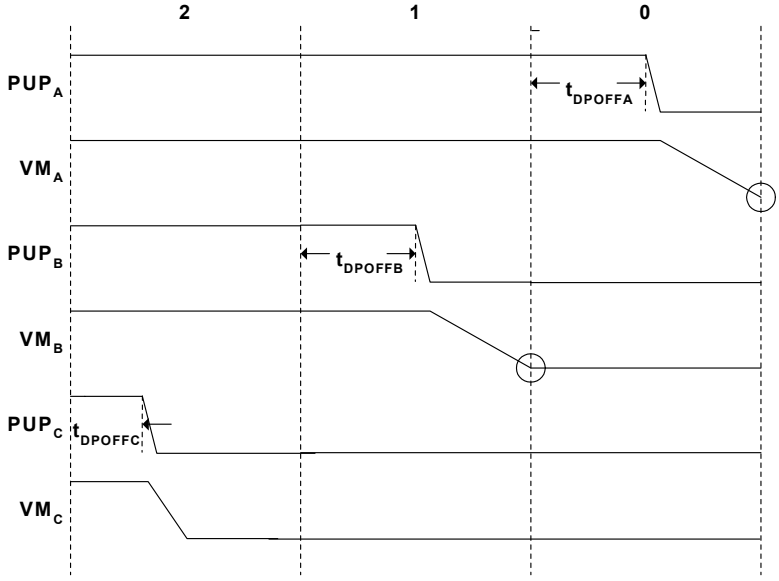


Figure 5B - Cascade Sequencing the Supplies Off

APPLICATIONS INFORMATION

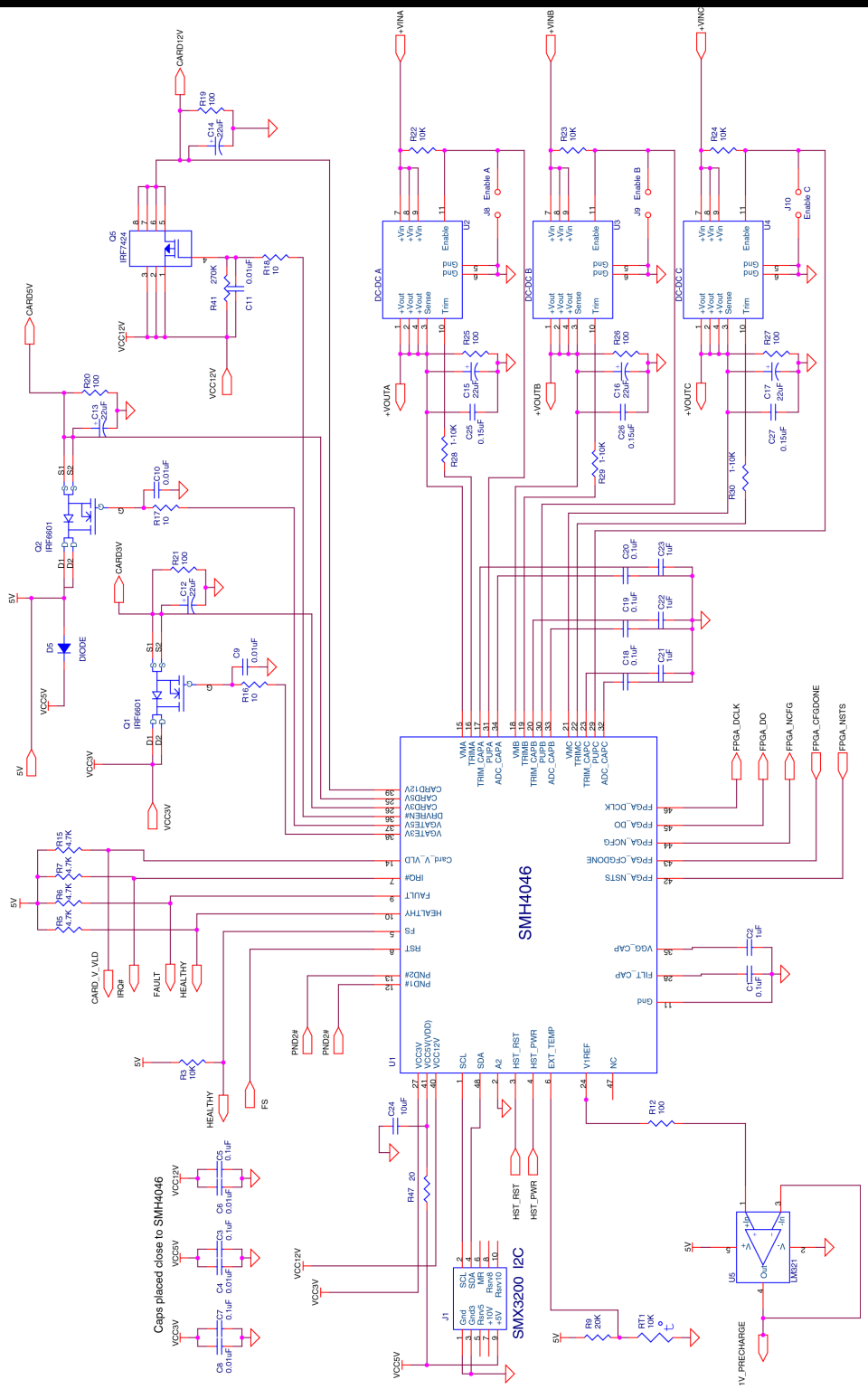


Figure 6 - Typical Applications Schematic

APPLICATIONS INFORMATION (CONTINUED)

Using the schematic in Figure 6 and assuming all input voltages are within the programmed limits, application of power to the SMH4046 will enable all DC-DC converters according to the sequence programmed for each channel in the SMH4046. An I^2C software Power-On command can also be used to enable the DC-DC converters. The waveforms in Figure 7 were generated using Channel 1 (12V output) for the time-base trigger. Note the outputs are asserted once the pre-programmed time limit is passed.

Conversely, the SMH4046 can issue an I^2C Power-Off command (Figure 8). The SMH4046 reverses the Power-Off sequence; that is, the first supply to shut off is the last to have turned on (Channel 4 in this case). As displayed in Figure 8, the supplies are turned off in reverse order of the turn-on sequence.

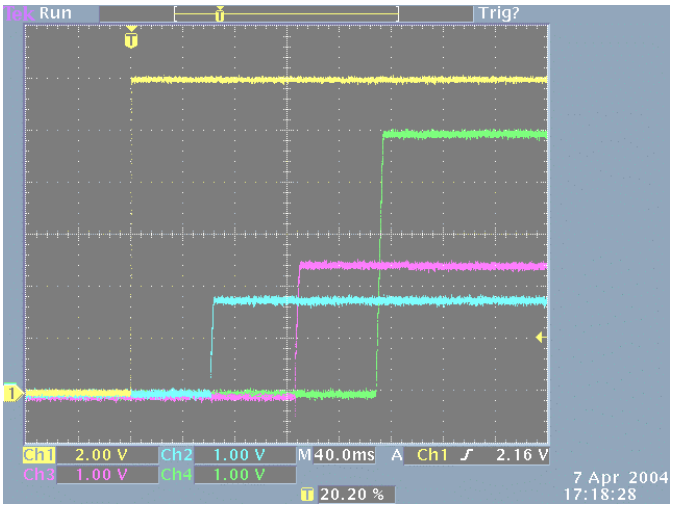


Figure 7: SMH4046EV Sequence-On Waveforms
Tektronix TDS3054: Time/Horizontal division = 40mS
Ch 1(2V/Div) = 12V output (Yellow trace)
Ch 2 (1V/Div) = 1.8V DC-DC converter output (Blue trace)
Ch 3 (1V/Div) = 2.5V DC-DC converter output (Purple trace)
Ch 4 (1V/Div) = 5.0V output (Green trace)

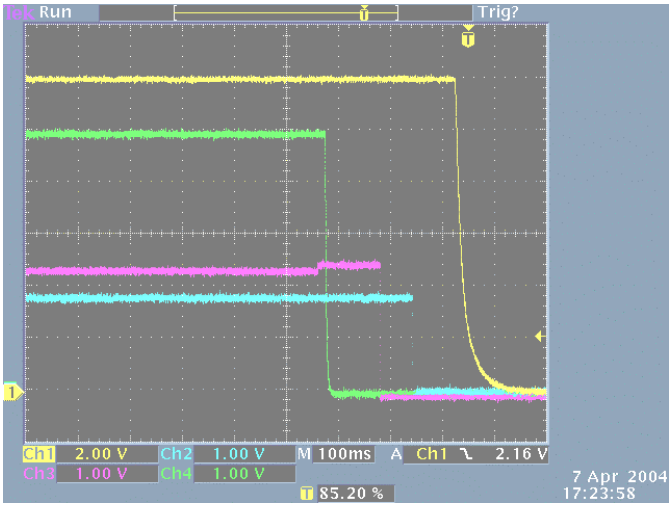


Figure 8: SMH4046EV Sequence-Off Waveforms
Tektronix TDS3054: Time/Horizontal division = 100mS
Ch 1(2V/Div) = 12V output (Yellow trace)
Ch 2 (1V/Div) = 1.8V DC-DC converter output (Blue trace)
Ch 3 (1V/Div) = 2.5V DC-DC converter output (Purple trace)
Ch 4 (1V/Div) = 5.0V output (Green trace)

The SMH4046's has many features including the ability to change the channel sequence positions and slew-rates for system flexibility and software programmability to simplify changes. Figure 9 displays the SMH4046 margining the 2.5V converter high and the 1.8V converter low.

APPLICATIONS INFORMATION (CONTINUED)

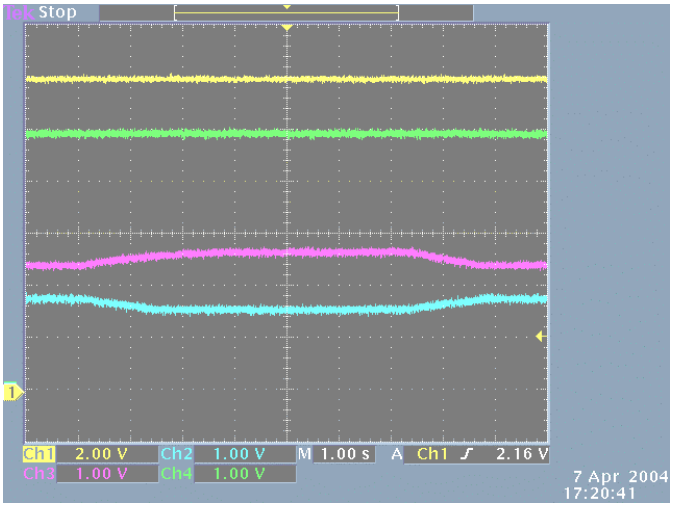


Figure 9: SMH4046EV Margining Waveforms
Tektronix TDS3054: Time/Horizontal division = 1S
Ch 1(2V/Div) = 12V output (Yellow trace)
Ch 2 (1V/Div) = 1.8V DC-DC converter output (Blue trace)
Ch 3 (1V/Div) = 2.5V DC-DC converter output (Purple trace)
Ch 4 (1V/Div) = 5.0V output (Green trace)

Figure 10 displays the SMH4046 shutting the power supplies (Force Shutdown) during the Sequence-On interval due to the time-out of the Sequence Termination Timer.

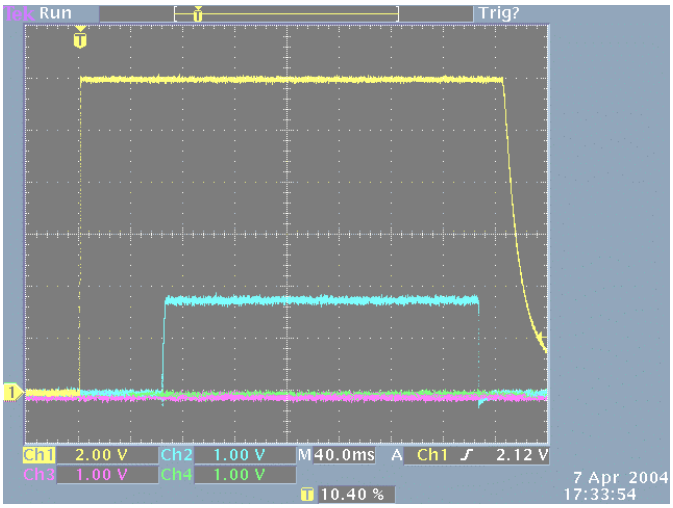


Figure 10: SMH4046EV Forced Sequence-Off
Tektronix TDS3054: Time/Horizontal division = 40mS
Ch 1(2V/Div) = 12V output (Yellow trace)
Ch 2 (1V/Div) = 1.8V DC-DC converter output (Blue trace)
Ch 3 (1V/Div) = 2.5V DC-DC converter output (Purple trace)
Ch 4 (1V/Div) = 5.0V output (Green trace)

COMMENTS & PRECAUTIONS

The SMH4046 is a precision integrated circuit requiring certain attention is spent with regards to component selection and printed circuit board layout to ensure the greatest possible performance. Bypass all DC-DC converter outputs with a suitable low value capacitor to decrease the high frequency noise and thereby improve the SMH4046's accuracy.

Locate the VCC bypass capacitors nearby the SMH4046 returning the low side directly to a ground pin on the device. Do the same for the bulk capacitor for the DC-DC converter inputs, the 3.3V and 12V inputs; if used. Add an additional low value bypass capacitor if the supplies are noisy.

VCC5 Noise

Noise introduced onto the supply (VCC5 pin) of the SMH4046 by the DC/DC converters or other sources may affect the ADC and ADOC^{tm} (margining) accuracy. The result is that the ADC reading and final ADOC^{tm} (margined) voltage may exhibit an error or the actual ADOC voltage may differ noticeably from the target value. To obtain more accurate results, an external series 20Ω (R47 in Figure 6) resistor should be added in series between the VCC5 pin 41 and the supply voltage and a 10µF ceramic bypass capacitor (C24 in Figure 6) added from VCC5 to GND to form a low pass filter.

ADC Function – VOUT Noise

The ADC can appear to return erroneous readings when connected to a power supply DC/DC converter output exhibiting a low frequency noise component. Adding additional filter capacitance to the VMX pins 15, 18 and 21 can reduce this effect by lowering the corner frequency of the low pass filter (C25, C26 and C27 in Figure 6). The maximum recommended value is 150nF.

I²C 2-WIRE SERIAL INTERFACE

Programming Information

I²C Bus Interface

The I²C bus interface is a standard two-wire serial protocol that allows communication between integrated circuits. The data line (SDA) is a bi-directional I/O; the clock line (SCL) runs at speeds of up to 400kHz. The SMH4046 supports a 100 kHz clock rate. The SDA line must be connected to a positive logic supply through a pull-up resistor located on the bus.

Start and Stop Conditions

Both the SDA and SCL pins remain high when the bus is not busy. Data transfers between devices may be initiated with a Start condition. A high-to-low transition of the SDA input while the SCL pin is high is defined as a Start condition. A low-to-high transition SDA while SCL is high is defined as a Stop condition. Figure 11 shows a timing diagram of the start and stop conditions.

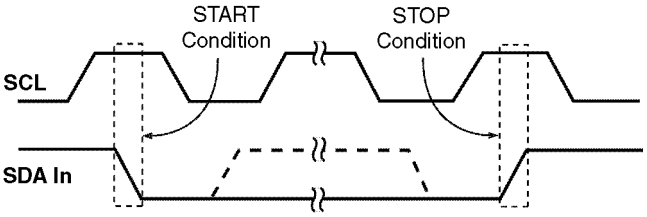


Figure 11 - Start and Stop Conditions

Master/Slave Protocol

The master/slave protocol defines any device that sends data onto the bus as a transmitter, and any device that receives data as a receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the SMH4046 is referred to as a Slave device since it never initiates any data transfers. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because a change on the data line while SCL is high is interpreted as either a Start or a Stop condition.

Acknowledge

Data is always transferred in bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The transmitting device releases the bus after transmitting eight bits. During the ninth clock cycle the Receiver pulls the SDA line low to acknowledge that it received the eight bits of data. This is shown by the ACK callout in Figure 12.

When the last byte has been transferred to the Master during a read of the SMH4046, the Master leaves SDA high for a Not Acknowledge (NACK) cycle. This causes the SMH4046 part to stop sending data, and the Master issues a Stop on the clock pulse following the NACK.

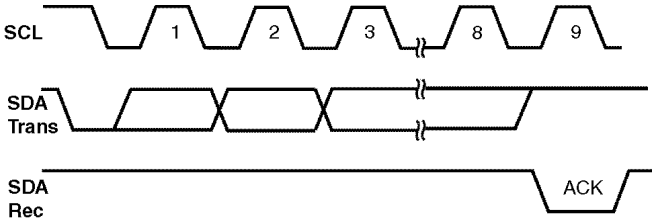


Figure 12 - Acknowledge Timing

Read and Write

The first byte from a Master is always made up of a 7-bit Slave address and the Read/Write (R/W) bit. The R/W bit tells the Slave whether the Master is reading data from the bus or writing data to the bus (1 = Read, 0 = Write). The first four of the seven address bits are called the Device Type Identifier (DTI). In the case of the SMH4046, the next two bits are Bus Address values, used to distinguish multiple devices on a common bus. The seventh bit of the slave address represents the ninth bit of the word address. The SMH4046 issues an Acknowledge after recognizing a Start condition and its DTI. Figure 13 shows an example of a typical master address byte transmission.

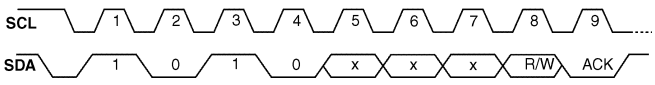


Figure 13 - Typical Master Address Byte Transmission

I²C 2-WIRE SERIAL INTERFACE (CONTINUED)

During a read by the Master device, the SMH4046 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SMH4046 continues to transmit data. If an Acknowledge is not detected (NACK), the SMH4046 terminates any subsequent data transmission. The read transfer protocol on SDA is shown in Figure 14.

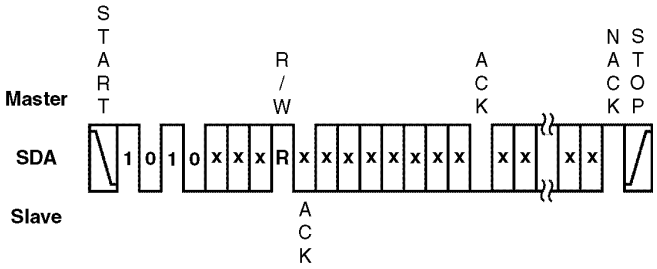


Figure 14 - Read Protocol

During a Master write, the SMH4046 receives eight bits of data, then generates an Acknowledge signal. The device continues to generate the ACK condition on SDA until a Stop condition is generated by the Master. The write transfer protocol on SDA is shown in Figure 15.

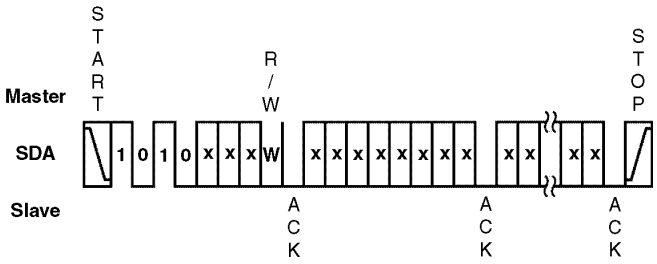


Figure 15 - Write Protocol

Random Access Read

Random address read operations (Figure 16) allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMH4046 to the desired address.

After the word address Acknowledge is received by the Master, it immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SMH4046 responds with an Acknowledge and then transmits the 8 data bits stored at the addressed location. At this point, the Master sets the SDA line to NACK and generates a Stop condition. The SMH4046 discontinues data transmission and reverts to its standby power mode.

Sequential Reads

Sequential reads (Figure 16) can be initiated as either a current address read or a random access read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMH4046.

The SMH4046 continues to output data for each Acknowledge received. The Master sets the SDA line to NACK and generates a Stop condition. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal.

For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter rolls over and the memory continues to output data.

I²C 2-WIRE SERIAL INTERFACE (CONTINUED)

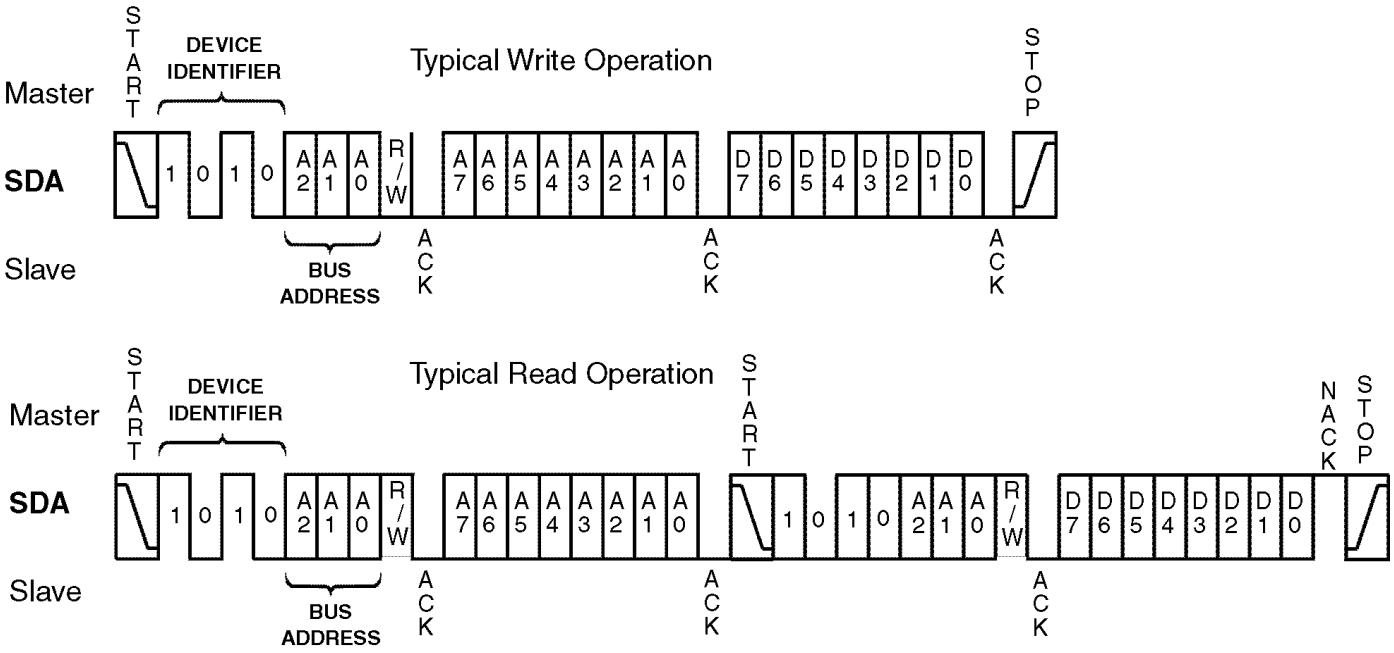


Figure 16 - Typical EE Memory Write and Random Read Operations

FPGA Configuration Interface

The FPGA interface is used to perform configuration of industry standard FPGAs by loading application specific data into the FPGA configuration memory via the SMH4046 FPGA interface. To enable the FPGA interface option, Bit 7 of configuration register hex0C must be set to a 1. Bits [2:0] of register hex84, slave address 1001are write/read bits that are mapped to output pins FPGA_DCLK, FPGA_DO, and FPGA_NCFG, respectively.

A write to these bits will result in the same corresponding state on the output pins. Bits [7:6] are mapped to input pins FPGA_NSTS and FPGA_CFGDONE, respectively. The state of these pins is reflected in the corresponding bits and can be read. The function of each pin is described in Table 1. For more information, see the FPGA data sheet for configuration options.

Symbol	Type	Description
FPGA_NSTS	I	FPGA configuration status input pin
FPGA_CFGDONE	I	FPGA_CFGDONE indicates completion of the configuration process.
FPGA_NCFG	O	FPGA_NCFG is a configuration control output. A low transition resets the target device; a low-to-high transition begins configuration.
FPGA_DO	O	FPGA_DO provides preamble and configuration data to downstream devices in a daisy-chain.
FPGA_DCLK	O	FPGA Configuration clock output. Clock output used to clock configuration data using pin FPGA_DO.

TABLE 1 – FPGA Configuration interface

I²C 2-WIRE SERIAL INTERFACE (CONTINUED)

Register Access

The SMH4046 contains a 2-wire bus interface for register access as explained in the previous section. This bus is highly configurable, while maintaining the industry standard protocol. The SMH4046 responds to one of two selectable Device Type Addresses: 1010_{BIN}, generally assigned to NV-memories and the default address for the SMH4046, or 1011_{BIN}. The Device Type Address is assigned by programming bit 3 of Register 0x0E.

The configuration registers may be locked out by setting bit 7 of register 0x0D high. This is a one-time, non-reversible operation.

The SMH4046 has two virtual address pins, A[1:0] (set with R0E[1:0]), associated with the 2-wire bus.

Slave Address	Bus Address	Register Type
1001_{BIN}	A2 A1 A0	Command and Status Registers, ADC Conversion Readout
1010_{BIN} or 1011_{BIN}	A2 A1 0	2-k Bits of General-Purpose Memory
	A2 A1 1	Configuration Registers

Table 2 - Address bytes used by the SMH4046.

I²C PROGRAMMING INFORMATION (CONTINUED)

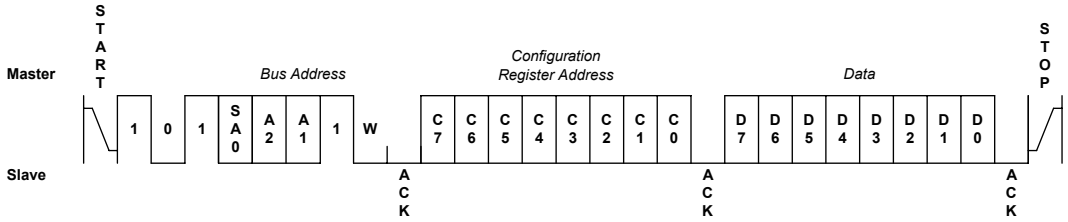
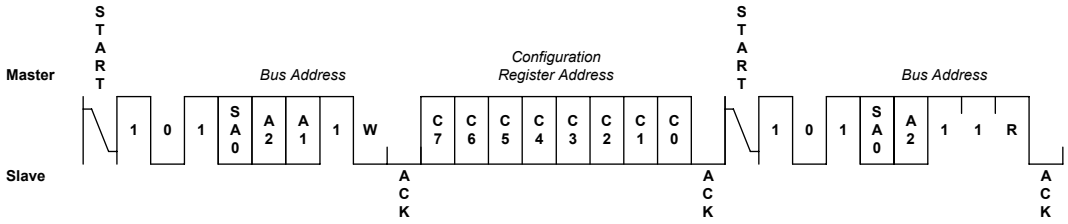


Figure 17 - Configuration Register Byte Write



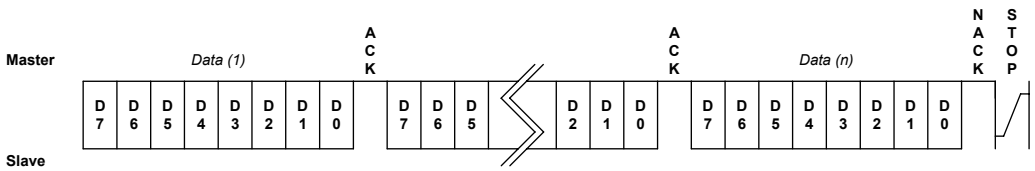


Figure 18 - Configuration Register Read

I²C PROGRAMMING INFORMATION (CONTINUED)

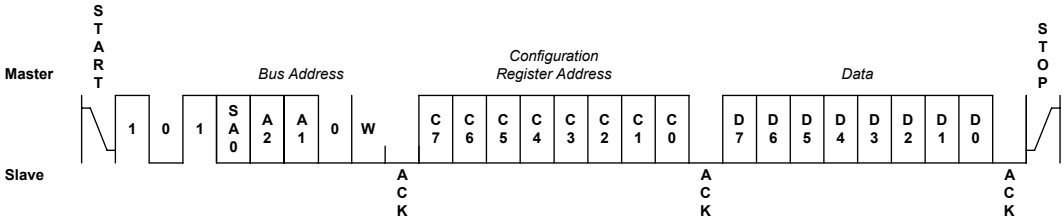


Figure 19 – General Purpose Memory Byte Write

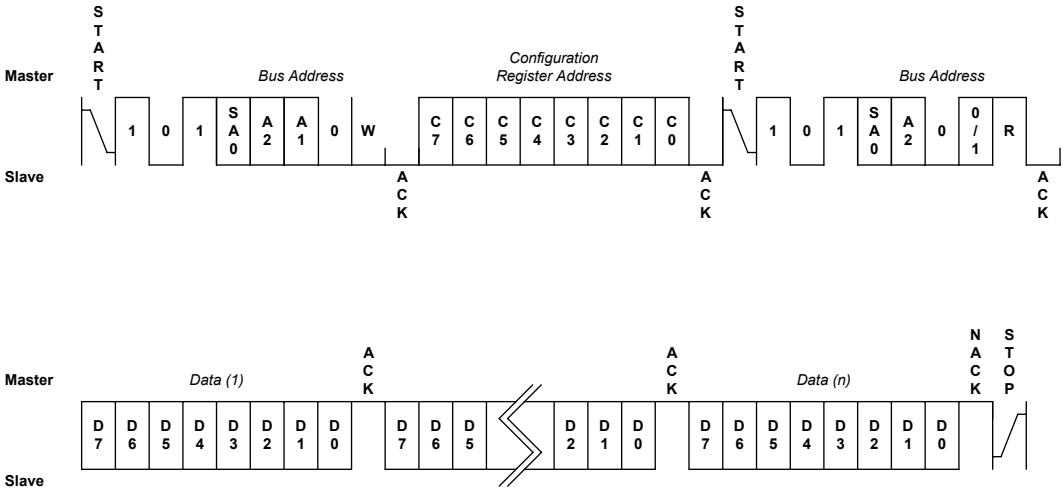


Figure 20 - General Purpose Memory Read

I²C PROGRAMMING INFORMATION (CONTINUED)

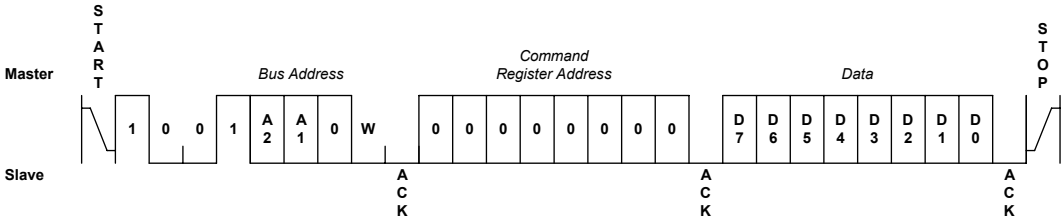
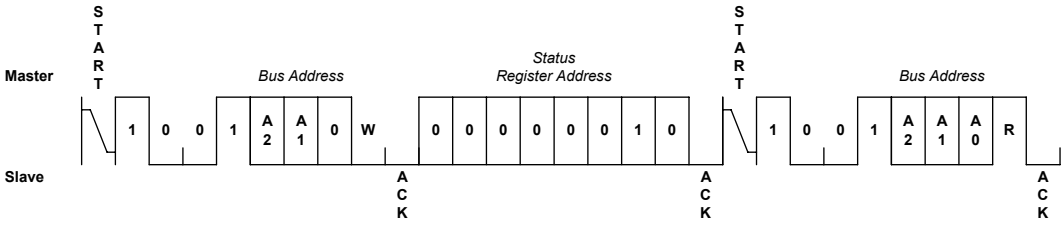


Figure 21 – Command Register Write



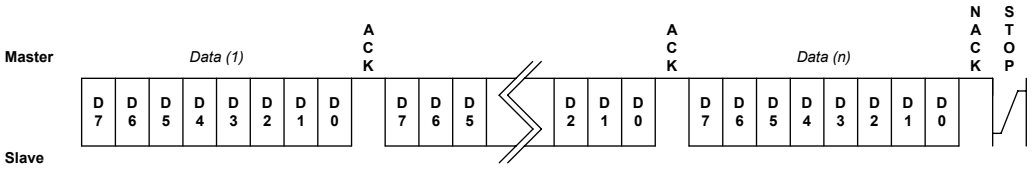


Figure 22 - Status Register Read

I²C DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative.

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I²C serial bus format so that it can be directly downloaded to the SMH4046 via the programming Dongle and cable. An example of the connection interface is shown in Figure 23.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

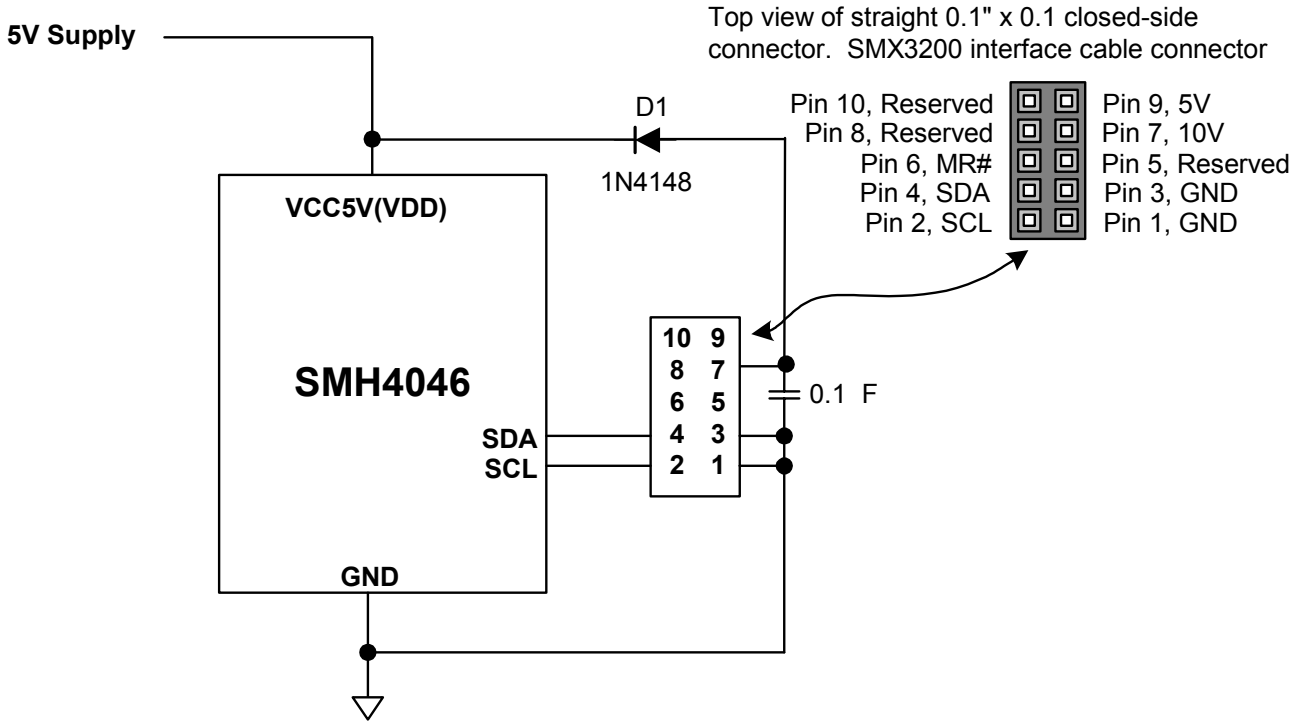


Figure 23 – SMX3200 Programmer I²C serial bus connections to program the SMH4046.

The latest revisions of all software and an application brief describing the SMX3200 is available from the website at:

http://www.summitmicro.com/tech_support/tech.htm#GUI

CONFIGURATION REGISTERS

Configuration Registers:

The configuration registers are accessible via the I^2C interface at slave address 1010 or 1011 and 1001. These registers determine which features of the device are active, set voltage sensing threshold levels, and define the programmable output logic.

The following tables describe the configuration register bits in detail. The following registers are accessed using slave address 101 SA0 A2 A1 1 (SA0 = C_0E[3]).

Register R00 – VREF nominal settings.
Bits D[7:6] are unused and should be set to 00. Bits D[5:4] control the Ch C VREF value. Bits D[3:2] control Ch B VREF and Bits D[1:0] control Ch A VREF.

Register R00								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Unused.
-	**-**	**0**	**0**	**-**	**-**	**-**	**-**	Ch C VREF=0.75 V
-	**-**	**0**	**1**	**-**	**-**	**-**	**-**	Ch C VREF=1.0 V
-	**-**	**1**	**0**	**-**	**-**	**-**	**-**	Ch C VREF=1.25 V
-	**-**	**1**	**1**	**-**	**-**	**-**	**-**	Ch C VREF=2.0 V
-	**-**	**-**	**-**	**1**	**1**	**-**	**-**	Ch B VREF selection Nominal
-	**-**	**-**	**-**	**-**	**-**	**1**	**1**	Ch A VREF selection Nominal

Register R01 – Channel A Nominal Setting.
Bits D[7:0] control the Channel A Margin Nominal setting. The DC Control Voltage setting bits (C[7:0]) are set using C[7:0] = 256 * VREF_CNTL / DC Control Voltage. VREF_CNTL is from register R00.

Register R01								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel A Margin Nominal Bits [7:0]

Register R02 – Channel C Nominal Setting.
Bits D[7:0] control the Channel C Margin Nominal setting

Register R02								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel C Margin Nominal Bits [7:0]

Register R03 – Channel B Nominal Setting.
Bits D[7:0] control the Channel B Margin Nominal setting

Register R03								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel B Margin Nominal Bits [7:0]

CONFIGURATION REGISTERS (CONTINUED)

Register R04 – Over-Current Configuration.
Bit D[7] and D[5] are unused. Bit D[6] controls if OC causes an IRQ and D[4] controls if OC causes a FAULT. Bits D[3:0] control the overcurrent Delay.

Register R04								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Unused
-	**0**	-	-	-	-	-	-	OC does not cause an IRQ
-	**1**	-	-	-	-	-	-	OC causes an IRQ
-	-	**0**	-	-	-	-	-	Unused
-	-	-	**0**	-	-	-	-	OC does not cause a FAULT
-	-	-	**1**	-	-	-	-	OC causes a FAULT
-	-	-	-	**0**	**0**	**0**	**0**	Minimum Overcurrent Delay = 5.5µs, 1LSB=3µs
-	-	-	-	**1**	**1**	**1**	**1**	Maximum Overcurrent Delay = 50.5µs

Register R05 – Overcurrent configuration and fault latch.
Bits D[7:6] control the VDD differential level that causes an OC. Bits D[5:4] control the VCC3 differential level that causes an OC. Bit D[3] controls the 5V OC detection. Bit D[2] controls the 3V OC detection. Bit D[1] controls the FAULT output latch and D[0] is unused.

Register R05								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	-	-	-	-	-	-	50mV differential between VDD and CARD5V causes OC
0	**1**	-	-	-	-	-	-	100mV differential between VDD and CARD5V causes OC
1	**0**	-	-	-	-	-	-	150mV differential between VDD and CARD5V causes OC
1	**1**	-	-	-	-	-	-	250mV differential between VDD and CARD5V causes OC
-	-	**0**	**0**	-	-	-	-	50mV differential between VCC3 and CARD3V causes OC
-	-	**0**	**1**	-	-	-	-	100mV differential between VCC3 and CARD3V causes OC
-	-	**1**	**0**	-	-	-	-	150mV differential between VCC3 and CARD3V causes OC
-	-	**1**	**1**	-	-	-	-	250mV differential between VCC3 and CARD3V causes OC
-	-	-	-	**0**	-	-	-	OC detection on 5V channel OFF
-	-	-	-	**1**	-	-	-	OC detection on 5V channel ON
-	-	-	-	-	**0**	-	-	OC detection on 3V channel OFF
-	-	-	-	-	**1**	-	-	OC detection on 3V channel ON
-	-	-	-	-	-	**0**	-	Fault output is unlatched
-	-	-	-	-	-	**1**	-	Fault output is latched
-	-	-	-	-	-	-	**0**	Unused

CONFIGURATION REGISTERS (CONTINUED)

Register R06 –Healthy Triggers.

Register R06								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Ext Temp fault does not cause a HEALTHY.
1	-	-	-	-	-	-	-	Ext Temp fault causes a HEALTHY.
-	**0**	-	-	-	-	-	-	Internal Temp fault does not cause a HEALTHY.
-	**1**	-	-	-	-	-	-	Internal Temp fault causes a HEALTHY.
-	-	**0**	-	-	-	-	-	CARD12V fault does not cause a HEALTHY.
-	-	**1**	-	-	-	-	-	CARD12V fault causes a HEALTHY.
-	-	-	**0**	-	-	-	-	CARD5V fault does not cause a HEALTHY.
-	-	-	**1**	-	-	-	-	CARD5V fault causes a HEALTHY.
-	-	-	-	**0**	-	-	-	CARD3V fault does not cause a HEALTHY.
-	-	-	-	**1**	-	-	-	CARD3V fault causes a HEALTHY.
-	-	-	-	-	**0**	-	-	VMC fault does not cause a HEALTHY.
-	-	-	-	-	**1**	-	-	VMC fault causes a HEALTHY.
-	-	-	-	-	-	**0**	-	VMB fault does not cause a HEALTHY.
-	-	-	-	-	-	**1**	-	VMB fault causes a HEALTHY.
-	-	-	-	-	-	-	**0**	VMA fault does not cause a HEALTHY.
-	-	-	-	-	-	-	**1**	VMA fault causes a HEALTHY.

Register R0C – Misc Config

Register R0C								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	FPGA feature disabled.
1	-	-	-	-	-	-	-	FPGA selected from register.
-	**0**	-	-	-	-	-	-	ADOC fast convergence disabled.
-	**1**	-	-	-	-	-	-	ADOC fast convergence enabled.
-		**0**	-	-	-	-	-	Unused
-		**0**	-	-	-	-	-	Unused
-	-	-	**0**	-	-	-	-	Unused
-	-	-	**0**	-	-	-	-	Unused
-	-	-	-	**0**	-	-	-	VGATE charge pump not always on.
-	-	-	-	**1**	-	-	-	VGATE charge pump always on.
-	-	-	-	-	**0**	-	-	Channel C Trim polarity normal.
-	-	-	-	-	**1**	-	-	Channel C Trim polarity inverse.
-	-	-	-	-	-	**0**	-	Channel B Trim polarity normal.
-	-	-	-	-	-	**1**	-	Channel B Trim polarity inverse.
-	-	-	-	-	-	-	**0**	Channel A Trim polarity normal.
-	-	-	-	-	-	-	**1**	Channel A Trim polarity inverse.

CONFIGURATION REGISTERS (CONTINUED)

Register R0D – Misc Config.

Register R0D								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**-**	**-**	**-**	**-**	**-**	**-**	**-**	Config registers unlocked.
1	**-**	**-**	**-**	**-**	**-**	**-**	**-**	Config registers locked.
	0							Don't wait for temp within spec.
	1							Wait for temp within spec.
		0						VGATE slew rate is 250V/S.
		1						VGATE slew rate is 1000V/S.
			0					VGATE5 configured as an open drain output.
			1					VGATE5 configured as a high voltage output.
				0				VGATE3 configured as an open drain output.
				1				VGATE3 configured as a high voltage output.
					0			Channel C DC Control/Margining disabled.
					1			Channel C DC Control/Margining enabled.
						0		Channel B DC Control/Margining disabled.
						1		Channel B DC Control/Margining enabled.
							0	Channel A DC Control/Margining disabled.
							1	Channel A DC Control/Margining enabled.

Register R0E – Command and Control Configuration Settings

Register R0E								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Sequence termination time = 40mS
0	**1**	**-**	**-**	**-**	**-**	**-**	**-**	Sequence termination time = 75mS
1	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Sequence termination time = 150mS
1	**1**	**-**	**-**	**-**	**-**	**-**	**-**	Sequence termination time = 300mS
-	**-**	**0**	**0**	**-**	**-**	**-**	**-**	RESET timeout period = 1mS
-	**-**	**0**	**1**	**-**	**-**	**-**	**-**	RESET timeout period = 40mS
-	**-**	**1**	**0**	**-**	**-**	**-**	**-**	RESET timeout period = 150mS
-	**-**	**1**	**1**	**-**	**-**	**-**	**-**	RESET timeout period = 300mS
-	**-**	**-**	**-**	**0**	**-**	**-**	**-**	Slave address = 1010
-	**-**	**-**	**-**	**1**	**-**	**-**	**-**	Slave address = 1011
-	**-**	**-**	**-**	**-**	**0**	**-**	**-**	A2 = 0
-	**-**	**-**	**-**	**-**	**1**	**-**	**-**	A2 = pin level
-	**-**	**-**	**-**	**-**	**-**	**0**	**-**	A1 = 0
-	**-**	**-**	**-**	**-**	**-**	**1**	**-**	A1 = 1
-	**-**	**-**	**-**	**-**	**-**	**1**	**0**	A0 = 0
-	**-**	**-**	**-**	**-**	**-**	**1**	**1**	A0 = 1

CONFIGURATION REGISTERS (CONTINUED)

Register R0F – Command and Control Configuration Settings

Register R0F								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Don't wait for VCC3 out of fault before sequencing.
1	-	-	-	-	-	-	-	Wait for VCC3 out of fault before sequencing.
	0	-	-	-	-	-	-	No write command required for Active Control.
	1	-	-	-	-	-	-	Write command required for Active Control.
-	-	**0**	-	-	-	-	-	Auto Monitor actions wait for ADOC ready.
-	-	**1**	-	-	-	-	-	Auto Monitor actions don't wait for ADOC ready.
-	-	-	**0**	-	-	-	-	Sequence off in reverse order.
-	-	-	**1**	-	-	-	-	Sequence off in same order.
-	-	-	-	**0**	-	-	-	Power off required to clear a Forced Shutdown.
-	-	-	-	**1**	-	-	-	Power off not required to clear a Forced Shutdown.
-	-	-	-	-	**0**	-	-	Abort not allowed during power off.
-	-	-	-	-	**1**	-	-	Abort allowed during power off.
-	-	-	-	-	-	**0**	-	Don't wait for 12VIN out of fault before sequencing.
-	-	-	-	-	-	**1**	-	Wait for 12VIN out of fault before sequencing.
-	-	-	-	-	-	-	**0**	Don't wait for VDD out of fault before sequencing.
-	-	-	-	-	-	-	**1**	Wait for VDD out of fault before sequencing.

Register R10 – PUPA Configuration.

Register R10								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Channel A not used in sequencing
1	-	-	-	-	-	-	-	Channel A used in sequencing
-	**0**	**0**	**0**	-	-	-	-	Channel A assigned to sequence position 0
-	**0**	**0**	**1**					Channel A assigned to sequence position 1
-	**0**	**1**	**0**	-	-	-	-	Channel A assigned to sequence position 2
-	**0**	**1**	**1**	-	-	-	-	Channel A assigned to sequence position 3
-	**1**	**0**	**0**	-	-	-	-	Channel A assigned to sequence position 4
-	**1**	**0**	**1**	-	-	-	-	Channel A assigned to sequence position 5
-	**1**	**1**	**0**	-	-	-	-	Unused
-	**1**	**1**	**1**	-	-	-	-	Null position (not used in sequencing)
-	-	-	-	**0**	**0**	-	-	Channel A power-on delay time = 1mS
-	-	-	-	**0**	**1**	-	-	Channel A power-on delay time = 20mS
-	-	-	-	**1**	**0**	-	-	Channel A power-on delay time = 40mS
-	-	-	-	**1**	**1**	-	-	Channel A power-on delay time = 75mS
-	-	-	-	-	-	**0**	**0**	Channel A power-off delay time = 1mS
-	-	-	-	-	-	**0**	**1**	Channel A power-off delay time = 20mS
-	-	-	-	-	-	**1**	**0**	Channel A power-off delay time = 40mS
-	-	-	-	-	-	**1**	**1**	Channel A power-off delay time = 75mS

CONFIGURATION REGISTERS (CONTINUED)

Register R11 –PUPB Configuration.

Register R11								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Channel B not used in sequencing
1	-	-	-	-	-	-	-	Channel B used in sequencing
-	**0**	**0**	**0**	-	-	-	-	Channel B assigned to sequence position 0
-	**0**	**0**	**1**					Channel B assigned to sequence position 1
-	**0**	**1**	**0**	-	-	-	-	Channel B assigned to sequence position 2
-	**0**	**1**	**1**	-	-	-	-	Channel B assigned to sequence position 3
-	**1**	**0**	**0**	-	-	-	-	Channel B assigned to sequence position 4
-	**1**	**0**	**1**	-	-	-	-	Channel B assigned to sequence position 5
-	**1**	**1**	**0**	-	-	-	-	Unused
-	**1**	**1**	**1**	-	-	-	-	Null position (not used in sequencing)
-	-	-	-	**0**	**0**	-	-	Channel B power-on delay time = 1mS
-	-	-	-	**0**	**1**	-	-	Channel B power-on delay time = 20mS
-	-	-	-	**1**	**0**	-	-	Channel B power-on delay time = 40mS
-	-	-	-	**1**	**1**	-	-	Channel B power-on delay time = 75mS
-	-	-	-	-	-	**0**	**0**	Channel B power-off delay time = 1mS
-	-	-	-	-	-	**0**	**1**	Channel B power-off delay time = 20mS
-	-	-	-	-	-	**1**	**0**	Channel B power-off delay time = 40mS
-	-	-	-	-	-	**1**	**1**	Channel B power-off delay time = 75mS

Register R12 – PUPC Configuration

Register R12								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Channel C not used in sequencing
1	-	-	-	-	-	-	-	Channel C used in sequencing
-	**0**	**0**	**0**	-	-	-	-	Channel C assigned to sequence position 0
-	**0**	**0**	**1**					Channel C assigned to sequence position 1
-	**0**	**1**	**0**	-	-	-	-	Channel C assigned to sequence position 2
-	**0**	**1**	**1**	-	-	-	-	Channel C assigned to sequence position 3
-	**1**	**0**	**0**	-	-	-	-	Channel C assigned to sequence position 4
-	**1**	**0**	**1**	-	-	-	-	Channel C assigned to sequence position 5
-	**1**	**1**	**0**	-	-	-	-	Unused
-	**1**	**1**	**1**	-	-	-	-	Null position (not used in sequencing)
-	-	-	-	**0**	**0**	-	-	Channel C power-on delay time = 1mS
-	-	-	-	**0**	**1**	-	-	Channel C power-on delay time = 20mS
-	-	-	-	**1**	**0**	-	-	Channel C power-on delay time = 40mS
-	-	-	-	**1**	**1**	-	-	Channel C power-on delay time = 75mS
-	-	-	-	-	-	**0**	**0**	Channel C power-off delay time = 1mS
-	-	-	-	-	-	**0**	**1**	Channel C power-off delay time = 20mS
-	-	-	-	-	-	**1**	**0**	Channel C power-off delay time = 40mS
-	-	-	-	-	-	**1**	**1**	Channel C power-off delay time = 75mS

CONFIGURATION REGISTERS (CONTINUED)

Register R13 – VGATE3 Configuration

Register R13								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Channel VGATE3 not used in sequencing
1	-	-	-	-	-	-	-	Channel VGATE3 used in sequencing
-	**0**	**0**	**0**	-	-	-	-	Channel VGATE3 assigned to sequence position 0
-	**0**	**0**	**1**					Channel VGATE3 assigned to sequence position 1
-	**0**	**1**	**0**	-	-	-	-	Channel VGATE3 assigned to sequence position 2
-	**0**	**1**	**1**	-	-	-	-	Channel VGATE3 assigned to sequence position 3
-	**1**	**0**	**0**	-	-	-	-	Channel VGATE3 assigned to sequence position 4
-	**1**	**0**	**1**	-	-	-	-	Channel VGATE3 assigned to sequence position 5
-	**1**	**1**	**0**	-	-	-	-	Unused
-	**1**	**1**	**1**	-	-	-	-	Null position (not used in sequencing)
-	-	-	-	**0**	**0**	-	-	Channel VGATE3 power-on delay time = 1mS
-	-	-	-	**0**	**1**	-	-	Channel VGATE3 power-on delay time = 20mS
-	-	-	-	**1**	**0**	-	-	Channel VGATE3 power-on delay time = 40mS
-	-	-	-	**1**	**1**	-	-	Channel VGATE3 power-on delay time = 75mS
-	-	-	-	-	-	**0**	**0**	Channel VGATE3 power-off delay time = 1mS
-	-	-	-	-	-	**0**	**1**	Channel VGATE3 power-off delay time = 20mS
-	-	-	-	-	-	**1**	**0**	Channel VGATE3 power-off delay time = 40mS
-	-	-	-	-	-	**1**	**1**	Channel VGATE3 power-off delay time = 75mS

Register R14 – VGATE5 Configuration

Register R14								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Channel VGATE5 not used in sequencing
1	-	-	-	-	-	-	-	Channel VGATE5 used in sequencing
-	**0**	**0**	**0**	-	-	-	-	Channel VGATE5 assigned to sequence position 0
-	**0**	**0**	**1**					Channel VGATE5 assigned to sequence position 1
-	**0**	**1**	**0**	-	-	-	-	Channel VGATE5 assigned to sequence position 2
-	**0**	**1**	**1**	-	-	-	-	Channel VGATE5 assigned to sequence position 3
-	**1**	**0**	**0**	-	-	-	-	Channel VGATE5 assigned to sequence position 4
-	**1**	**0**	**1**	-	-	-	-	Channel VGATE5 assigned to sequence position 5
-	**1**	**1**	**0**	-	-	-	-	Unused
-	**1**	**1**	**1**	-	-	-	-	Null position (not used in sequencing)
-	-	-	-	**0**	**0**	-	-	Channel VGATE5 power-on delay time = 1mS
-	-	-	-	**0**	**1**	-	-	Channel VGATE5 power-on delay time = 20mS
-	-	-	-	**1**	**0**	-	-	Channel VGATE5 power-on delay time = 40mS
-	-	-	-	**1**	**1**	-	-	Channel VGATE5 power-on delay time = 75mS
-	-	-	-	-	-	**0**	**0**	Channel VGATE5 power-off delay time = 1mS
-	-	-	-	-	-	**0**	**1**	Channel VGATE5 power-off delay time = 20mS
-	-	-	-	-	-	**1**	**0**	Channel VGATE5 power-off delay time = 40mS
-	-	-	-	-	-	**1**	**1**	Channel VGATE5 power-off delay time = 75mS

CONFIGURATION REGISTERS (CONTINUED)

Register R15 – DRVREN# Configuration.

Register R15								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Channel DRVREN# not used in sequencing
1	-	-	-	-	-	-	-	Channel DRVREN# used in sequencing
-	**0**	**0**	**0**	-	-	-	-	Channel DRVREN# assigned to sequence position 0
-	**0**	**0**	**1**					Channel DRVREN# assigned to sequence position 1
-	**0**	**1**	**0**	-	-	-	-	Channel DRVREN# assigned to sequence position 2
-	**0**	**1**	**1**	-	-	-	-	Channel DRVREN# assigned to sequence position 3
-	**1**	**0**	**0**	-	-	-	-	Channel DRVREN# assigned to sequence position 4
-	**1**	**0**	**1**	-	-	-	-	Channel DRVREN# assigned to sequence position 5
-	**1**	**1**	**0**	-	-	-	-	Unused
-	**1**	**1**	**1**	-	-	-	-	Null position (not used in sequencing)
-	-	-	-	**0**	**0**	-	-	Channel DRVREN# power-on delay time = 1mS
-	-	-	-	**0**	**1**	-	-	Channel DRVREN# power-on delay time = 20mS
-	-	-	-	**1**	**0**	-	-	Channel DRVREN# power-on delay time = 40mS
-	-	-	-	**1**	**1**	-	-	Channel DRVREN# power-on delay time = 75mS
-	-	-	-	-	-	**0**	**0**	Channel DRVREN# power-off delay time = 1mS
-	-	-	-	-	-	**0**	**1**	Channel DRVREN# power-off delay time = 20mS
-	-	-	-	-	-	**1**	**0**	Channel DRVREN# power-off delay time = 40mS
-	-	-	-	-	-	**1**	**1**	Channel DRVREN# power-off delay time = 75mS

Register R18, 1A, 1C, 1E – Write Only MARGIN_COMMAND

.

Register R18								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Unused
-	**0**	-	-	-	-	-	-	Unused
-	-	**0**	**0**	-	-	-	-	Channel A Command = Margin Nominal
-	-	**0**	**1**	-	-	-	-	Channel A Command = Margin Nominal
-	-	**1**	**0**	-	-	-	-	Channel A Command = Margin Low
-	-	**1**	**1**	-	-	-	-	Channel A Command = Margin High
-	-	-	-	**0**	**0**	-	-	Channel C Command = Margin Nominal
-	-	-	-	**0**	**1**	-	-	Channel C Command = Margin Nominal
-	-	-	-	**1**	**0**	-	-	Channel C Command = Margin Low
-	-	-	-	**1**	**1**	-	-	Channel C Command = Margin High
-	-	-	-	-	-	**0**	**0**	Channel B Command = Margin Nominal
-	-	-	-	-	-	**0**	**1**	Channel B Command = Margin Nominal
-	-	-	-	-	-	**1**	**0**	Channel B Command = Margin Low
-	-	-	-	-	-	**1**	**1**	Channel B Command = Margin High

CONFIGURATION REGISTERS (CONTINUED)

Register R30 – VREF Margin Channels A-C.

Register R30								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Unused
-	**0**	-	-	-	-	-	-	Unused
-	-	**0**	**0**	-	-	-	-	Channel C VREF Margin High Selection = 0.75V
-	-	**0**	**1**	-	-	-	-	Channel C VREF Margin High Selection = 1.00V
-	-	**1**	**0**	-	-	-	-	Channel C VREF Margin High Selection = 1.25V
-	-	**1**	**1**	-	-	-	-	Channel C VREF Margin High Selection = 2.00V
-	-	-	-	**0**	**0**	-	-	Channel B VREF Margin High Selection = 0.75V
-	-	-	-	**0**	**1**	-	-	Channel B VREF Margin High Selection = 1.00V
-	-	-	-	**1**	**0**	-	-	Channel B VREF Margin High Selection = 1.25V
-	-	-	-	**1**	**1**	-	-	Channel B VREF Margin High Selection = 2.00V
-	-	-	-	-	-	**0**	**0**	Channel A VREF Margin High Selection = 0.75V
-	-	-	-	-	-	**0**	**1**	Channel A VREF Margin High Selection = 1.00V
-	-	-	-	-	-	**1**	**0**	Channel A VREF Margin High Selection = 1.25V
-	-	-	-	-	-	**1**	**1**	Channel A VREF Margin High Selection = 2.00V

Register R31 – Channel A Margin High bits

Register R31								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel A Margin High Bits [7:0]

Register R32 – Channel C Margin High bits

Register R32								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel C Margin High Bits [7:0]

Register R33 – Channel B Margin High bits

Register R33								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel B Margin High Bits [7:0]

CONFIGURATION REGISTERS (CONTINUED)

Register R40 – VREF Margin Channels A-C.

Register R40								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**-**	**-**	**-**	**-**	**-**	**-**	**-**	Unused
-	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Unused
-	**-**	**0**	**0**	**-**	**-**	**-**	**-**	Channel C VREF Margin Low Selection = 0.75V
-	**-**	**0**	**1**	**-**	**-**	**-**	**-**	Channel C VREF Margin Low Selection = 1.00V
-	**-**	**1**	**0**	**-**	**-**	**-**	**-**	Channel C VREF Margin Low Selection = 1.25V
-	**-**	**1**	**1**	**-**	**-**	**-**	**-**	Channel C VREF Margin Low Selection = 2.00V
-	**-**	**-**	**-**	**0**	**0**	**-**	**-**	Channel B VREF Margin Low Selection = 0.75V
-	**-**	**-**	**-**	**0**	**1**	**-**	**-**	Channel B VREF Margin Low Selection = 1.00V
-	**-**	**-**	**-**	**1**	**0**	**-**	**-**	Channel B VREF Margin Low Selection = 1.25V
-	**-**	**-**	**-**	**1**	**1**	**-**	**-**	Channel B VREF Margin Low Selection = 2.00V
-	**-**	**-**	**-**	**-**	**-**	**0**	**0**	Channel A VREF Margin Low Selection = 0.75V
-	**-**	**-**	**-**	**-**	**-**	**0**	**1**	Channel A VREF Margin Low Selection = 1.00V
-	**-**	**-**	**-**	**-**	**-**	**1**	**0**	Channel A VREF Margin Low Selection = 1.25V
-	**-**	**-**	**-**	**-**	**-**	**1**	**1**	Channel A VREF Margin Low Selection = 2.00V

Register R41 – Channel A Margin Low bits

Register R41								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel A Margin Low Bits [7:0]

Register 42 – Channel C Margin Low bits

Register R42								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel C Margin Low Bits [7:0]

Register R43 – Channel B Margin Low bits

Register R43								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel B Margin Low Bits [7:0]

CONFIGURATION REGISTERS (CONTINUED)

Register R80, 88, 90, 98, A0, A8, B0, B8 – Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD and 12VIN Limit Triggers, Limit Bits [9:8].

Register R80, 88, 90, 98, A0, A8, B0, B8								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**-**	**-**	**-**	**-**	**-**	**-**	**-**	Limit does not trigger a RST
1	**-**	**-**	**-**	**-**	**-**	**-**	**-**	Limit triggers a RST
-	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Limit does not trigger an IRQ
-	**1**	**-**	**-**	**-**	**-**	**-**	**-**	Limit triggers an IRQ
-	**-**	**0**	**-**	**-**	**-**	**-**	**-**	Limit does not trigger a Power Down
-	**-**	**1**	**-**	**-**	**-**	**-**	**-**	Limit triggers a Power Down
-	**-**	**-**	**0**	**-**	**-**	**-**	**-**	Limit does not trigger a Forced Shutdown
-	**-**	**-**	**1**			**-**	**-**	Limit triggers a Forced Shutdown
-	**-**	**-**	**-**	**0**	**0**	**-**	**-**	Limit Consecutive Conversions for Fault = 1
-	**-**	**-**	**-**	**0**	**1**	**-**	**-**	Limit Consecutive Conversions for Fault = 2
-	**-**	**-**	**-**	**1**	**0**	**-**	**-**	Limit Consecutive Conversions for Fault = 4
-	**-**	**-**	**-**	**1**	**1**	**-**	**-**	Limit Consecutive Conversions for Fault = 6
-	**-**	**-**	**-**	**-**	**-**	**C9**	**C8**	Channel Low Limit 1 Bits [9:8]

Register R81, 89, 91, 99, A1, A9, B1, B9 – Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD and 12VIN Limit Settings [7:0].

Register R81, 89, 91, 99, A1, A9, B1, B9								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel Low Limit 1 Bits [7:0]

Register R82, 8A, 92, 9A, A2, AA, B2, BA – Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD and 12VIN Limit Settings [9:8].

Register R82, 8A, 92, 9A, A2, AA, B2, BA								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
-	**-**	**-**	**-**	**-**	**-**	**C9**	**C8**	Channel Low Limit 2 Bits [9:8]

Register R83, 8B, 93, 9B, A3, AB, B3, BB– Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD and 12VIN Limit Settings [7:0].

Register R83, 8B, 93, 9B, A3, AB, B3, BB								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Channel Low Limit 2 Bits [7:0]

Register R84, 8C, 94, 9C, A4, AC, B4, BC– Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD and 12VIN Limit Settings [9:8].

Register R84, 8C, 94, 9C, A4, AC, B4, BC								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
-	**-**	**-**	**-**	**-**	**-**	**C9**	**C8**	Channel High Limit 1 Bits [9:8]

CONFIGURATION REGISTERS (CONTINUED)

Register R85, 8D, 95, 9D, A5, AD, B5, BD – Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD and 12VIN Limit Settings [7:0].

Register R85, 8D, 95, 9D, A5, AD, B5, BD								
D7	D6	D5	D4	D3	D2	D1	D0	Action
C7	C6	C5	C4	C3	C2	C1	C0	Channel High Limit 1 Bits [7:0]

Register R86, 8E, 96, 9E, A6, AE, B6, BE – Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD and 12VIN Limit Settings [9:8].

Register R86, 8E, 96, 9E, A6, AE, B6, BE								
D7	D6	D5	D4	D3	D2	D1	D0	Action
-	-	-	-	-	-	C9	C8	Channel High Limit 2 Bits [9:8]

Register R87, 8F, 97, 9F, A7, AF, B7, BF – Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD and 12VIN Limit Settings [7:0].

Register R87, 8F, 97, 9F, A7, AF, B7, BF								
D7	D6	D5	D4	D3	D2	D1	D0	Action
C7	C6	C5	C4	C3	C2	C1	C0	Channel High Limit 2 Bits [7:0]

Register RC0 –VCC3 Low Limit 1 Triggers, Limit Bits [9:8].

Register RC0, C2, C4, C6								
D7	D6	D5	D4	D3	D2	D1	D0	Action
0	-	-	-	-	-	-	-	VCC3 Low Limit 1 does not trigger a RST
1	-	-	-	-	-	-	-	VCC3 Low Limit 1 triggers a RST
-	0	-	-	-	-	-	-	VCC3 Low Limit 1 does not trigger an IRQ
-	1	-	-	-	-	-	-	VCC3 Low Limit 1 triggers an IRQ
-	-	0	-	-	-	-	-	VCC3 Low Limit 1 does not trigger a Power Down.
-	-	1	-	-	-	-	-	VCC3 Low Limit 1 triggers a Power Down
-	-	-	0	-	-	-	-	VCC3 Low Limit 1 does not trigger a Fault
-	-	-	1			-	-	VCC3 Low Limit 1 triggers a Fault
-	-	-	-	0	0	-	-	VCC3 Low Limit 1 Consecutive Conversions for Fault = 1
-	-	-	-	0	1	-	-	VCC3 Low Limit 1 Consecutive Conversions for Fault = 2
-	-	-	-	1	0	-	-	VCC3 Low Limit 1 Consecutive Conversions for Fault = 4
-	-	-	-	1	1	-	-	VCC3 Low Limit 1 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	C9	C8	VCC3 Low Low Limit 1 Bits [9:8]

Register RC1– VCC3 Low Limit 1 Settings [7:0].

Register RC1								
D7	D6	D5	D4	D3	D2	D1	D0	Action
C7	C6	C5	C4	C3	C2	C1	C0	VCC3 Low limit 1 Bits[7:0]

CONFIGURATION REGISTERS (CONTINUED)

Register RC2 –VCC3 Low Limit 2 Triggers, Limit Bits [9:8].

Register C2								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	VCC3 Low Limit 2 does not trigger a RST
1	-	-	-	-	-	-	-	VCC3 Low Limit 2 triggers a RST
-	**0**	-	-	-	-	-	-	VCC3 Low Limit 2 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	VCC3 Low Limit 2 triggers an IRQ
-	-	**0**	-	-	-	-	-	VCC3 Low Limit 2 does not trigger a Power Down.
-	-	**1**	-	-	-	-	-	VCC3 Low Limit 2 triggers a Power Down
-	-	-	**0**	-	-	-	-	VCC3 Low Limit 2 does not trigger a Fault
-	-	-	**1**			-	-	VCC3 Low Limit 2 triggers a Fault
-	-	-	-	**0**	**0**	-	-	VCC3 Low Limit 2 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	VCC3 Low Limit 2 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	VCC3 Low Limit 2 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	VCC3 Low Limit 2 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	VCC3 Low Limit 2 Bits [9:8]

Register RC3 – VCC3 Low Limit 2 Settings [7:0].

Register RC3								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	VCC3 Low limit 2 Bits[7:0]

CONFIGURATION REGISTERS (CONTINUED)

Register RC4 –VCC3 High Limit 1 Triggers, Limit Bits [9:8].

Register C4								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	VCC3 High Limit 1 does not trigger a RST
1	-	-	-	-	-	-	-	VCC3 High Limit 1 triggers a RST
-	**0**	-	-	-	-	-	-	VCC3 High Limit 1 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	VCC3 High Limit 1 triggers an IRQ
-	-	**0**	-	-	-	-	-	VCC3 High Limit 1 does not trigger a Power Down.
-	-	**1**	-	-	-	-	-	VCC3 High Limit 1 triggers a Power Down
-	-	-	**0**	-	-	-	-	VCC3 High Limit 1 does not trigger a Fault
-	-	-	**1**			-	-	VCC3 High Limit 1 triggers a Fault
-	-	-	-	**0**	**0**	-	-	VCC3 High Limit 1 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	VCC3 High Limit 1 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	VCC3 High Limit 1 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	VCC3 High Limit 1 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	VCC3 High Limit 1 Bits [9:8]

Register RC5 – VCC3 High Limit 1 Settings [7:0].

Register RC5								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	VCC3 High limit 1 Bits[7:0]

CONFIGURATION REGISTERS (CONTINUED)

Register RC6 –VCC3 High Limit 2 Triggers, Limit Bits [9:8].

Register C6								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	VCC3 High Limit 2 does not trigger a RST
1	-	-	-	-	-	-	-	VCC3 High Limit 2 triggers a RST
-	**0**	-	-	-	-	-	-	VCC3 High Limit 2 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	VCC3 High Limit 2 triggers an IRQ
-	-	**0**	-	-	-	-	-	VCC3 High Limit 2 does not trigger a Power Down.
-	-	**1**	-	-	-	-	-	VCC3 High Limit 2 triggers a Power Down
-	-	-	**0**	-	-	-	-	VCC3 High Limit 2 does not trigger a Fault
-	-	-	**1**			-	-	VCC3 High Limit 2 triggers a Fault
-	-	-	-	**0**	**0**	-	-	VCC3 High Limit 2 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	VCC3 High Limit 2 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	VCC3 High Limit 2 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	VCC3 High Limit 2 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	VCC3 High Limit 2 Bits [9:8]

Register RC7 – VCC3 High Limit 2 Settings [7:0].

Register RC7								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	VCC3 High limit 2 Bits[7:0]

Register RC8– VTEMP Low Limit 1 Triggers, Limit Bits [9:8].

Register RC8								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	VTEMP Low Limit 1 does not trigger a RST
1	-	-	-	-	-	-	-	VTEMP Low Limit 1 triggers a RST
-	**0**	-	-	-	-	-	-	VTEMP Low Limit 1 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	VTEMP Low Limit 1 triggers an IRQ
-	-	**0**	-	-	-	-	-	VTEMP Low Limit 1 does not trigger a Pwr. Dn.
-	-	**1**	-	-	-	-	-	VTEMP Low Limit 1 triggers a Power Down
-	-	-	**0**	-	-	-	-	VTEMP Low Limit 1 does not trigger a Fault
-	-	-	**1**			-	-	VTEMP Low Limit 1 triggers a Fault
-	-	-	-	**0**	**0**	-	-	VTEMP Low Limit 1 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	VTEMP Low Limit 1 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	VTEMP Low Limit 1 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	VTEMP Low Limit 1 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	VTEMP Low Limit 1 Bits [9:8]

CONFIGURATION REGISTERS (CONTINUED)

Register RC9– VTEMP Low Limit 1 Settings [7:0].

Register RC9								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	VTEMP Low Limit 1 Bits[7:0]

Register RCA– VTEMP Low Limit 2 Triggers, Limit Bits [9:8].

Register RCA								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	VTEMP Low Limit 2 does not trigger a RST
1	-	-	-	-	-	-	-	VTEMP Low Limit 2 triggers a RST
-	**0**	-	-	-	-	-	-	VTEMP Low Limit 2 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	VTEMP Low Limit 2 triggers an IRQ
-	-	**0**	-	-	-	-	-	VTEMP Low Limit 2 does not trigger a Pwr. Dn.
-	-	**1**	-	-	-	-	-	VTEMP Low Limit 2 triggers a Power Down
-	-	-	**0**	-	-	-	-	VTEMP Low Limit 2 does not trigger a Fault
-	-	-	**1**			-	-	VTEMP Low Limit 2 triggers a Fault
-	-	-	-	**0**	**0**	-	-	VTEMP Low Limit 2 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	VTEMP Low Limit 2 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	VTEMP Low Limit 2 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	VTEMP Low Limit 2 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	VTEMP Low Limit 2 Bits [9:8]

Register RCB – VTEMP Low Limit 2 Settings [7:0].

Register RCB								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	VTEMP Low Limit 2 Bits[7:0]

CONFIGURATION REGISTERS (CONTINUED)

Register RCC– VTEMP High Limit 1 Triggers, Limit Bits [9:8].

Register RCC								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	VTEMP High Limit 1 does not trigger a RST
1	-	-	-	-	-	-	-	VTEMP High Limit 1 triggers a RST
-	**0**	-	-	-	-	-	-	VTEMP High Limit 1 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	VTEMP High Limit 1 triggers an IRQ
-	-	**0**	-	-	-	-	-	VTEMP High Limit 1 does not trigger a Power Down
-	-	**1**	-	-	-	-	-	VTEMP High Limit 1 triggers a Power Down
-	-	-	**0**	-	-	-	-	VTEMP High Limit 1 does not trigger a Fault
-	-	-	**1**			-	-	VTEMP High Limit 1 triggers a Fault
-	-	-	-	**0**	**0**	-	-	VTEMP High Limit 1 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	VTEMP High Limit 1 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	VTEMP High Limit 1 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	VTEMP High Limit 1 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	VTEMP High Limit 1 Bits [9:8]

Register RCD – VTEMP High Limit 1 Settings [7:0].

Register RCD								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	VTEMP High Limit 1 Bits[7:0]

Register RCE– VTEMP High Limit 2 Triggers, Limit Bits [9:8].

Register RCE								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	VTEMP High Limit 2 does not trigger a RST
1	-	-	-	-	-	-	-	VTEMP High Limit 2 triggers a RST
-	**0**	-	-	-	-	-	-	VTEMP High Limit 2 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	VTEMP High Limit 2 triggers an IRQ
-	-	**0**	-	-	-	-	-	VTEMP High Limit 2 does not trigger a Pwr. Dn.
-	-	**1**	-	-	-	-	-	VTEMP High Limit 2 triggers a Power Down
-	-	-	**0**	-	-	-	-	VTEMP High Limit 2 does not trigger a Fault
-	-	-	**1**			-	-	VTEMP High Limit 2 triggers a Fault
-	-	-	-	**0**	**0**	-	-	VTEMP High Limit 2 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	VTEMP High Limit 2 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	VTEMP High Limit 2 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	VTEMP High Limit 2 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	VTEMP High Limit 2 Bits [9:8]

CONFIGURATION REGISTERS (CONTINUED)

Register RCF – VTEMP High Limit 2 Settings [7:0].

Register RCF								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	VTEMP High Limit 2 Bits[7:0]

Register RD0 – EXT_TEMP Low Limit 1 Triggers, Limit Bits [9:8].

Register RD0								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	EXT_TEMP Low Limit 1 does not trigger a RST
1	-	-	-	-	-	-	-	EXT_TEMP Low Limit 1 triggers a RST
-	**0**	-	-	-	-	-	-	EXT_TEMP Low Limit 1 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	EXT_TEMP Low Limit 1 triggers an IRQ
-	-	**0**	-	-	-	-	-	EXT_TEMP Low Limit 1 does not trigger a Power Down
-	-	**1**	-	-	-	-	-	EXT_TEMP Low Limit 1 triggers a Power Down
-	-	-	**0**	-	-	-	-	EXT_TEMP Low Limit 1 does not trigger a Fault
-	-	-	**1**			-	-	EXT_TEMP Low Limit 1 triggers a Fault
-	-	-	-	**0**	**0**	-	-	EXT_TEMP Low Limit 1 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	EXT_TEMP Low Limit 1 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	EXT_TEMP Low Limit 1 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	EXT_TEMP Low Limit 1 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	EXT_TEMP Low Limit 1 Bits [9:8]

Register RD1– EXT_TEMP Low Limit 1 Settings [9:8].

Register RD1								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	EXT_TEMP Low Limit 1 Bits[7:0]

CONFIGURATION REGISTERS (CONTINUED)

Register RD2 – EXT_TEMP Low Limit 2 Triggers, Limit Bits [9:8].

Register RD2								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	EXT_TEMP Low Limit 2 does not trigger a RST
1	-	-	-	-	-	-	-	EXT_TEMP Low Limit 2 triggers a RST
-	**0**	-	-	-	-	-	-	EXT_TEMP Low Limit 2 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	EXT_TEMP Low Limit 2 triggers an IRQ
-	-	**0**	-	-	-	-	-	EXT_TEMP Low Limit 2 does not trigger a Pwr Dwn
-	-	**1**	-	-	-	-	-	EXT_TEMP Low Limit 2 triggers a Power Down
-	-	-	**0**	-	-	-	-	EXT_TEMP Low Limit 2 does not trigger a Fault
-	-	-	**1**			-	-	EXT_TEMP Low Limit 2 triggers a Fault
-	-	-	-	**0**	**0**	-	-	EXT_TEMP Low Limit 2 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	EXT_TEMP Low Limit 2 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	EXT_TEMP Low Limit 2 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	EXT_TEMP Low Limit 2 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	EXT_TEMP Low Limit 2 Bits [9:8]

Register RD3– EXT_TEMP Low Limit 2 Settings [7:0].

Register RD3								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	EXT_TEMP Low Limit 2 Bits [7:0]

Register RD4 – EXT_TEMP High Limit 1 Triggers, Limit Bits [9:8].

Register RD4								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	EXT_TEMP High Limit 1 does not trigger a RST
1	-	-	-	-	-	-	-	EXT_TEMP High Limit 1 triggers a RST
-	**0**	-	-	-	-	-	-	EXT_TEMP High Limit 1 does not trigger an IRQ
-	**1**	-	-	-	-	-	-	EXT_TEMP High Limit 1 triggers an IRQ
-	-	**0**	-	-	-	-	-	EXT_TEMP High Limit 1 does not trigger a Pwr. Dn.
-	-	**1**	-	-	-	-	-	EXT_TEMP High Limit 1 triggers a Power Down
-	-	-	**0**	-	-	-	-	EXT_TEMP High Limit 1 does not trigger a Fault
-	-	-	**1**			-	-	EXT_TEMP High Limit 1 triggers a Fault
-	-	-	-	**0**	**0**	-	-	EXT_TEMP High Limit 1 Consecutive Conversions for Fault = 1
-	-	-	-	**0**	**1**	-	-	EXT_TEMP High Limit 1 Consecutive Conversions for Fault = 2
-	-	-	-	**1**	**0**	-	-	EXT_TEMP High Limit 1 Consecutive Conversions for Fault = 4
-	-	-	-	**1**	**1**	-	-	EXT_TEMP High Limit 1 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	**C9**	**C8**	EXT_TEMP High Limit 1 Bits [9:8]

CONFIGURATION REGISTERS (CONTINUED)

Register RD5 – EXT_TEMP High Limit 1 Settings [9:8].

Register RD5								
D7	D6	D5	D4	D3	D2	D1	D0	Action
C7	C6	C5	C4	C3	C2	C1	C0	EXT_TEMP High Limit 1 Bits [7:0]

Register RD6 – EXT_TEMP High Limit 2 Triggers, Limit Bits [9:8].

Register RD6								
D7	D6	D5	D4	D3	D2	D1	D0	Action
0	-	-	-	-	-	-	-	EXT_TEMP High Limit 2 does not trigger a RST
1	-	-	-	-	-	-	-	EXT_TEMP High Limit 2 triggers a RST
-	0	-	-	-	-	-	-	EXT_TEMP High Limit 2 does not trigger an IRQ
-	1	-	-	-	-	-	-	EXT_TEMP High Limit 2 triggers an IRQ
-	-	0	-	-	-	-	-	EXT_TEMP High Limit 2 does not trigger a Power Down
-	-	1	-	-	-	-	-	EXT_TEMP High Limit 2 triggers a Power Down
-	-	-	0	-	-	-	-	EXT_TEMP High Limit 2 does not trigger a Fault
-	-	-	1			-	-	EXT_TEMP High Limit 2 triggers a Fault
-	-	-	-	0	0	-	-	EXT_TEMP High Limit 2 Consecutive Conversions for Fault = 1
-	-	-	-	0	1	-	-	EXT_TEMP High Limit 2 Consecutive Conversions for Fault = 2
-	-	-	-	1	0	-	-	EXT_TEMP High Limit 2 Consecutive Conversions for Fault = 4
-	-	-	-	1	1	-	-	EXT_TEMP High Limit 2 Consecutive Conversions for Fault = 6
-	-	-	-	-	-	C9	C8	EXT_TEMP High Limit 2 Bits [9:8]

Register RD7 – EXT_TEMP High Limit 1 Settings [7:0].

Register RD7								
D7	D6	D5	D4	D3	D2	D1	D0	Action
C7	C6	C5	C4	C3	C2	C1	C0	EXT_TEMP High Limit 2 Bits [7:0]

Register RE0, E2, E4, E6, E8, EA – Channel A, B, C, CARD12, CARD3, CARD5 Off Limits [9:8].

Register RE0, E2, E4, E6, E8, EA								
D7	D6	D5	D4	D3	D2	D1	D0	Action
	-	-	-	-	-	C9	C8	Channel/CardX Off Limits [9:8]

Register RE1, E3, E5, E7, E9, EB – Channel A, B, C, CARD12, CARD3, CARD5 Off Limits [7:0].

Register RE1 E3, E5, E7, E9, EB								
D7	D6	D5	D4	D3	D2	D1	D0	Action
C7	C6	C5	C4	C3	C2	C1	C0	Channel/CardX Off Limits [7:0]

CONFIGURATION REGISTERS (CONTINUED)

Registers accessed using slave address 1001 A2 A1 A0.

Register R00, 08, 10, 18, 20, 28, 30, 38, 40, 48, 50 - Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD, 12VIN, VCC3, VTEMP, EXT_TEMP ADC Register Readout [9:8].

Register R00, 08, 10, 18, 20, 28, 30, 38, 40, 48, 50								
D7	D6	D5	D4	D3	D2	D1	D0	Action
Ch	Ch	Ch	Ch	Ch	0	-	-	Channel being read
-	-	-	-	-	0		-	Unused
					0	C9	C8	Upper 2 bits of ADC readout

Register R01, 09, 11, 19, 21, 29, 30, 39, 41, 49, 51- Channel A, B, C, CARD12V, CARD3V, CARD5V, VDD, 12VIN, VCC3, VTEMP, EXT_TEMP ADC Register Readout [7:0].

Register R01, 09, 11, 19, 21, 29, 30, 39, 41, 49, 51								
D7	D6	D5	D4	D3	D2	D1	D0	Action
C7	C6	C5	C4	C3	C2	C1	C0	Channel being read

Register R80 Communication Interface Command and Control .

Register R80								
D7	D6	D5	D4	D3	D2	D1	D0	Action
0	0	0	-	-	-	-	0	Does Nothing
1	0	0	-	-	-	-	0	Power-On command
0	1	0	-	-	-	-	0	Power-Off command
0	0	1	-	-	-	-	0	Forced Shutdown command
-	-	-	0	-	-	-	0	Command does not Clear IRQ
-	-	-	1	-	-	-	0	Command Clears IRQ
-	-	-	-	0	-	-	0	Sequenced Channels not out of Fault (Read Only)
-	-	-	-	1	-	-	0	Sequenced Channels out of Fault (Read Only)
-	-	-	-	-	0	-	0	Sequenced Channels not Below Off Limit (Read Only)
-	-	-	-	-	1	-	0	Sequenced Channels Below Off Limit (Read Only)
-	-	-	-	-	-	0	0	IRQ not Present (Read-Only)
-	-	-	-	-	-	1	0	IRQ Present (Read-Only)
-	-	-	-	-	-	-	0	Unused

CONFIGURATION REGISTERS (CONTINUED)

Register R81 Status Registers (Fault [10:8]).

Register R81								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	Sequence not Aborted
1	-	-	-	-	-	-	-	Sequence Aborted
-	**0**	**0**	**0**	-	-	-	-	Sequence Position Aborted = 0
-	**0**	**0**	**1**	-	-	-	-	Sequence Position Aborted = 1
-	**0**	**1**	**0**	-	-	-	-	Sequence Position Aborted = 2
	0	**1**	**1**	-	-	-	-	Sequence Position Aborted = 3
	1	**0**	**0**	-	-	-	-	Sequence Position Aborted = 4
	1	**0**	**1**	-	-	-	-	Sequence Position Aborted = 5
-	-	-	-	**0**	-	-	-	Unused
-	-	-	-	**0**	**0**	**0**	**0**	[EXT_TEMP, Vtemp, VCC3] = No Fault
-	-	-	-	**0**	**1**	**1**	**1**	[EXT_TEMP, Vtemp, VCC3] = Fault

Register R82 Status Registers (Fault [7:0]).

Register R82								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	[12VIN, VDD, CARD5V, CARD3V, CARD12V, ChC, ChB, ChA] = No Fault
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	[12VIN, VDD, CARD5V, CARD3V, CARD12V, ChC, ChB, ChA] = Fault

Register R84 FPGA I/O.

Register R84								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	-	-	-	-	-	-	-	FPGA_NSTS input
1	-	-	-	-	-	-	-	FPGA_NSTS input
-	**0**	-	-	-	-	-	-	FPGA_CFGDONE input
-	**1**	-	-	-	-	-	-	FPGA_CFGDONE input
-		**0**	**0**	**0**	-	-	-	Unused
-	-	-	-	-	**0**	-	-	FPGA_DCLK Data output
-	-	-	-	-	**1**	-	-	FPGA_DCLK Data output
-	-	-	-	-		**0**	-	FPGA_D0 Data output
-	-	-	-	-		**1**	-	FPGA_D0 Data output
-	-	-	-	-	-		**0**	FPGA_NCFG Data output
-	-	-	-	-	-		**1**	FPGA_NCFG Data output

CONFIGURATION REGISTERS (CONTINUED)

Register R85 Read-Only Margin Command.

Register R85								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**-**	**-**	**-**	**-**	**-**	**-**	**-**	DC Control not Ready
1	**-**	**-**	**-**	**-**	**-**	**-**	**-**	DC Control Ready
-	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Unused
-	**-**	**0**	**0**	**-**	**-**	**-**	**-**	Channel A Margin Nominal
-		**0**	**1**	**-**	**-**	**-**	**-**	Channel A Margin Nominal
-	**-**	**1**	**0**	**-**	**-**	**-**	**-**	Channel A Margin Low
-	**-**	**1**	**1**	**-**	**-**	**-**	**-**	Channel A Margin High
-	**-**	**-**	**-**	**0**	**0**	**-**	**-**	Channel C Margin Nominal
-	**-**	**-**	**-**	**0**	**1**	**-**	**-**	Channel C Margin Nominal
-	**-**	**-**	**-**	**1**	**0**	**-**	**-**	Channel C Margin Low
-	**-**	**-**	**-**	**1**	**1**	**-**	**-**	Channel C Margin High
-	**-**	**-**	**-**	**-**	**-**	**0**	**0**	Channel B Margin Nominal
-	**-**	**-**	**-**	**-**	**-**	**0**	**1**	Channel B Margin Nominal
-	**-**	**-**	**-**	**-**	**-**	**1**	**0**	Channel B Margin Low
-	**-**	**-**	**-**	**-**	**-**	**1**	**1**	Channel B Margin High

Register R87 Write Protect.

Register R87								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
-	**-**	**-**	**-**	**-**	**-**	**-**	**-**	EEPROM Write Protected
0	**1**	**0**	**1**	**-**	**-**	**-**	**-**	EEPROM Not Write Protected
-	**-**	**-**	**-**	**-**	**-**	**-**	**-**	Config Write Protected
-	**-**	**-**	**-**	**0**	**1**	**0**	**1**	Config Not Write Protected

Register R88 Status Tracking Code.

Register R88								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	U01

CONFIGURATION REGISTERS (CONTINUED)

Register R8B Pin Polarity.

Register R8B								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Unused [7:6]
-	**-**	**0**	**-**	**-**	**-**	**-**	**-**	Healthy Active Low
-	**-**	**1**	**-**	**-**	**-**	**-**	**-**	Healthy Active High
-	**-**	**-**	**0**	**-**	**-**	**-**	**-**	Fault Active Low
-		**-**	**1**		**-**	**-**	**-**	Fault Active High
-	**-**	**-**	**-**	**0**	**-**	**-**	**-**	Reset Active Low
-	**-**	**-**	**-**	**1**	**-**	**-**	**-**	Reset Active High
-	**-**	**-**	**-**	**-**	**0**	**-**	**-**	HST_RST Active Low
-	**-**	**-**	**-**	**-**	**1**	**-**	**-**	HST_RST Active High
-	**-**	**-**	**-**	**-**	**-**	**0**	**-**	HST_PWR Active Low
-	**-**	**-**	**-**	**-**	**-**	**1**	**-**	HST_PWR Active High
-	**-**	**-**	**-**	**-**	**-**	**-**	**0**	FS Active Low
-	**-**	**-**	**-**	**-**	**-**	**-**	**1**	FS Active High

Register R8D Status Tracking Code.

Register R8D								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**-**	**-**	**-**	**-**	**-**	**-**	Unused [7:6]
-	**-**	**0**	**-**	**-**	**-**	**-**	**-**	VGATE High Voltage Level = 10.5V
-	**-**	**1**	**-**	**-**	**-**	**-**	**-**	VGATE High Voltage Level = 14V
-	**-**	**-**	**0**	**-**	**-**	**-**	**-**	VGATE5 PUP polarity active low
-	**-**	**-**	**1**	**-**	**-**	**-**	**-**	VGATE5 PUP polarity active high
-	**-**	**-**	**-**	**0**	**-**	**-**	**-**	VGATE3 PUP polarity active low
-	**-**	**-**	**-**	**1**	**-**	**-**	**-**	VGATE3 PUP polarity active high
-	**-**	**-**	**-**	**-**	**0**	**-**	**-**	Channel C PUP polarity active low
-	**-**			**-**	**1**	**-**	**-**	Channel C PUP polarity active high
-	**-**	**-**	**-**	**-**	**-**	**0**	**-**	Channel B PUP polarity active low
-	**-**	**-**	**-**	**-**	**-**	**1**	**-**	Channel B PUP polarity active high
-	**-**	**-**	**-**	**-**	**-**	**-**	**0**	Channel A PUP polarity active low
-	**-**	**-**	**-**	**-**	**-**	**-**	**1**	Channel A PUP polarity active high

DEFAULT CONFIGURATION REGISTER SETTINGS – SMH4046FC-232

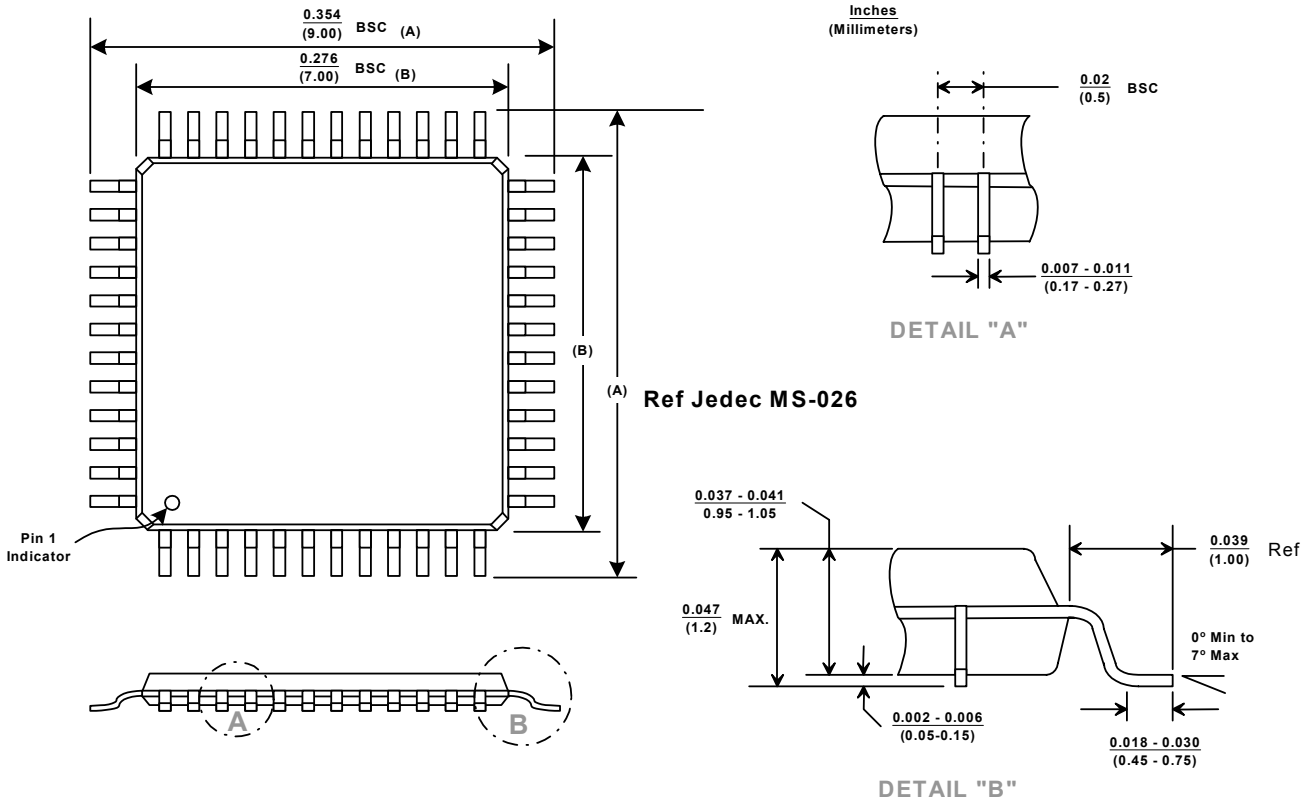
Register	Contents	Register	Contents	Register	Contents	Register	Contents
R00	0B	R8E	02	RB5	FF	RE4	00
R01	9B	R8F	49	RB6	03	RE5	3D
R02	80	R90	08	RB7	FF	RE6	00
R03	A0	R91	67	RB8	0D	RE7	3D
R04	04	R92	00	RB9	9A	RE8	00
R05	60	R93	67	RBA	0D	RE9	3D
R06	0F	R94	09	RBB	56	REA	00
R0C	4F	R95	D7	RBC	0F	REB	3D
R0D	3F	R96	01	RBD	FF		
R0E	C7	R97	EB	RBE	0F		
R0F	00	R98	02	RBF	FF		
R10	8F	R99	23	RC0	0A		
R11	9F	R9A	02	RC1	01		
R12	AF	R9B	24	RC2	09		
R13	BF	R9C	0B	RC3	9A		
R14	CF	R9D	FF	RC4	0B		
R15	DF	R9E	03	RC5	35		
R30	0B	R9F	FF	RC6	0B		
R31	92	RA0	01	RC7	FF		
R32	6A	RA1	0B	RC8	0C		
R33	91	RA2	00	RC9	00		
R40	0B	RA3	F6	RCA	0C		
R41	AB	RA4	0B	RCB	00		
R42	94	RA5	35	RCC	0D		
R43	B2	RA6	03	RCD	FF		
R80	01	RA7	FF	RCE	0D		
R81	9A	RA8	00	RCF	FF		
R82	01	RA9	CE	RD0	0C		
R83	9A	RAA	00	RD1	00		
R84 Note 1	0B	RAB	8F	RD2	0C		
R85	35	RAC	0B	RD3	00		
R86	03	RAD	4E	RD4	0F		
R87	35	RAE	03	RD5	D8		
R88	01	RAF	9B	RD6	0F		
R89	34	RB0	0A	RD7	D8		
R8A	01	RB1	67	RE0	00	Slave Address 1001	
R8B Note 1	34	RB2	0A	RE1	3D	R84 Note 1	07
R8C	0A	RB3	52	RE2	00	R8B Note 1	00
R8D Note 1	34	RB4	03	RE3	3D	R8D Note 1	00

The default device ordering number is SMH4046FC-232. It is programmed with the register contents as shown above and tested over the commercial temperature range. New device suffix numbers are assigned to non-default requirements.

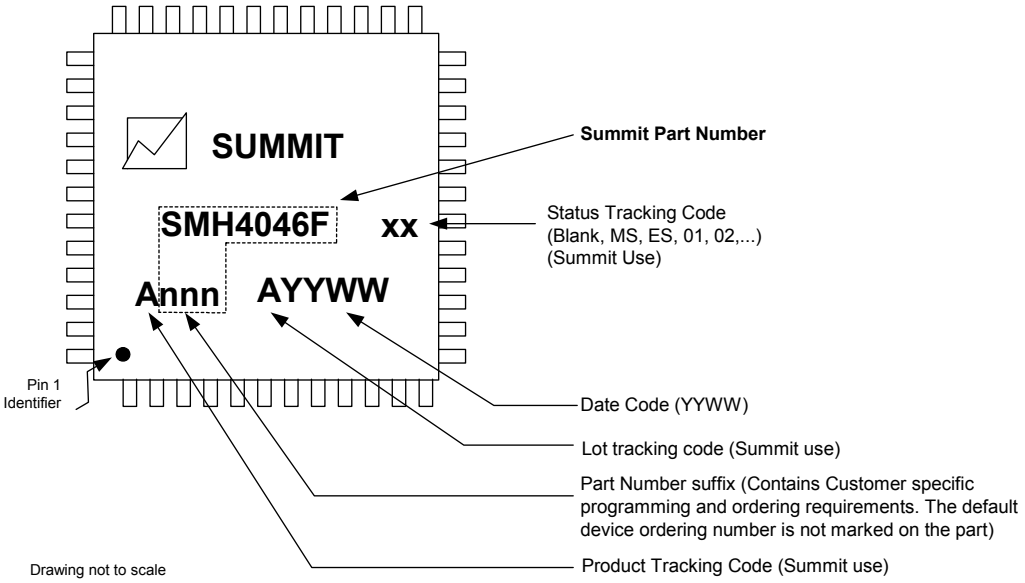
Note 1 – Two sets of configuration registers R84, R8B and R8D are at different slave addresses, address space 1001 and programmable slave address space 101X. The contents shown on the left side of the table are for address 101X. On the right side at slave address 1001, the contents are 07, 00 and 00.

PACKAGE

48 PIN TQFP PACKAGE



PART MARKING



ORDERING INFORMATION

SMH4046 F C nnn

Summit Part Number

Package
F=48 Lead TQFP

Temp Range
C=Commercial
Blank=Industrial

Part Number Suffix (see page 47)
Customer specific requirements are contained in the suffix such as Hex code, Hex code revision, etc.

NOTICE

NOTE 1 - This is a ***Preliminary Information*** data sheet that describes a Summit product currently in pre-production with limited characterization.

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http://www.summitmicro.com/prod_select/summary/SMH4046/SMH4046.htm

Device Errata sheets can be accessed by "right" or "left" mouse clicking on the link: http://www.summitmicro.com/errata/SMH4046

 PROGRAMMABLE ANALOG FOR A DIGITAL WORLD™