Programmable -48V Hot-Swap Controller with Forced Shut Down

FEATURES & APPLICATIONS

- **Soft Start Power Supply**
- **Live Insertion into a -48V backplane**
- **Programmable Control of a DC/DC Converter**
  - **I²C Power On/Off Control**
- **Highly Programmable Circuit Breaker**
  - **Active In-rush Current Limiting**
  - **Over-current Filter Circuit Breaker Immunity to Voltage Steps and Current Spikes**
- **Programmable Forced Shutdown Timer**
- **Internal Shunt Regulator Allows a Wide Supply Range**
- **14-pin SOIC and 16-pin SSOP packages**

APPLICATIONS

- **-48V Power Distribution**
  - **Telecom Line Cards**
  - **Central Office Switching**
  - **High Availability Servers**
  - **Hot Board Insertion**

INTRODUCTION

The SMH4802 is designed to control in-rush current during hot swapping of plug-in cards operating in a distributed power environment. The device drives an external power MOSFET switch that connects the supply to the load and protects against over-current conditions that might disrupt the host supply. It also provides under-voltage and over-voltage monitoring of the host power supply. When the source and drain voltages of the external MOSFETs are within specification it will provide a Power Good logic output that can be used to enable a DC/DC converter. Additional features of the device include: temperature sense or master enable input, a 5V reference output for expanding monitor functions, and duty-cycle or latched over-current protection modes. An internal Shunt regulator allows a wide supply range. The SMH4802 -48V Hot-Swap Controller also features a simple software I²C Power On/Off Interface for remote power control applications.

Programming of configuration, control and calibration values by the user can be simplified with the SMX3200 interface adapter and a windows based GUI supplied by Summit.

SIMPLIFIED APPLICATION DRAWING

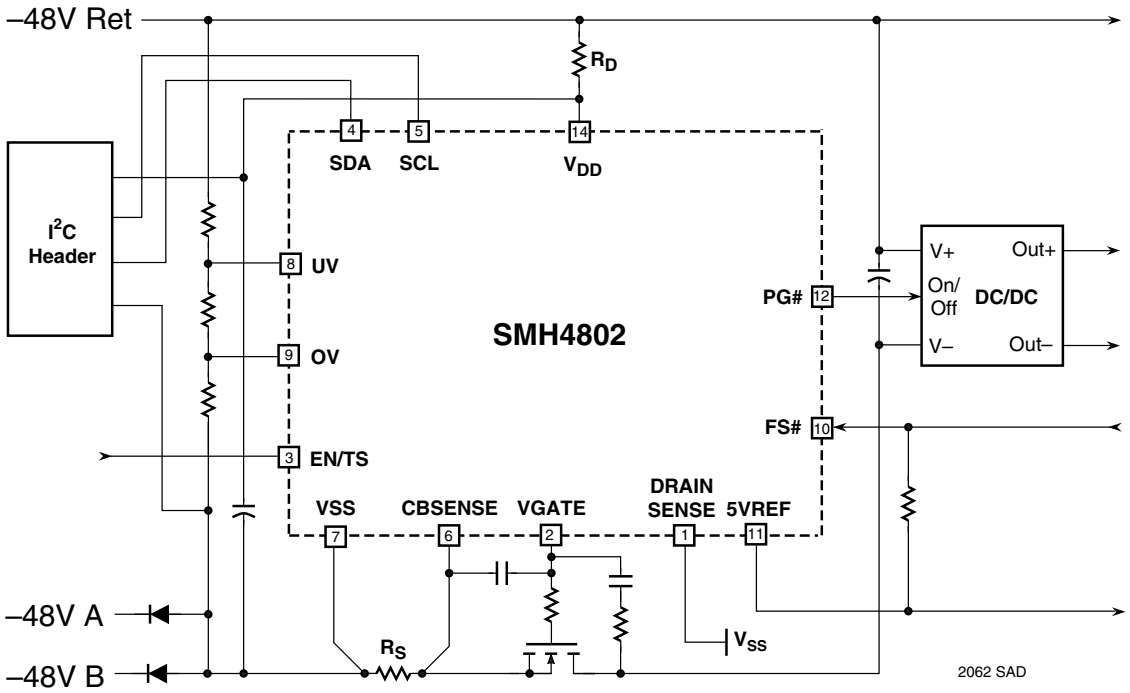


Figure 1. The drawing illustrates the SMH4802 in a typical line-card application. It should be noted this is just an example, and the specific component values are purposely not shown. Pin numbers reflect SOIC package.

GENERAL DESCRIPTION

The SMH4802 is an integrated power controller for hot swappable add-in cards. The device operates from a wide supply range and generates the signals necessary to drive an isolated output DC/DC converter. As a typical add-in board is inserted into the powered backplane, physical connections must first be made with the chassis to discharge any electrostatic voltage potentials. The board then contacts the long pins on the backplane that provide power and ground. As soon as power is applied, the device starts up, but does not immediately apply power to the output load. Under-voltage and over-voltage circuits inside the controller verify the input voltage is within the user-specified range.

Once these requirements are met, the hot-swap controller enables VGATE to turn on the external power MOSFET.

The VGATE output is current limited to $I_{VGATE,}$ allowing the slew rate to be easily modified using external passive components. During the controlled turn-on period the V_{DS} of the MOSFET is monitored by the DRAIN SENSE input. When DRAIN SENSE drops below 2.5V, and VGATE is greater than $V_{DD} - V_{GT}$, the PG# output can begin turning on the DC/DC converter.

Steady state operation is maintained as long as all conditions are normal. Any of the following events may cause the device to disable the DC/DC controller by shutting down the power MOSFET: an under-voltage or over-voltage condition on the host power supply; an over-current event detected on the CBSENSE input; a failure of the power MOSFET sensed via the DRAIN SENSE pin; the master enable (EN/TS) falling below 2.5V; or the FS# input being driven low by events on the secondary side of the DC/DC controller. If one of these events occurs the SMH4802 can be configured so VGATE shuts off and either latches into an off state or recycles power after a cooling down period, t_{CYC}.

FUNCTIONAL BLOCK DIAGRAM

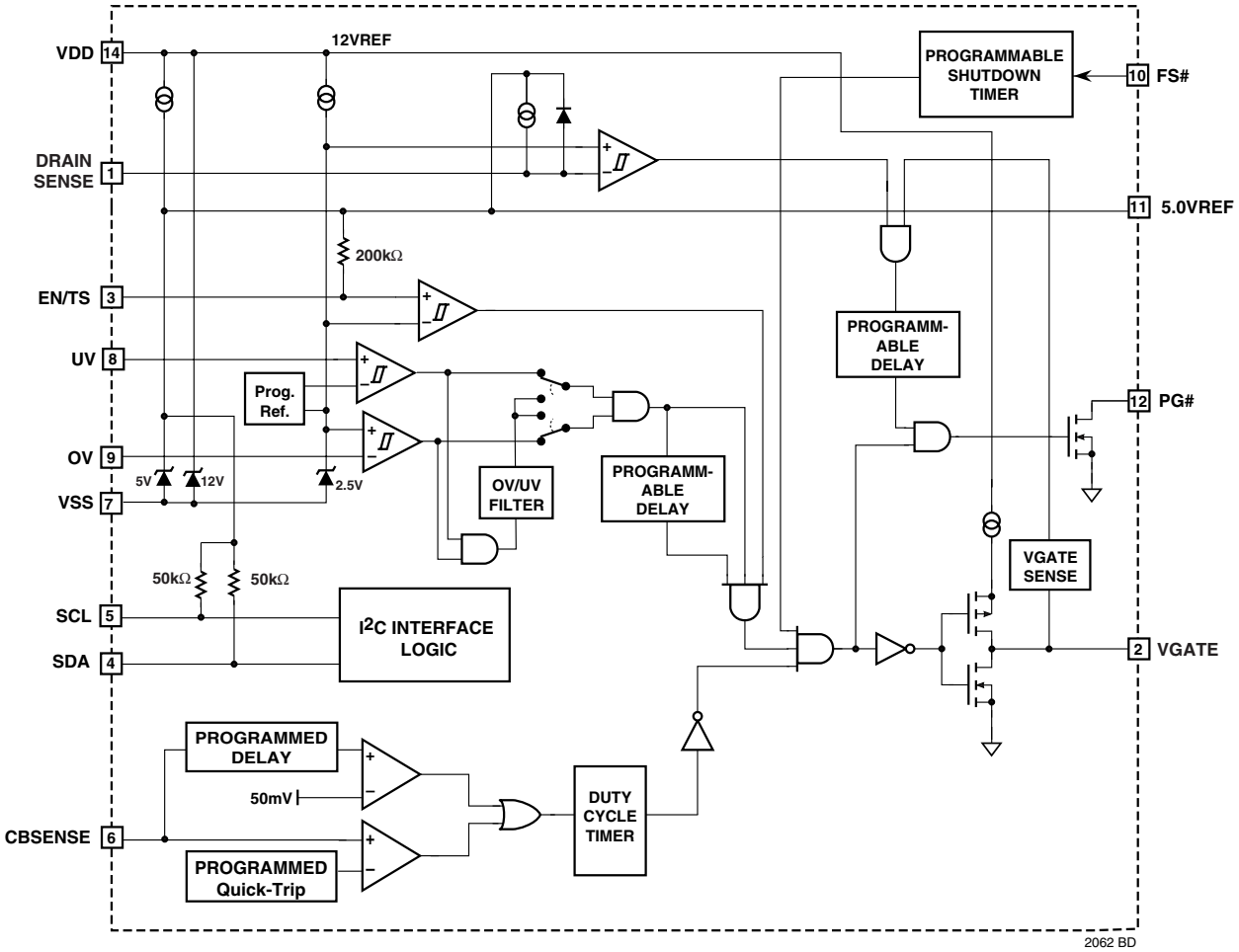
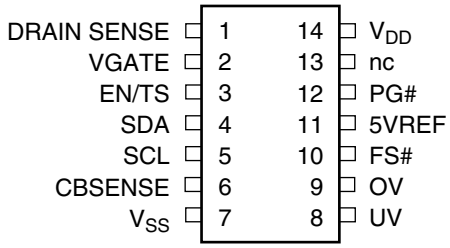


Figure 2. Functional Block diagram. Pin numbers reflect SOIC package.

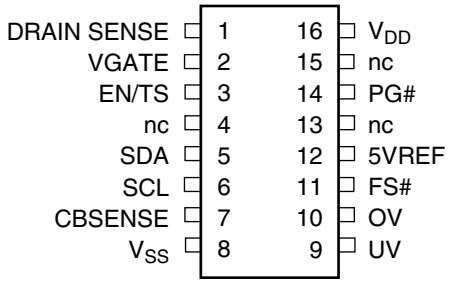
PIN CONFIGURATION

14-Pin SOIC



2062 14 PCon

16-Pin SSOP



2062 16 PCon

PIN DESCRIPTIONS

Pin No.	Type	Pin Name	Pin Description
1	I	DRAIN SENSE	The DRAIN SENSE input monitors the voltage at the drain of the MOSFET (the measure is with respect to V_{SS}). An internal 10µA source pulls the DRAIN SENSE signal towards the 5VREF level. DRAIN SENSE must be held below 2.5V to enable the PG# output.
2	O	VGATE	The VGATE output is a high side drive output, nearly equal to V_{DD}, used to turn on an external power MOSFET. This signal supplies a constant current output (100µA typical) which allows easy adjustment of the MOSFET turn-on slew rate.
3	I	EN/TS	The ENable/Temperature Sense input is the master enable input. VGATE will be disabled if EN/TS is less than 2.5V. This pin has an internal 200kΩ pullup to 5V.
4	I/O	SDA	SDA is the bidirectional serial data pin. It is configured as an open drain output. There is an internal 50kΩ resistor connected to 5VREF.
5	I	SCL	The SCL input is used to clock data into and out of the configuration registers. In the write mode data must remain stable on SDA while SCL is HIGH. In the read mode data is clocked out on the falling edge of SCL. There is an internal 50kΩ resistor connected to 5VREF.
6	I	CBSENSE	The Circuit Breaker SENSE input is used to detect over-current conditions across an external, low value sense resistor (R_S) tied in series with the power MOSFET. A voltage drop of greater than 50mV across the resistor for longer than t_{CBD} will trip the circuit breaker. To disable CBSENSE connect the pin directly to V_{SS}. A programmable Quick-Trip sense point is also available.
7	PWR	V_{SS}	V_{SS} is connected to the, negative side of the supply. All inputs and the 5VREF output are referenced to V_{SS}.
8	I	UV	The UV pin is used as an under-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE will be disabled if UV is less than 2.5V. A programmable internal hysteresis is available on the UV input, adjustable in increments of 62.5mV. A filter delay is also available on the UV input.

Note: Pin numbers reflect the 14 Pin SOIC package.

2062 Pin Table A

PIN DESCRIPTIONS (Continued)

Pin No.	Type	Pin Name	Pin Description
9	I	OV	The OV pin is used as an under-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE will be disabled if OV is greater than 2.5V. A filter delay is also available on the OV input.
10	I	FS#	The Forced Shutdown pin is an active low input that causes VGATE and the PG# output to be shut down at any time after an internal hold-off timer has expired. The hold-off timer allows supervisory circuits on the secondary side (which are not powered up initially) to control shut down of the SMH4802 via an opto-isolator. This input has no pullup resistor.
11	O	5VREF	This is a 5V output reference voltage that may be used to expand the logic input functions on the SMH4802. The reference output is with respect to V_{SS}.
12	O	PG#	PG# is an open-drain, active-low output with no internal pullup resistor. It can be used to switch a load or enable a DC/DC converter. PG# is enabled after 3 events: VGATE reaches V_{DD} - V_{GT} , the Drain Sense voltage is less than 2.5V, and the programmed delay time has expired. Voltage on this pin cannot exceed 12V as referenced to V_{SS}.
13	nc	nc	No connection
14	PWR	V_{DD}	V_{DD} is the positive supply connection. An internal shunt regulator connected between V_{DD} and V_{SS} develops approximately 12V that supplies the SMH4802. A resistor Must be placed in series with the V_{DD} pin to limit the regulator current (R_D in the application illustrations).

Note: Pin numbers reflect the 14 Pin SOIC package.

2062 Pin Table B

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Solder Temperature (10 secs) ..... 300°C
Terminal Voltage with Respect to V_{SS}:
V_{DD} ..... –0.5V to V_{DD}
OV, UV, DRAIN SENSE, SCL, SDA, FS#,
CBSENSE ..... –0.5V to V_{DD} +0.5V
EN/TS 10V
PG# ..... –0.5V to V_{DD} +0.5V
VGATE ..... V_{DD} +0.5V

RECOMMENDED OPERATING CONDITIONS

Temperature Range ..... (Industrial) –40°C to 85°C
..... (Commercial) –5°C to 70°C
$T_{J(Max)}$ ..... 150°C
$R_{\Theta J\text{-}A}$ ..... * ① 88°C/W; ② 115°C/W
$R_{\Theta J\text{-}C}$ ..... * ① 37°C/W; ② 40°C/W

Note — The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

* ① 14 pin SOIC; ② 16 pin SSOP.

DC OPERATING CHARACTERISTICS

(**Over Recommended Operating Conditions; Voltages are relative to** V_{SS}**, except** V_{GT})

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	I_{DD} = 3mA	11	12	13	V
$5V_{REF}$	5V reference output	I_{DD} = 3mA	4.75	5.00	5.25	V
I_{LOAD5}	5V reference output current	I_{DD} = 3mA	–1		1	mA
I_{DD}	Power supply current		2		10	mA
V_{UV}	Under-Voltage threshold	I_{DD} = 3mA	2.475	2.500	2.525	V
V_{UVHYST}	Under-Voltage hysteresis	I_{DD} = 3mA		63		mV
V_{OV}	Over-Voltage threshold	I_{DD} = 3mA	2.475	2.500	2.525	V
V_{OVHYST}	Over-Voltage hysteresis	I_{DD} = 3mA		10		mV
V_{GATE}	V_{GATE} output voltage				V_{DD}	V
I_{GATE}	V_{GATE} current output			100		µA
V_{SENSE}	DRAIN SENSE threshold	I_{DD} = 3mA	2.475	2.500	2.525	V
I_{SENSE}	DRAIN SENSE current output	$V_{SENSE} = V_{SS}$	–9	–10	–11	µA
V_{CB}	Circuit breaker threshold	I_{DD} = 3mA	40	50	60	mV
V_{QCB}	Programmable Quick Trip circuit breaker threshold			200		mV
				100		mV
				60		mV
			Off			—
$V_{EN/TS}$	EN/TS threshold	I_{DD} = 3mA	2.475	2.500	2.525	V
$V_{EN/TSHYST}$	EN/TS hysteresis	I_{DD} = 3mA		10		mV
V_{OL}	Output low voltage PG#	I_{OL} = 3mA	0		0.4	V
I_{IL}	Input current EN/TS	$V_{IL} = V_{SS}$		100		µA
V_{GT}	Gate threshold ($V_{GT} = V_{DD} - V_{GATE}$)		0.7	1.8	3.0	V

2062 Elect Table

AC OPERATING CHARACTERISTICS

Symbol	Description	Min.	Typ.	Max.	Units
t_{CBD}	Programmable 50mV Circuit Breaker Delay (filter)		5		µs
			50*		
			150		
			400		
t_{PGD}	Programmable Power Good Delay		5*		ms
			20		
			80		
			160		
t_{QTSD} ②	Quick Trip Shut Down		200		ns
t_{CYC}	Circuit breaker cycle time		2.5		s
			5		s
t_{PUVF}	Programmable Under-/Over-Voltage Filter		Off*		—
			5		ms
			80		ms
			160		ms
t_{SD}	Startup Delay ①		0.5		ms
			5		ms
			80 *		ms
			160		ms

2062 AC Table

* = Default value

① After UV and OV become valid there is a delay — t_{SD} — that precedes the turn on of VGATE. See Figure 6.

② Fast Shut Down delay from Fault to the beginning of VGATE off.

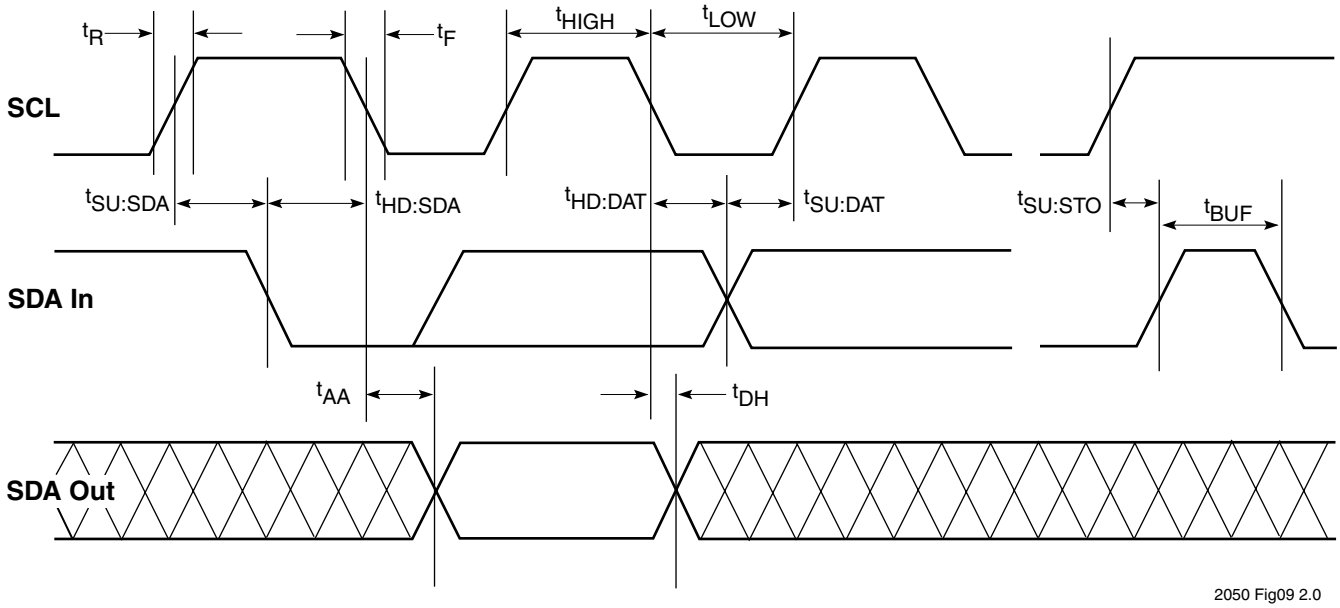
I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock low period		4.7		µs
t_{HIGH}	Clock high period		4.0		µs
t_{BUF}	Bus free time	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.2	3.5	µs
t_{DH}	Data Out hold time	SCL low (cycle n + 1) to SDA change	0.2		µs
t_R	SCL and SDA rise time			1000	ns
t_F	SCL and SDA fall time			300	ns
$t_{SU:DAT}$	Data In setup time		250		ns
$t_{HD:DAT}$	Data In hold time		0		ns
TI	Noise filter SCL and SDA	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

2062 Intf. Table

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS

Figure 3 shows a timing diagram for the Bus Interface Memory timing. One bit of data is transferred during each clock pulse. Note that data must remain stable when the clock is high.



2050 Fig09 2.0

Figure 3. Bus Interface Memory Timing

APPLICATIONS INFORMATION

Powering V_{DD}

The 12V shunt regulator between the V_{DD} and VSS pins allows the SMH4802 to operate over a wide range of supply voltages. It is necessary to use a series dropping resistor (R_D) between the host power supply and the V_{DD} pin in order to bias the shunt regulator and limit current into the device.

System Enable

The EN/TS input provides an active high comparator input that may be used as a master enable or temperature sense input.

Under-/Over-Voltage Sensing

The Under-Voltage (UV) and Over-Voltage (OV) inputs provide a set of comparators that act in conjunction with an external resistor divider network to sense when the host supply voltage exceeds the user defined limits. If the input to the UV pin rises above 2.5V, and the input to the OV pin falls below 2.5V, the power-up sequence may be initiated. If UV falls below 2.5V, or OV rises above 2.5V, the PG# and VGATE outputs will be shut down immediately.

Under-/Over-Voltage Filtering

The SMH4802 may also be configured so that an out of tolerance condition on UV/OV will not shut off the output immediately. A filter delay can be inserted so that only sustained under-voltage or over-voltage conditions will shut off the output. An out of tolerance condition on UV/OV for longer than the filter delay time (t_{UOFLTR}) will latch the VGATE and PG outputs in the off state if the UV/OV filter option is enabled. The Under-/Over-Voltage Filtering feature is disabled in the default configuration of the device.

Under-Voltage Hysteresis

The Under-Voltage comparator input may be configured with a programmable level of hysteresis. The compare level may be set in steps (up to 15) of 62.5mV below 2.5V. The default under-voltage hysteresis level is set to 62.5mV.

Soft Start Slew Rate Control

Once all of the preconditions for powering up the DC/DC converters have been met, the SMH4802 provides a means to soft start the external power FET limiting the in-rush current. Current limiting is generally needed due to the bulk capacitance across the power rails of the DC/DC converters. The VGATE output of the SMH4802 is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components.

Load Control — Turning on a DC/DC Converter

Once power has been ramped to the DC/DC converter, two conditions must be met before the PG# output can be asserted: the DRAIN SENSE voltage must be below 2.5V, and the VGATE voltage must be greater than $V_{DD} - V_{GT}$. The DRAIN SENSE input ensures the power MOSFET is not absorbing too much steady state power from operating at a high V_{DS}. (This sensor remains active at all times, except during the current regulation period).

The VGATE sensor ensures the power MOSFET is operating well into its saturation region before allowing the loads to be switched on. Once VGATE reaches $V_{DD} - V_{GT}$ this sensor is latched.

After the external MOSFET is properly switched on, the PG# output will be asserted after a delay of $t_{PGD.}$ The delay time is programmable from 5ms to 160ms.

NOTE: The PG# output has a 12V withstand capability, so high voltages must not be connected to this pin. A bipolar transistor or an opto-isolator can be used to boost the withstand voltage to that of the host supply.

Force Shutdown — Secondary Feedback

The Force Shutdown signal (FS#) is an active low input that provides a method of receiving feedback from the secondary side of the DC/DC controllers. A built-in hold-off timer allows the SMH4802 to ignore the state of the FS# input until the time period expires. The FS# input must be driven high by the end of this time period. If not, a low level on this input will shut off the VGATE and PG# outputs.

The purpose of the hold-off timer is to allow enough time for devices on the secondary side of the DC/DC controller to power-up and stabilize. This unique feature of the SMH4802 allows supervisory circuits, such as an SMS44, to control the shutdown of the primary side soft start circuit, even though the secondary side initially has no power.

Circuit Breaker Operation

The SMH4802 provides a number of circuit breaker functions to protect against over current conditions. A sustained over-current event could damage the host supply and/or the load circuitry.

The board's load current passes through a series resistor (R_S) connected between the MOSFET source (which is tied to CBSENSE) and V_{SS}. The breaker trips (Figure 4) whenever the voltage drop across R_S is greater than 50mV for more than t_{CBD} (a programmable filter delay ranging from 10µs to 500µs).

APPLICATIONS INFORMATION (Continued)

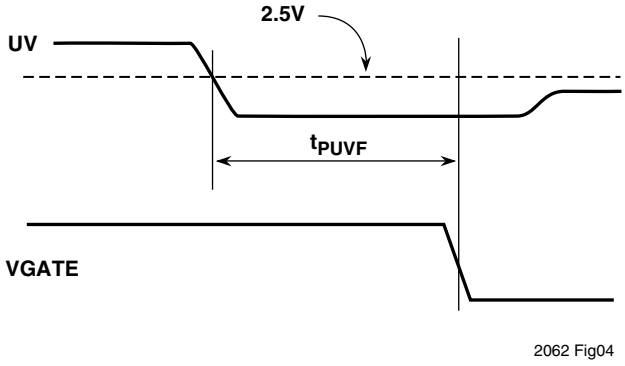


Figure 4. Under-/Over-Voltage Filter Timing

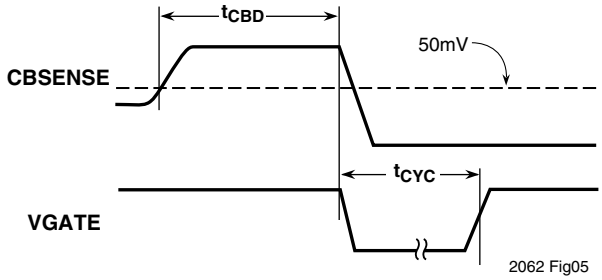
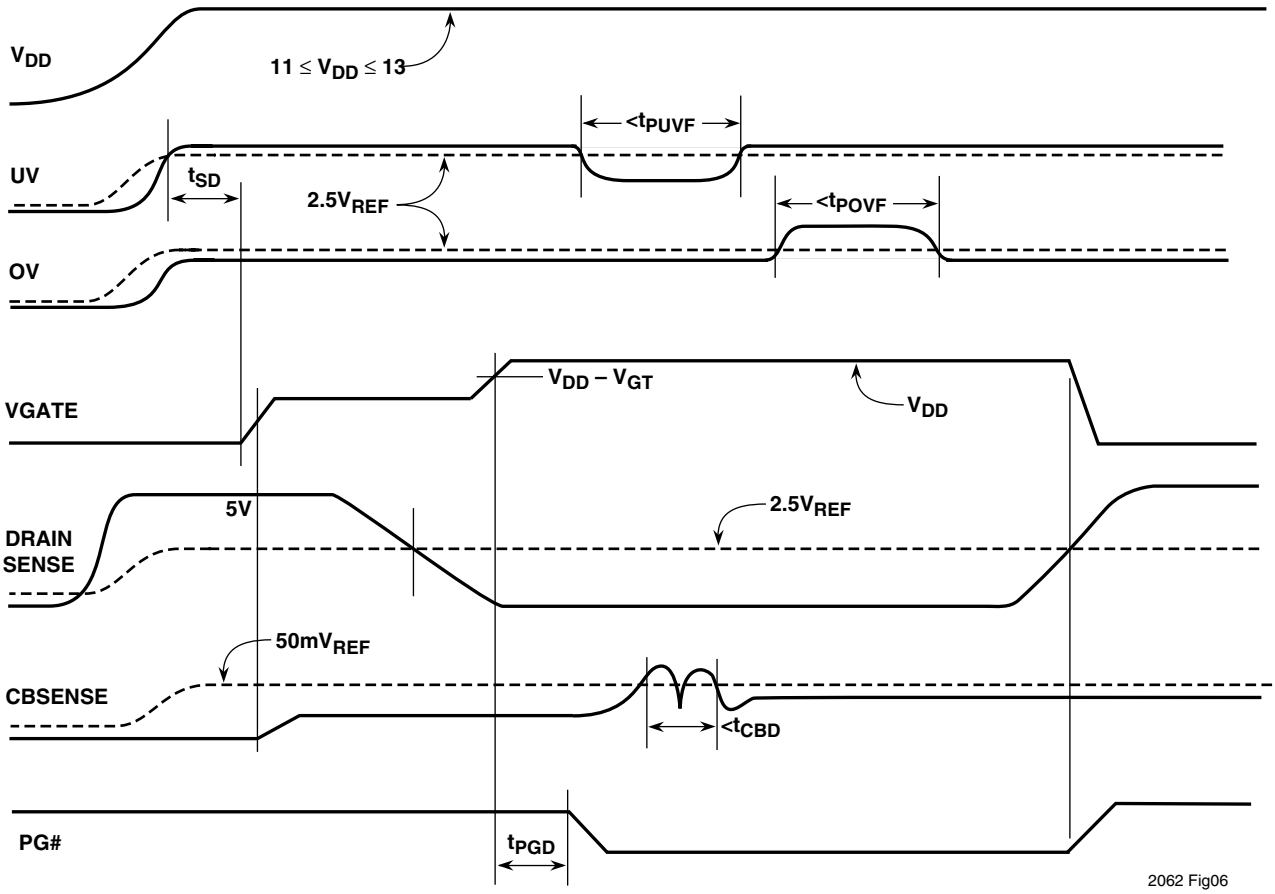


Figure 5. Circuit Breaker Cycle Mode

Power-on Timing

Figure 6 illustrates some power on sequences, including the UV and OV differentials to their reference, and Power Good cascading. Refer to the AC operating characteristics table for more information on the t_{CBD} timing.



Note: In current regulation mode the DRAIN SENSE signal will not affect the PG# output.

Figure 6. Power On Timing Sequence

APPLICATIONS INFORMATION (Continued)

Quick-Trip™ Circuit Breaker (Figure 7)

The SMH4802 provides a Quick-Trip feature that will cause the circuit breaker to trip immediately if the voltage drop across R_S exceeds V_{QCB}. The Quick-Trip can be disabled or set to 60mV, 100mV (default) or 200mV.

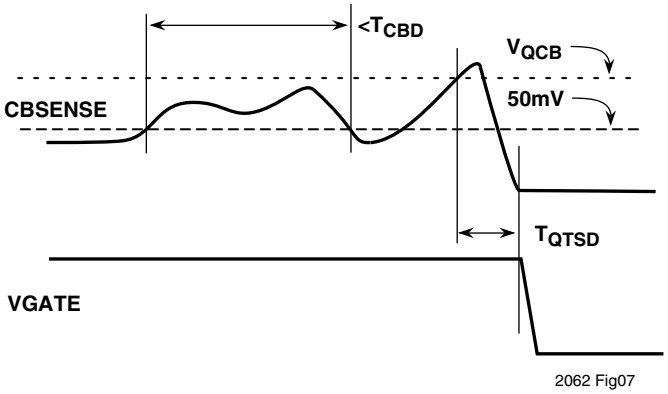


Figure 7. Circuit Breaker Quick Trip Response

Current Regulation

The current regulation mode is an optional feature that provides a means to regulate current through the MOSFET for a programmable period of time. It is generally enabled in applications that have switched dual (A and B) distributed power sources. By using the current regulation function unwarranted shutdowns can be avoided if one of the dual supplies is switched in when it is at a more negative potential than the currently operating supply.

When current regulation is selected it will be enabled during soft start (power on period) and during normal operation after the PG# output is enabled. If the voltage monitored at the CBSENSE pin is greater than 50mV, but less than V_{QCB}, the SMH4802 will reduce the VGATE voltage in order to maintain a CBSENSE potential less than 60mV, effectively regulating the current through the MOSFET.

Figures 8A and 8B illustrate the current regulation function. The time period t_{PCR} — selectable at 5, 80, or 320ms — is the maximum time during which regulation will be enforced. If either V_{QCB} or t_{PCR} are exceeded the VGATE and PG# outputs will immediately be de-asserted. However, if CBSENSE drops below 50mV before the timer ends, the timer is reset and VGATE resumes normal operation. If the Quick-Trip level is exceeded then the device will bypass the current regulation timer and shut down immediately. The Current Regulation feature is disabled in the default configuration.

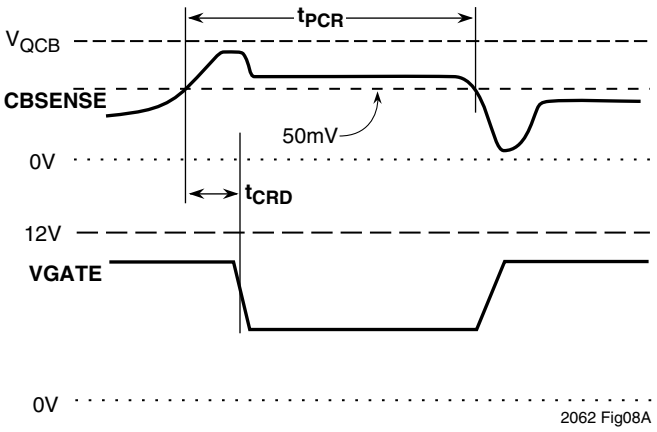


Figure 8A. Current Regulation With Recovery

Operating at High Voltages

The breakdown voltage of the external active and passive components limits the maximum operating voltage of the SMH4802 hot-swap controller. Components that must be able to withstand the full supply voltage are: the input and output decoupling capacitors, the protection diode in series with the DRAIN SENSE pin, the power MOSFET switch and the capacitor connected between its drain and gate, the high-voltage transistors connected to the power good outputs, and the dropper resistor connected to the controller's V_{DD} pin.

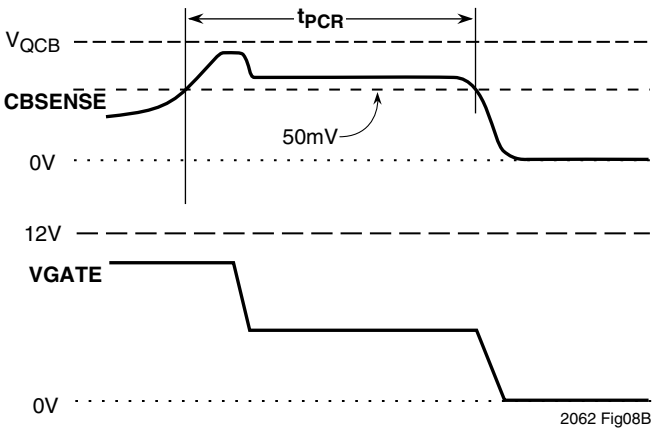


Figure 8B. Current Regulation Without Recovery

Over-Voltage and Under-Voltage Resistors

In Figure 9 the three resistors (R1, R2, and R3) connected to the OV and UV inputs must be capable of withstanding the maximum supply voltage of several hundred volts.

APPLICATIONS INFORMATION (Continued)

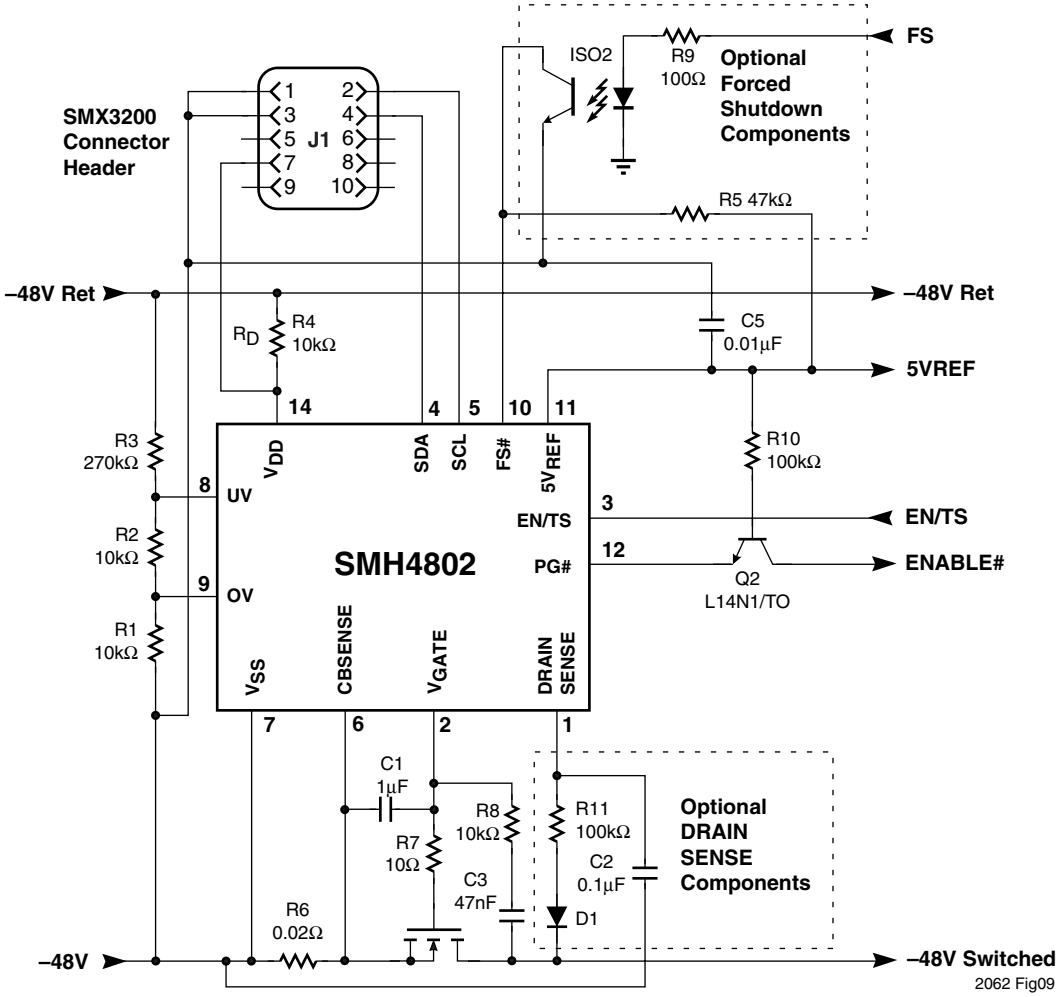


Figure 9. Example Applications Schematic.
Pin numbers reflect SOIC package.

Notes:

1. The 10Ω resistor (R7) must be located as close as possible to the MOSFET.
2. Optional interface circuit (Q2). The PG# output can be directly connected to the power module if the input voltage to the module is within tolerance and the voltage on the PG# output doesn't exceed 15V.
3. If the DRAIN SENSE signal is not used tie the pin directly to V_{SS} (pin 7).

The trip voltage of the UV and OV inputs is 2.5V relative to V_{SS}. Large value resistors can be used in the resistive divider as the input impedance of UV and OV is very high. The divider resistors should be high stability 1% metal-film resistors to keep the under-voltage and over-voltage trip points accurate.

Telecom Design Example

A hot-swap telecom application may use a 48V power supply with a –25% to +50% tolerance (*i.e.*, the 48V supply can vary from 36V to 72V). The formulas for calculating R1, R2, and R3 are as follows.

First, a peak current, ID_{MAX}, must be specified for the resistive network. The value of the current is arbitrary, but it cannot be too high (self-heating in R3 becomes a problem) or too low (the value of R3 becomes very large, and leakage currents can reduce the accuracy of the OV and UV trip points). The value of IDMAX should be ≥200µA for the best accuracy at the OV and UV trip points. A value

APPLICATIONS INFORMATION (Continued)

of 250µA for IDMAX is used to illustrate the following calculations.

With V_{OV} (2.5V) being the over-voltage trip point, R1 is calculated by the formula:

$$R1 = \frac{V_{OV}}{ID_{MAX}}$$

Substituting:

$$R1 = \frac{2.5V}{250\mu A} = 10k\Omega$$

Next the minimum current that flows through the resistive divider, ID_{MIN}, is calculated from the ratio of minimum and maximum supply voltage levels:

$$ID_{MIN} = \frac{ID_{MAX} \times VS_{MIN}}{VS_{MAX}}$$

Substituting:

$$ID_{MIN} = \frac{250\mu A \times 36V}{2.5V} = 125\mu A$$

Now the value of R3 is calculated from ID_{MIN}:

$$R3 = \frac{VS_{MIN} \times V_{UV}}{ID_{MIN}}$$

V_{UV} is the under-voltage trip point, also 2.5V. Substituting:

$$R3 = \frac{36V \times 2.5V}{125\mu A} = 286k\Omega$$

The closest standard 1% resistor value is 267kΩ

Then R2 is calculated:

$$R2 = \frac{2.5V}{125\mu A} - 10k\Omega = 20k\Omega - 10k\Omega = 10k\Omega$$

or

$$R2 = \frac{V_{UV}}{ID_{MIN}} - R1$$

Substituting:

$$R2 = \frac{2.5V}{125\mu A} - 10k\Omega = 20k\Omega - 10k\Omega = 10k\Omega$$

An Excel spread sheet is available on Summit's website (www.summitmicro.com) to simplify the resistor value calculations and tolerance analysis for R1, R2, and R3.

Dropper Resistor Selection

The SMH4802 is powered from the high-voltage supply via dropper resistor R_D. The dropper resistor must provide the SMH4802 (and its loads) with sufficient operating current under minimum supply voltage conditions, but must not allow the maximum supply current to be exceeded under maximum supply voltage conditions.

The dropper resistor value is calculated from:

$$R_D = \frac{VS_{MIN} - V_{DD_{MAX}}}{I_{DD} - I_{LOAD}}$$

where VS_{MIN} is the lowest operating supply voltage, V_{DDMAX} is the upper limit of the SMH4802 supply voltage, I_{DD} is minimum current required for the SMH4802 to operate, and I_{LOAD} is any additional load current from the 2.5V and 5V outputs and between V_{DD} and V_{SS}.

Calculate the minimum wattage required for RD from:

$$P_{RO} \geq \frac{\left(VS_{MAX} - V_{DD_{MIN}}\right)^2}{R_D}$$

where V_{DDMIN} is the lower limit of the SMH4802 supply voltage, and VS_{MAX} is the highest operating supply voltage.

In circumstances where the input voltage may swing over a wide range (*e.g.,* from 20V to 100V) the maximum current may be exceeded. In these circumstances it may be necessary to add an 11V Zener diode between V_{DD} and V_{SS} to handle the wide current range. The Zener voltage should be below the nominal regulation voltage of the SMH4802 so that it becomes the primary regulator.

MOSFET V_{DS}(ON) Threshold

The drain sense input on the SMH4802 monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. When the MOSFET's V_{DS} is below the user-defined threshold the MOSFET switch is considered to be ON. The $V_{DS}(ON)_{THRESHOLD}$ is adjusted using the resistor R_T in series with the drain sense protection diode. This protection, or blocking, diode prevents high voltage breakdown of the drain sense input when the MOSFET switch is OFF. A low leakage MMBD1401 diode offers protection up to 100V. For high voltage applications (up to 500V) the Central Semiconductor CMR1F-10M diode should be used. The $V_{DS}(ON)_{THRESHOLD}$ is calculated from:

$$V_{DS}(ON)_{THRESHOLD} = V_{SENSE} - (I_{SENSE} - R_T) - V_{DIODE}$$

APPLICATIONS INFORMATION (Continued)

where V_{DIODE} is the forward voltage drop of the protection diode. The $V_{DS}(ON)_{THRESHOLD}$ varies over temperature due to the temperature dependence of V_{DIODE} and I_{SENSE}. The calculation below gives the $V_{DS}(ON)_{THRESHOLD}$ under the worst case condition of 85°C ambient. Using a 68kΩ resistor for R_T gives:

$$V_{DS}(ON)_{THRESHOLD} = 2.5V - (15\mu A \times 68k\Omega) - 0.5V = 1V$$

The voltage drop across the MOSFET switch and sense resistor, V_{DSS}, is calculated from:

$$V_{DSS} = I_D (R_S \times R_{ON})$$

where I_D is the MOSFET drain current, RS is the circuit breaker sense resistor and R_{ON} is the MOSFET on resistance.

The dropper resistor value should be chosen such that the minimum and maximum I_{DD} and V_{DD} specifications of the SMH4802 are maintained across the host supply's valid operating voltage range. First, subtract the minimum V_{DD} of the SMH4802 from the low end of the voltage, and divide by the minimum I_{DD} value. Using this value of resistance as R_D find the operating current that would result from running at the high end of the supply voltage to verify that the resulting current is less than the maximum I_{DD} current allowed. If some range of supply voltage is chosen that would cause the maximum I_{DD} specification to be violated, then an external zener diode with a breakdown voltage of 11V should be used across V_{DD}.

As an example of choosing the proper R_D value, assume the host supply voltage ranges from 36 to 72V. The largest dropper resistor that can be used is: (36V-11V)/3mA = 8.3kΩ. Next, confirm that this value of R_D also works at the high end: (72V-13V)/8.3kΩ = 7.08mA, which is less than 8mA.

The FS# input can also be used in conjunction with a secondary-side supervisory circuit providing a positive feedback loop during the power up sequence. As an example, assume the SMH4802 is configured to turn on –48V to three DC/DC converters and then sequentially turn on the converters with a 1.6ms delay. Further, assume all of the enable inputs are true and PG# has just been sequenced on. If FS# option 4 (100_{BIN} in register 5) has been selected, then FS# must be driven high within 1.6ms after PG# goes low, otherwise the PG# output is disabled.

Ideally, there would be a secondary-side supervisor similar to the SMS44 that would have its reset time-out period programmed to be less than 1.6ms. After the last supply turns on, the RESET# output of the SMS44 would be released and FS# pulled high. However, if for any reason not all of the supplies turn on, RESET# is not released and the SMH4802 disables the PG# output.

Soft Start Slew Rate Control

The –48V turn on time is controlled by the SMH4802 and by the values of R8, C1 and C3 in Figure 9. The turn on time is approximately 10ms with the component values shown. Increasing the capacitance reduces the output slew rate and increases the turn on time. The capacitors prevent the MOSFET from turning on simultaneously with the application of –48V. Resistor R8 is specified to limit the current into and the rate of charge of C1. The ratio of C1 to C3 (20:1) limits the MOSFET's V_{GS} to approximately 2V once the –48V supply is connected and C1 is fully charged.

DEVELOPMENT HARDWARE & SOFTWARE

PROGRAMMING CONNECTION

The SMH4802 uses the industry standard I²C 2-wire serial data interface. This interface provides access to the configuration registers and the nonvolatile fault latch.

Device configuration utilizing the Windows based SMH4802 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMH4802. The Dongle connects directly to the parallel port of a PC and the target application. It programs the device through a cable using the I²C bus protocol.

The SMX3200 system consists of a programming Dongle, cable and Windows GUI software. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website.

When design prototyping is complete, the software can generate a HEX data file that should then be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

The Windows GUI software will generate the data and send it in I²C serial bus format so that it can be directly downloaded to the SMH4802 via the programming Dongle and cable. An example of the connection interface is shown in Figure 10.

When design prototyping is complete the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

Caution: If the device is powered from -48V during programming damage may occur when connecting the dongle to a system utilizing an earth-connected positive terminal. Either disabling the -48V connection or using a laptop computer is the best way to avoid damage.

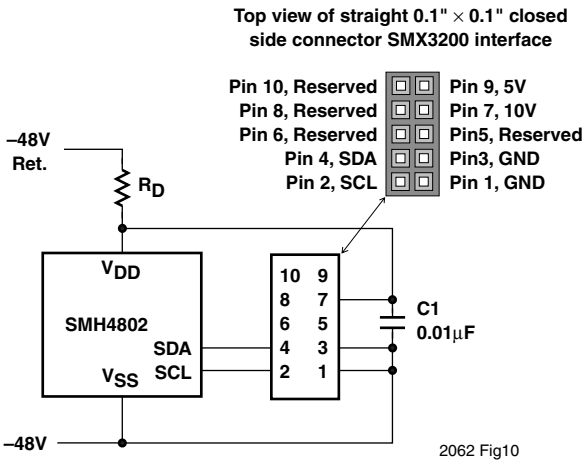


Figure 10. SMX3200 Programmer I²C serial bus connections.

Pin numbers reflect SOIC package.

PROGRAMMING INFORMATION

I²C Bus Interface

The I²C bus is a two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA) and a serial clock line (SCL). The SMH4802 supports a 100 kHz clock rate.

The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. The SMH4802 contains a Schmitt input on both the SDA and SCL signals.

Start and Stop Conditions

Both the SDA and SCL pins remain high when the bus is not busy. Data transfers between devices may be initiated with a Start condition only when SCL and SDA are high. A high-to-low transition of the SDA while the SCL pin is high is defined as a Start condition. A low-to-high transition on SDA while SCL is high is defined as a Stop condition. Figure 11 shows a timing diagram of the start and stop conditions.

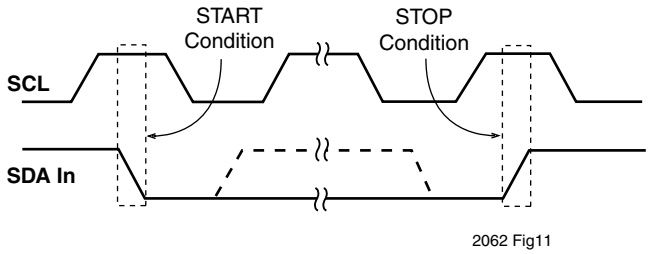


Figure 11. Start and Stop Conditions

Master/Slave Protocol

The master/slave protocol defines any device that sends data onto the bus as a transmitter, and any device that receives data as a receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the SMH4802 is referred to as a Slave device since it never initiates any data transfers.

Acknowledge

Data is always transferred in bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The transmitting device releases the bus after transmitting eight bits. During the ninth clock cycle the Receiver pulls the SDA line low to acknowledge that it received the eight bits of data. This is shown by the ACK in Figure 12.

When the last byte has been transferred to the Master during a read of the SMH4802 the Master leaves SDA high for a Not Acknowledge (NACK) cycle. This causes the SMH4802 part to stop sending data, and the Master issues a Stop on the clock pulse following the NACK.

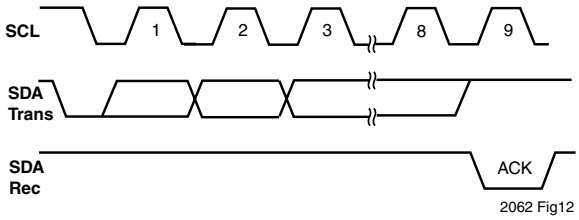


Figure 12. Acknowledge Timing

Read and Write

The first byte from a Master is always made up of a 7-bit Slave address and the Read/Write (R/W) bit. The R/W bit tells the Slave whether the Master is reading data from the bus or writing data to the bus (1 = Read, 0 = Write). The first four of the seven address bits are called the Device Type Identifier (DTI). The DTI for the SMH4802 is 1010_{BIN}. The next three bits are Address values for A2, A1, and A0 (if multiple devices are used). The SMH4802 issues an Acknowledge after recognizing a Start condition and its DTI. Figure 13 shows an example of a typical master address byte transmission.

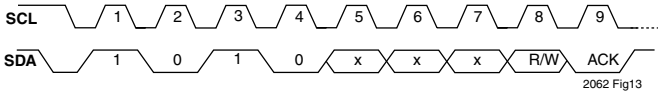


Figure 13. Typical Master Address Byte Transmission

During a read by the Master device the SMH4802 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SMH4802 continues to transmit data. If an Acknowledge is not detected (NACK) the SMH4802 terminates any subsequent data transmission. The read transfer protocol on SDA is shown in Figure 14.

During a Master write the SMH4802 receives eight bits of data, then generates an Acknowledge signal. The device continues to generate the ACK condition on SDA until a Stop condition is generated by the Master. The write transfer protocol on SDA is shown in Figure 15.

Random Access Read

Random address read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMH4802 to the desired address.

PROGRAMMING INFORMATION (Continued)

After the word address Acknowledge is received by the Master it immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SMH4802 responds with an Acknowledge and then transmits the 8 data bits stored at the addressed location. At this point, the Master sets the SDA line to NACK and generates a Stop condition. The SMH4802 discontinues data transmission and reverts to its standby power mode.

Sequential Reads

Sequential reads can be initiated as either a current address read or a random access read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMH4802.

The SMH4802 continues to output data for each Acknowledge received. The Master sets the SDA line to NACK and generates a Stop condition. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal.

For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter rolls over and the memory continues to output data.

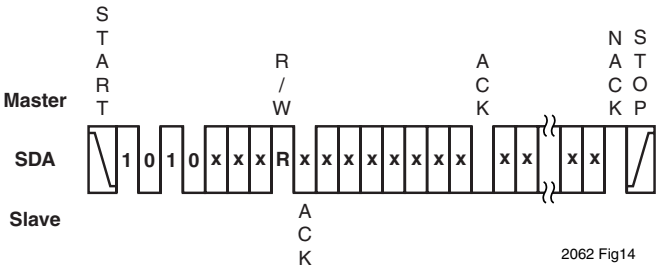


Figure 14. Read Protocol

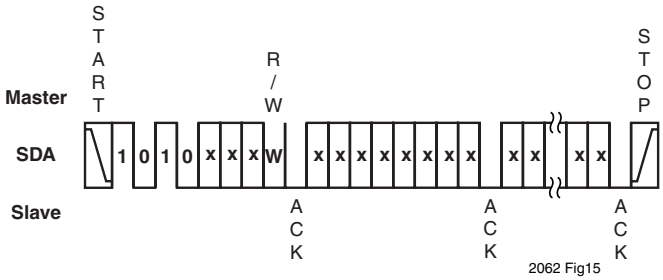


Figure 15. Write Protocol

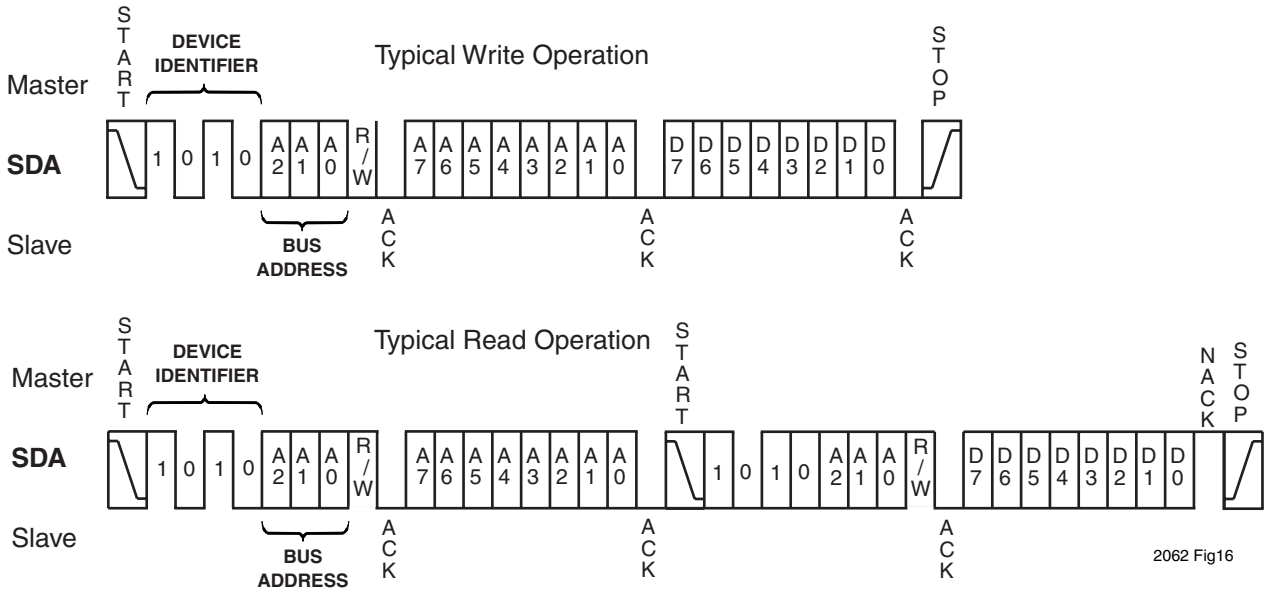


Figure 16. Sequential Bus Cycles

PROGRAMMING INFORMATION (Continued)

Register Access

The SMH4802 contains a 2-wire bus interface for register access as explained in the previous section. This bus is highly configurable while maintaining the industry standard protocol. The SMH4802 responds to one of two selectable Device Type Addresses: 1010_{BIN}, generally assigned to NV-memories, or 1011_{BIN}, which is the default address for the SMH4802. The Device Type Address is assigned by programming bit 3 of Register 8.

Register accesses are also programmable using bits 2 and 1 of Register 8. Accesses can be denied (no reads or writes), read only, or read/write (default state).

The SMH4802 has three address pins (A2, A1 and A0) associated with the 2-wire bus. The SMH4802 can be configured to respond only to the proper serial data string of the Device Type Address and specific bus addresses (Register 8, bit 0 set); or to the Device Type Address and any bus address (Register 8, bit 0 cleared).

Master/Slave Protocol

The master/slave protocol defines any device that sends data onto the bus as a transmitter and any device that receives data as a receiver. The device controlling data transmission is called the Master and the controlled device is called the Slave. The SMH4802 is always a Slave device since it never initiates any data transfers. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because a change on the data line while SCL is high is interpreted as either a Start or a Stop condition.

Register Bit Maps

The SMH4802 has eight user programmable, nonvolatile configuration registers. Although 8-bit data transfers are used for reading and writing the registers, only the 4 least significant bits of each register are utilized by the device. Therefore, in each of the following registers, bits 7 through 4 are left blank. Bits 3 through 0 are used as shown for each register.

DEFAULT CONFIGURATION REGISTER SETTINGS - SMH4802-169

Register	Hex Contents	Description
R02	9	Over-current delay and Quick-Trip over-current reference level.
R03	2	Power good sequencing delay. CB mode enable.
R04	B	PG# enable, over-/under-voltage filter delay, circuit breaker cycle time.
R05	C	Non-volatile fault latch enable, FS# function control.
R06	C	Under- and over-voltage filter enables, VGATE current regulation control.
R07	9	Under-voltage hysteresis control.
R08	1	I^2C control, including device type address, configuration register read/write status, and slave address response control.
R09	9	Power good sequence speed.
R0C	0	Non-volatile fault latch. Set by hardware when fault is detected.

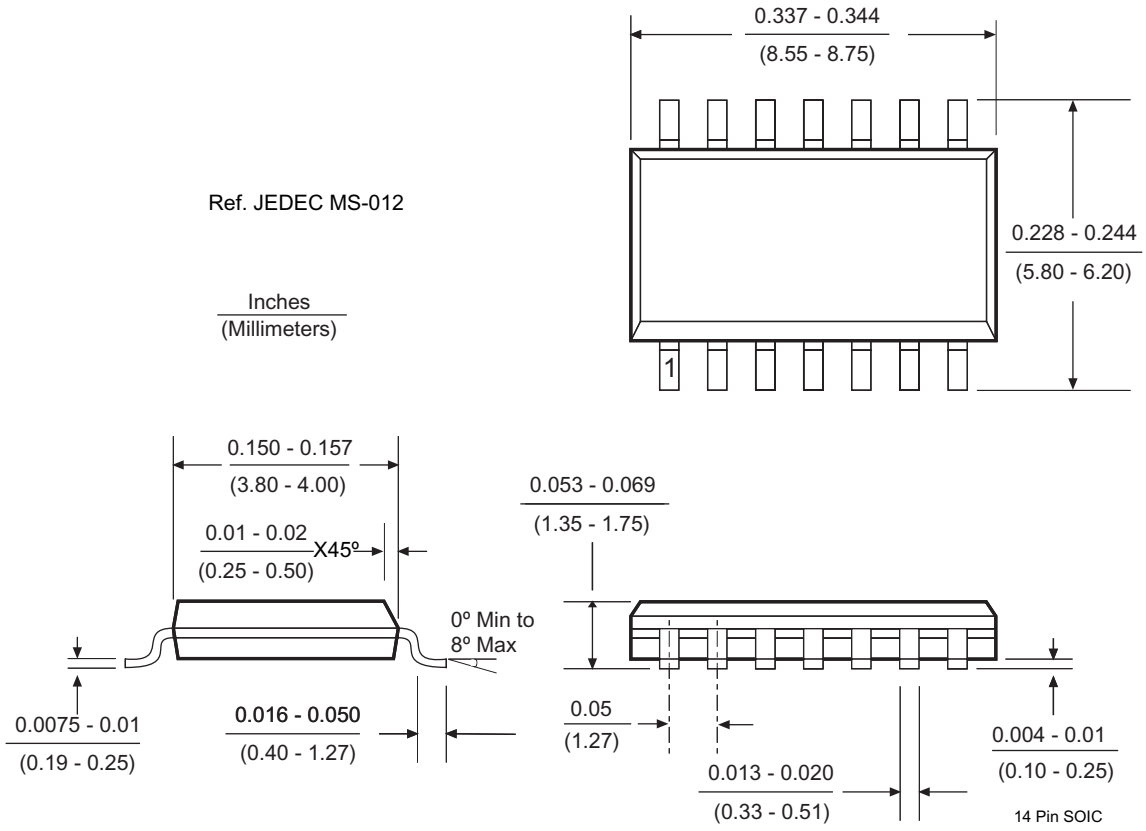
2062 Reg Table

PACKAGES

14 PIN SOIC PACKAGE

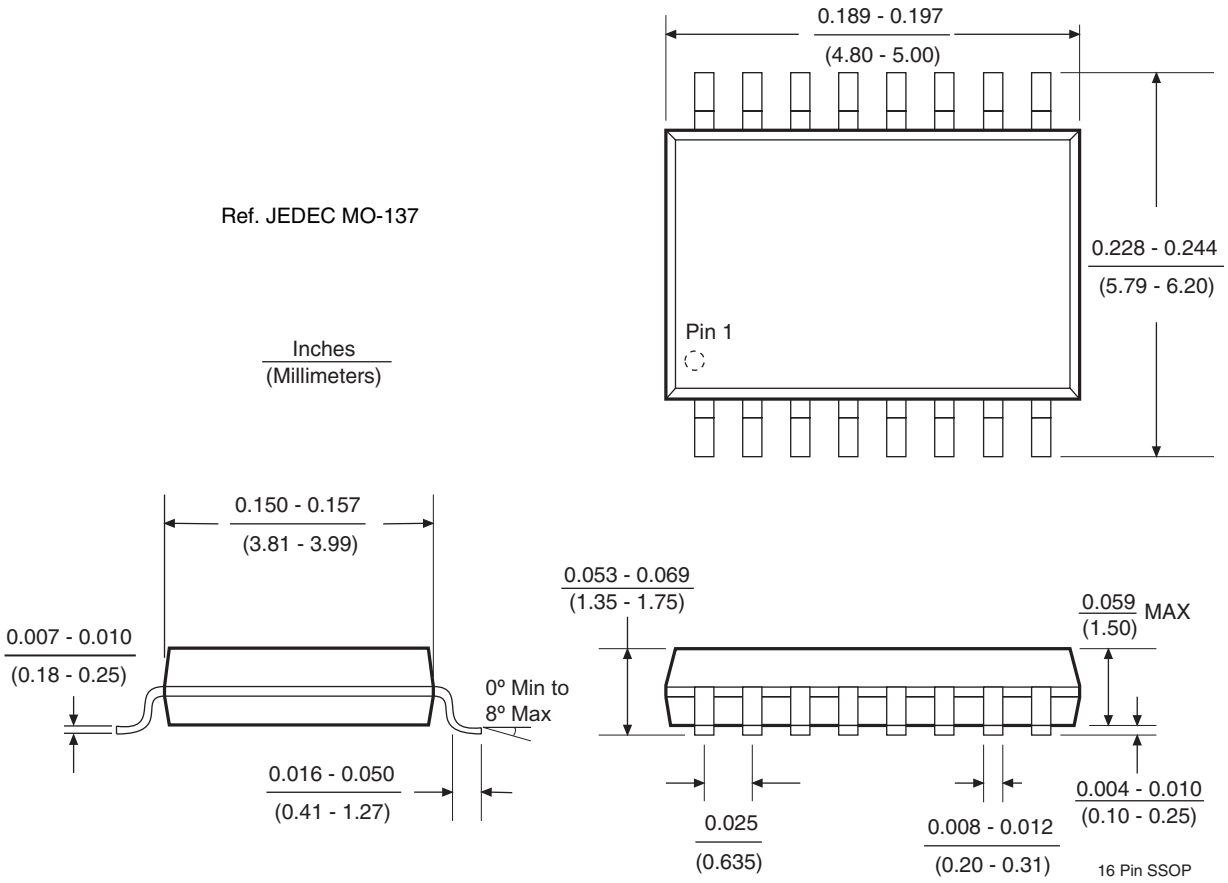
Ref. JEDEC MS-012

Inches
(Millimeters)

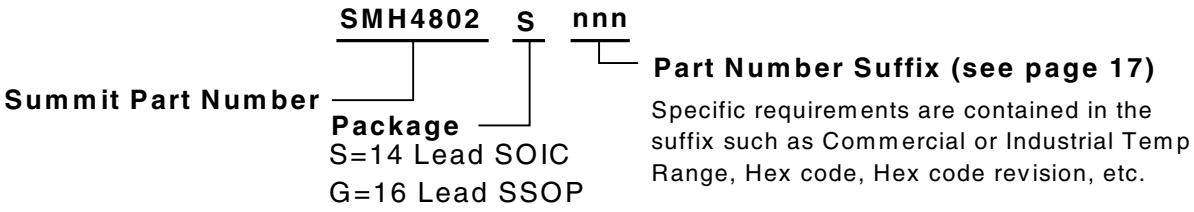


PACKAGES (Continued)

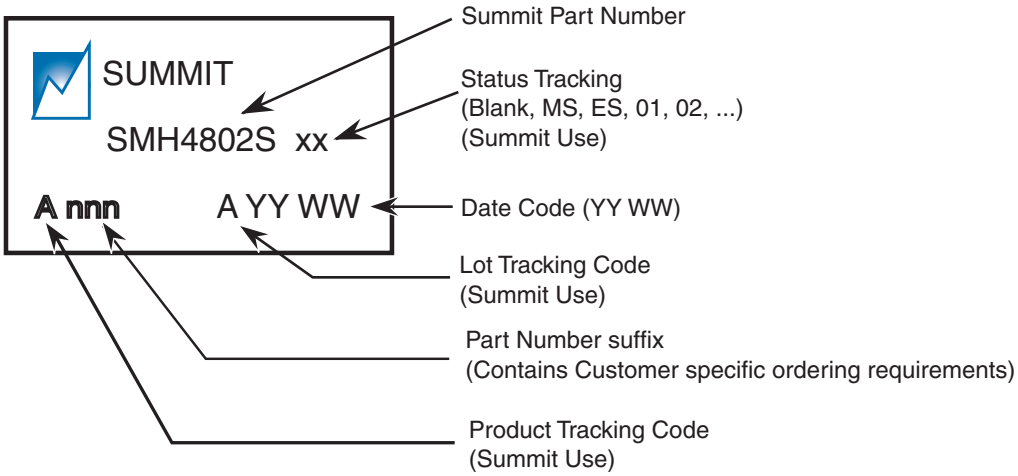
16 PIN SSOP PACKAGE



ORDERING INFORMATION



PART MARKING



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