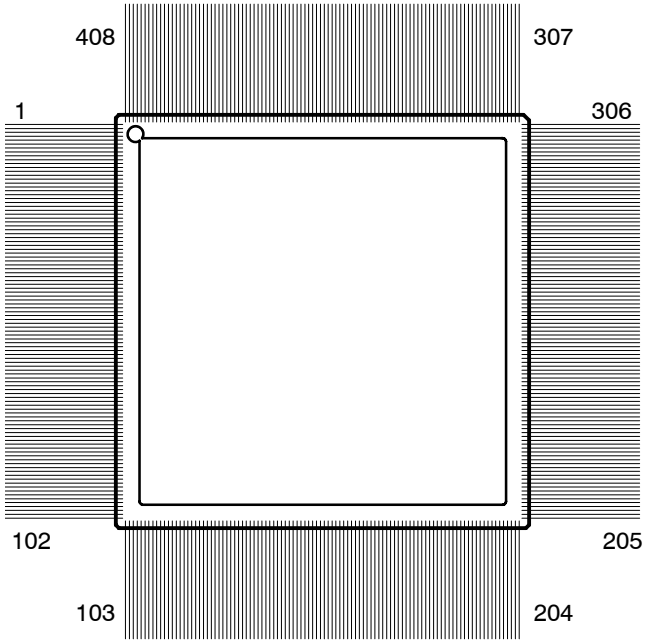
- **Performance:**
  - **80 Million Floating-Point Operations Per Second (MFLOPS) With 496-MBps-Burst I/O Rate for 40-MHz Modules**
  - **Zero-Wait-State Local Memory for Each Processor**
- **Organization:**
  - **128K-Word × 32-Bit Static Random-Access Memory (SRAM) (SMJ320MCM42D)**
  - **256K-Word × 32-Bit SRAM (SMJ320MCM42C)**
- **Compliant With MIL-PRF-38535 QML**
- **Dual C40 Performance With Local Memory Requiring Only 8.7 Square Inches of Board Space**
- **Enhanced Performance Offered By Multichip-Module Solution**
  - **SMJ320MCM42C**
    - **67% Reduction in Number of Interconnects**
    - **54% Reduction (Minimum) in Board Area**
    - **Estimated 38% Reduction in Power Dissipation Due to Reduced Parasitic Capacitance and Interconnect Lengths**
  - **SMJ320MCM42D**
    - **56% Reduction in Number of Interconnects**
    - **30% Reduction (Minimum) in Board Area**
    - **Estimated 20% Reduction in Power Dissipation Due to Reduced Parasitic Capacitance and Interconnect Lengths**
- **Four Memory Ports for High Data Bandwidth**
  - **Two Full 2G-Word External Buses**
- **Two Internal Buses Mapped to Memory**
  - **128K-Word × 32-Bit SRAM for Each C40 Local Bus (SMJ320MCM42D)**
  - **256K-Word × 32-Bit SRAM for Each C40 Local Bus (SMJ320MCM42C)**
- **Ten External Communication Ports for Direct Processor-to-Processor Communication**

HFN PACKAGE‡
(TOP VIEW)



‡ Terminal assignment information is provided by the terminal assignments table. Package is shown for pinout reference only.

- **IEEE-1149.1† (JTAG) Boundary-Scan Compatible**
- **408-Lead Ceramic Quad Flatpack Package (HFN Suffix)**
- **Operating Free-Air Temperature Ranges:**
  –55°C to 125°C . . . (Military)
  0°C to 70°C . . . (Commercial)
- **Communication-Port Connection Provided Between C40s for Interprocessor Communication**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† IEEE Standard 1149.1–1990 Standard Test-Access Port and Boundary-Scan Architecture

description

The 42 dual C40 multichip module (MCM) contains two SMJ320C40 digital signal processors (DSPs) with 128K words × 32 bits (42D) or 256K words × 32 bits (42C) of zero-wait-state SRAMs mapped to each local bus. Global address and data buses with two sets of control signals are routed externally for each processor, allowing external memory to be accessed. The external global bus provides a continuous address reach of 2G words.

The dual C40 configuration allows standard microprocessor initialization using the bootstrap loader. Both reset-vector-control terminals are brought out to external terminals for each processor. A single CLKIN line and a RESET line feed both processors in parallel, minimizing clock skew and allowing easy synchronization for interlocked operations.

Communication port 0 of CPU #1 connects to communication port 3 of CPU #2 for direct processor-to-processor communication.

The IEEE-1149.1 (JTAG) test ports of the C40s are connected serially to allow scan operations and emulation of the module as a whole. Testability of the 42 adds value and reduces development and support costs. Texas Instruments offers a wide variety of ANSI/IEEE-1149.1 products and support.

The 42 dual C40 MCM is packaged in a 408-pin ceramic quad flat pack. The 42 dual C40 MCM is available in both a commercial temperature range (0°C to 70°C) and a military temperature range (–55°C to 125°C) option.

For additional information when designing for cold temperature operation, please see Texas Instruments application report *320C3x, 320C4x and 320MCM42x Power-up Sensitivity at Cold Temperature*, literature number SGUA001.

device symbol nomenclature

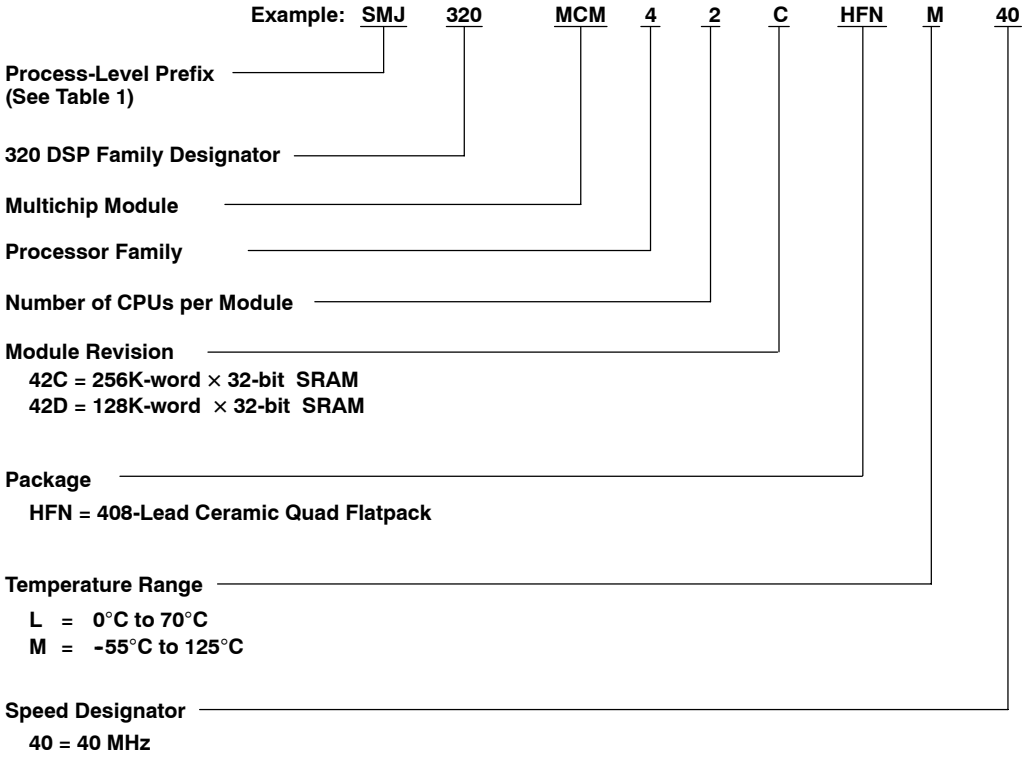


Table 1. MCM Processing Matrix

PROCESS LEVEL	TEMPERATURE RANGE		DIE	100% PROCESSED	SPEED TEST	TEST TEMPERATURE RANGE	QUALIFICATION TESTING
SM	L version	0°C to 70°C	Probed	No	No	25°C to 70°C	Package
	M version	–55°C to 125°C	Probed	No	Yes	–55°C to 125°C	Package
SMJ†	M version	–55°C to 125°C	KGD‡	Yes	Yes	–55°C to 125°C	MIL-H-38534

† SMJ-level product is full MIL-PRF-38535 QML compliant.
‡ KGD stands for the known-good-die strategy as defined in the reference documentation section.

Terminal Assignments

TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME	TERMINAL NO.	TERMINAL NAME
1	ROMEN_C40_#1	52	A10_C40_#1	103	$\overline{\text{RDY1\_C40\_\#2}}$	154	C4D5_C40_#2
2	IIOF0_C40_#1	53	A9_C40_#1	104	V_{SS}_DR	155	C4D4_C40_#2
3	IIOF1_C40_#1	54	A8_C40_#1	105	V_{SS}_CL	156	C4D3_C40_#2
4	IIOF2_C40_#1	55	A7_C40_#1	106	$\overline{\text{LOCK\_C40\_\#2}}$	157	C4D2_C40_#2
5	IIOF3_C40_#1	56	A6_C40_#1	107	V_{CC}_CL	158	C4D1_C40_#2
6	$\overline{\text{NMI\_C40\_\#1}}$	57	A5_C40_#1	108	V_{SS}_CL	159	C4D0_C40_#2
7	V_{CC}_DR	58	A4_C40_#1	109	$\overline{\text{CE0\_C40\_\#2}}$	160	V_{CC}_DR
8	V_{SS}_CL	59	V_{CC}_DR	110	$\overline{\text{RDY0\_C40\_\#2}}$	161	V_{CC}_DR
9	TCLK0_C40_#1	60	A3_C40_#1	111	$\overline{\text{DE\_C40\_\#2}}$	162	V_{SS}_CL
10	TCLK1_C40_#1	61	A2_C40_#1	112	TCK_COMM	163	C2D7_C40_#2
11	H3_C40_#1	62	A1_C40_#1	113	TDO_C40_#2	164	C2D6_C40_#2
12	H1_C40_#1	63	A0_C40_#1	114	TMS_COMM	165	C2D5_C40_#2
13	V_{SS}_CL	64	D31_C40_#2	115	$\overline{\text{TRST\_COMM}}$	166	C2D4_C40_#2
14	$\overline{\text{IACK\_C40\_\#1}}$	65	D30_C40_#2	116	EMU0_COMM	167	C2D3_C40_#2
15	CLKIN_COMM	66	D29_C40_#2	117	EMU1_COMM	168	C2D2_C40_#2
16	V_{CC}_DR	67	D28_C40_#2	118	PAGE1_C40_#2	169	C2D1_C40_#2
17	V_{CC}_CL	68	D27_C40_#2	119	R/$\overline{\text{W}}$1_C40_#2	170	C2D0_C40_#2
18	V_{CC}_DR	69	D26_C40_#2	120	$\overline{\text{STRB1\_C40\_\#2}}$	171	$\overline{\text{CRDY2\_C40\_\#2}}$
19	V_{SS}_CL	70	V_{CC}_DR	121	STAT0_C40_#2	172	$\overline{\text{CSTRB2\_C40\_\#2}}$
20	V_{SS}_DR	71	D25_C40_#2	122	STAT1_C40_#2	173	$\overline{\text{CACK2\_C40\_\#2}}$
21	V_{CC}_DR	72	D24_C40_#2	123	V_{SS}_CL	174	$\overline{\text{CREQ2\_C40\_\#2}}$
22	V_{CC}_DR	73	D23_C40_#2	124	STAT2_C40_#2	175	V_{CC}_DR
23	V_{CC}_CL	74	D22_C40_#2	125	STAT3_C40_#2	176	$\overline{\text{CRDY1\_C40\_\#2}}$
24	V_{SS}_CL	75	D21_C40_#2	126	PAGE0_C40_#2	177	$\overline{\text{CSTRB1\_C40\_\#2}}$
25	V_{SS}_DR	76	D20_C40_#2	127	R/$\overline{\text{W}}$0_C40_#2	178	$\overline{\text{CACK1\_C40\_\#2}}$
26	V_{SS}_CL	77	D19_C40_#2	128	$\overline{\text{STRB0\_C40\_\#2}}$	179	$\overline{\text{CREQ1\_C40\_\#2}}$
27	V_{CC}_DR	78	D18_C40_#2	129	$\overline{\text{AE\_C40\_\#2}}$	180	$\overline{\text{CRDY0\_C40\_\#2}}$
28	A30_C40_#1	79	D17_C40_#2	130	RESETLOC1_C40_#2	181	$\overline{\text{CSTRB0\_C40\_\#2}}$
29	A29_C40_#1	80	D16_C40_#2	131	V_{CC}_DR	182	$\overline{\text{CACK0\_C40\_\#2}}$
30	A28_C40_#1	81	V_{SS}_CL	132	RESETLOC0_C40_#2	183	$\overline{\text{CREQ0\_C40\_\#2}}$
31	V_{CC}_DR	82	V_{SS}_CL	133	$\overline{\text{RESET\_COMM}}$	184	V_{SS}_DR
32	A27_C40_#1	83	V_{CC}_DR	134	$\overline{\text{CRDY5\_C40\_\#2}}$	185	V_{SS}_CL
33	A26_C40_#1	84	V_{SS}_DR	135	$\overline{\text{CSTRB5\_C40\_\#2}}$	186	V_{SS}_DR
34	A25_C40_#1	85	D15_C40_#2	136	$\overline{\text{CACK5\_C40\_\#2}}$	187	V_{CC}_DR
35	A24_C40_#1	86	D14_C40_#2	137	$\overline{\text{CREQ5\_C40\_\#2}}$	188	C1D7_C40_#2
36	A23_C40_#1	87	D13_C40_#2	138	$\overline{\text{CRDY4\_C40\_\#2}}$	189	C1D6_C40_#2
37	A22_C40_#1	88	D12_C40_#2	139	$\overline{\text{CSTRB4\_C40\_\#2}}$	190	C1D5_C40_#2
38	A21_C40_#1	89	D11_C40_#2	140	$\overline{\text{CACK4\_C40\_\#2}}$	191	C1D4_C40_#2
39	A20_C40_#1	90	D10_C40_#2	141	$\overline{\text{CREQ4\_C40\_\#2}}$	192	C1D3_C40_#2
40	A19_C40_#1	91	D9_C40_#2	142	V_{CC}_DR	193	C1D2_C40_#2
41	A18_C40_#1	92	D8_C40_#2	143	C5D7_C40_#2	194	C1D1_C40_#2
42	A17_C40_#1	93	D7_C40_#2	144	C5D6_C40_#2	195	C1D0_C40_#2
43	V_{CC}_DR	94	D6_C40_#2	145	C5D5_C40_#2	196	V_{CC}_DR
44	V_{SS}_CL	95	D5_C40_#2	146	C5D4_C40_#2	197	C0D7_C40_#2
45	V_{SS}_DR	96	V_{CC}_DR	147	C5D3_C40_#2	198	C0D6_C40_#2
46	A16_C40_#1	97	D4_C40_#2	148	C5D2_C40_#2	199	C0D5_C40_#2
47	A15_C40_#1	98	D3_C40_#2	149	C5D1_C40_#2	200	C0D4_C40_#2
48	A14_C40_#1	99	D2_C40_#2	150	C5D0_C40_#2	201	C0D3_C40_#2
49	A13_C40_#1	100	D1_C40_#2	151	V_{CC}_DR	202	C0D2_C40_#2
50	A12_C40_#1	101	D0_C40_#2	152	C4D7_C40_#2	203	C0D1_C40_#2
51	A11_C40_#1	102	$\overline{\text{CE1\_C40\_\#2}}$	153	C4D6_C40_#2	204	C0D0_C40_#2

Terminal Assignments (Continued)

TERMINAL		TERMINAL		TERMINAL		TERMINAL	
NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
205	ROMEN_C40_#2	256	A9_C40_#2	307	V_{SS}_DR	358	V_{SS}_DR
206	IIOF0_C40_#2	257	A8_C40_#2	308	V_{SS}_CL	359	V_{CC}_DR
207	IIOF1_C40_#2	258	A7_C40_#2	309	$\overline{\text{LOCK\_C40\_\#1}}$	360	C3D7_C40_#1
208	IIOF2_C40_#2	259	A6_C40_#2	310	V_{CC}_CL	361	C3D6_C40_#1
209	IIOF3_C40_#2	260	A5_C40_#2	311	V_{SS}_CL	362	C3D5_C40_#1
210	$\overline{\text{NMI\_C40\_\#2}}$	261	A4_C40_#2	312	$\overline{\text{CE0\_C40\_\#1}}$	363	C3D4_C40_#1
211	V_{CC}_DR	262	V_{CC}_DR	313	$\overline{\text{RDY0\_C40\_\#1}}$	364	C3D3_C40_#1
212	V_{SS}_CL	263	A3_C40_#2	314	$\overline{\text{DE\_C40\_\#1}}$	365	C3D2_C40_#1
213	TCLK0_C40_#2	264	A2_C40_#2	315	TDI_C40_#1	366	C3D1_C40_#1
214	TCLK1_C40_#2	265	A1_C40_#2	316	PAGE1_C40_#1	367	C3D0_C40_#1
215	H3_C40_#2	266	A0_C40_#2	317	R/$\overline{\text{W}}$1_C40_#1	368	V_{CC}_DR
216	H1_C40_#2	267	D31_C40_#1	318	$\overline{\text{STRB1\_C40\_\#1}}$	369	V_{SS}_CL
217	V_{SS}_CL	268	D30_C40_#1	319	STAT0_C40_#1	370	C2D7_C40_#1
218	$\overline{\text{IACK\_C40\_\#2}}$	269	D29_C40_#1	320	STAT1_C40_#1	371	C2D6_C40_#1
219	V_{CC}_DR	270	D28_C40_#1	321	V_{SS}_CL	372	C2D5_C40_#1
220	V_{CC}_DR	271	D27_C40_#1	322	STAT2_C40_#1	373	C2D4_C40_#1
221	V_{CC}_DR	272	D26_C40_#1	323	STAT3_C40_#1	374	C2D3_C40_#1
222	V_{SS}_CL	273	V_{CC}_DR	324	PAGE0_C40_#1	375	C2D2_C40_#1
223	V_{SS}_DR	274	D25_C40_#1	325	R/$\overline{\text{W}}$0_C40_#1	376	C2D1_C40_#1
224	V_{CC}_DR	275	D24_C40_#1	326	$\overline{\text{STRB0\_C40\_\#1}}$	377	C2D0_C40_#1
225	V_{CC}_DR	276	D23_C40_#1	327	$\overline{\text{AE\_C40\_\#1}}$	378	V_{SS}_DR
226	V_{CC}_CL	277	D22_C40_#1	328	RESETLOC1_C40_#1	379	V_{CC}_DR
227	V_{SS}_CL	278	D21_C40_#1	329	V_{CC}_DR	380	$\overline{\text{CRDY3\_C40\_\#1}}$
228	V_{SS}_DR	279	D20_C40_#1	330	RESETLOC0_C40_#1	381	$\overline{\text{CSTRB3\_C40\_\#1}}$
229	V_{SS}_CL	280	D19_C40_#1	331	$\overline{\text{CRDY5\_C40\_\#1}}$	382	$\overline{\text{CACK3\_C40\_\#1}}$
230	V_{CC}_DR	281	D18_C40_#1	332	$\overline{\text{CSTRB5\_C40\_\#1}}$	383	$\overline{\text{CREQ3\_C40\_\#1}}$
231	A30_C40_#2	282	D17_C40_#1	333	$\overline{\text{CACK5\_C40\_\#1}}$	384	V_{CC}_CL
232	A29_C40_#2	283	D16_C40_#1	334	$\overline{\text{CREQ5\_C40\_\#1}}$	385	V_{SS}_CL
233	A28_C40_#2	284	V_{SS}_CL	335	$\overline{\text{CRDY4\_C40\_\#1}}$	386	$\overline{\text{CRDY2\_C40\_\#1}}$
234	V_{CC}_DR	285	V_{SS}_CL	336	$\overline{\text{CSTRB4\_C40\_\#1}}$	387	$\overline{\text{CSTRB2\_C40\_\#1}}$
235	A27_C40_#2	286	V_{CC}_DR	337	$\overline{\text{CACK4\_C40\_\#1}}$	388	$\overline{\text{CACK2\_C40\_\#1}}$
236	A26_C40_#2	287	V_{SS}_DR	338	$\overline{\text{CREQ4\_C40\_\#1}}$	389	$\overline{\text{CREQ2\_C40\_\#1}}$
237	A25_C40_#2	288	D15_C40_#1	339	V_{SS}_DR	390	V_{CC}_DR
238	A24_C40_#2	289	D14_C40_#1	340	V_{CC}_DR	391	$\overline{\text{CRDY1\_C40\_\#1}}$
239	A23_C40_#2	290	D13_C40_#1	341	C5D7_C40_#1	392	$\overline{\text{CSTRB1\_C40\_\#1}}$
240	A22_C40_#2	291	D12_C40_#1	342	C5D6_C40_#1	393	$\overline{\text{CACK1\_C40\_\#1}}$
241	A21_C40_#2	292	D11_C40_#1	343	C5D5_C40_#1	394	$\overline{\text{CREQ1\_C40\_\#1}}$
242	A20_C40_#2	293	D10_C40_#1	344	C5D4_C40_#1	395	V_{SS}_DR
243	A19_C40_#2	294	D9_C40_#1	345	C5D3_C40_#1	396	V_{SS}_CL
244	A18_C40_#2	295	D8_C40_#1	346	C5D2_C40_#1	397	V_{SS}_DR
245	A17_C40_#2	296	D7_C40_#1	347	C5D1_C40_#1	398	V_{CC}_DR
246	V_{CC}_DR	297	D6_C40_#1	348	C5D0_C40_#1	399	C1D7_C40_#1
247	V_{SS}_CL	298	D5_C40_#1	349	V_{CC}_DR	400	C1D6_C40_#1
248	V_{SS}_DR	299	V_{CC}_DR	350	C4D7_C40_#1	401	C1D5_C40_#1
249	A16_C40_#2	300	D4_C40_#1	351	C4D6_C40_#1	402	C1D4_C40_#1
250	A15_C40_#2	301	D3_C40_#1	352	C4D5_C40_#1	403	C1D3_C40_#1
251	A14_C40_#2	302	D2_C40_#1	353	C4D4_C40_#1	404	C1D2_C40_#1
252	A13_C40_#2	303	D1_C40_#1	354	C4D3_C40_#1	405	C1D1_C40_#1
253	A12_C40_#2	304	D0_C40_#1	355	C4D2_C40_#1	406	C1D0_C40_#1
254	A11_C40_#2	305	$\overline{\text{CE1\_C40\_\#1}}$	356	C4D1_C40_#1	407	V_{CC}_DR
255	A10_C40_#2	306	$\overline{\text{RDY1\_C40\_\#1}}$	357	C4D0_C40_#1	408	V_{SS}_DR

functional block diagram

The following terminals have 10-kΩ pullup resistors added within the module:

- $\overline{\text{CREQx\_C40\_\#1}}$, $\overline{\text{CACKx\_C40\_\#1}}$, $\overline{\text{CSTRBx\_C40\_\#1}}$, $\overline{\text{CRDYx\_C40\_\#1}}$, where x = 1, 2, 3, 4, or 5
- $\overline{\text{CREQy\_C40\_\#2}}$, $\overline{\text{CACKy\_C40\_\#2}}$, $\overline{\text{CSTRBy\_C40\_\#2}}$, $\overline{\text{CRDYy\_C40\_\#2}}$, where y = 0, 1, 2, 4, or 5
- $\overline{\text{LCE1\_C40\_\#1}}$, $\overline{\text{LCE2\_C40\_\#2}}$ (internal connections)

A total of 18 decoupling capacitors have been connected within the module.

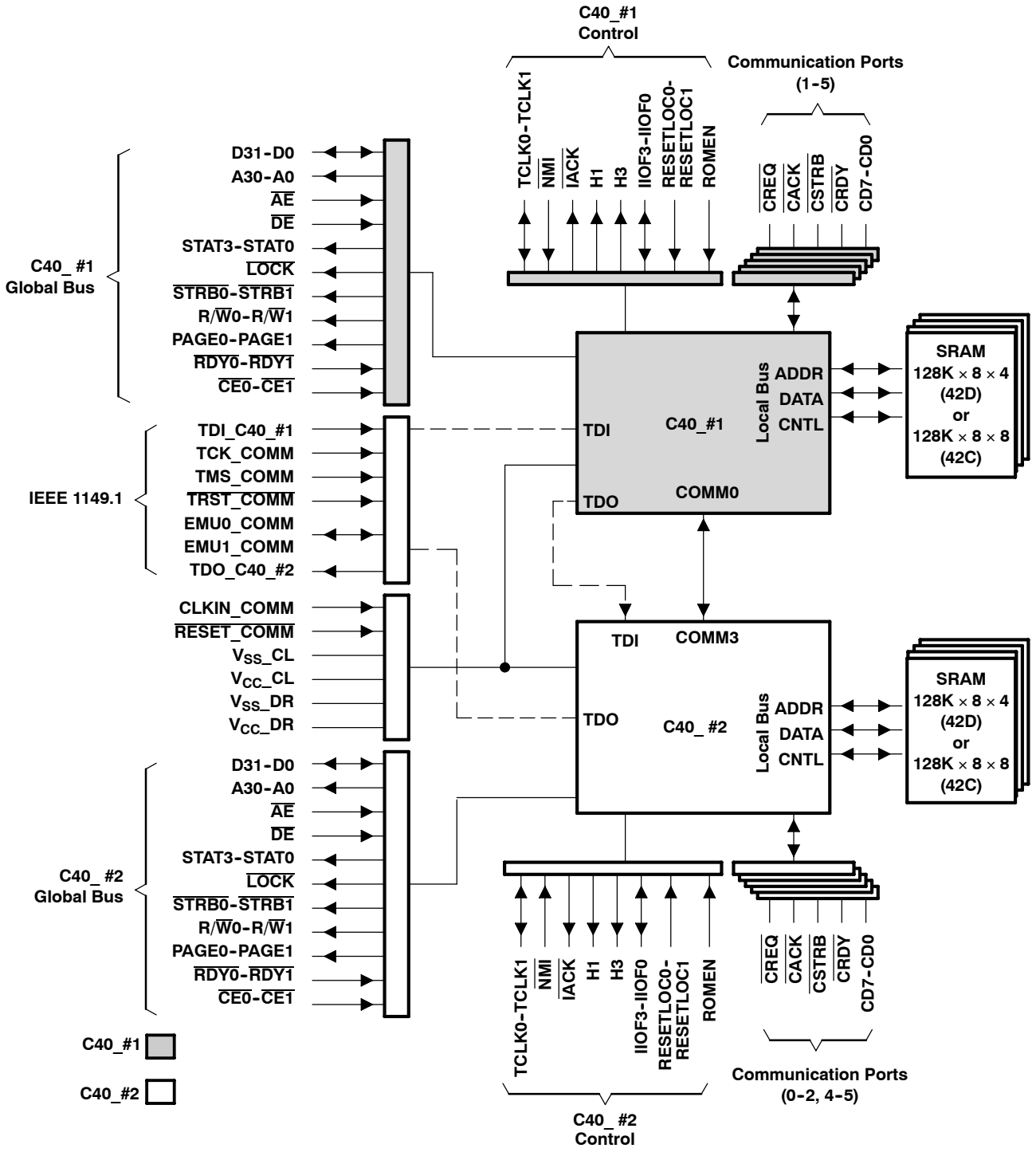
Between clean power and ground, the following capacitors have been connected:

- Two 0.1-μF capacitors
- Two 0.01-μF capacitors

Between dirty power and ground, the following capacitors have been connected:

- Twelve 0.1-μF capacitors
- Two 0.01-μF capacitors

functional block diagram (continued)



operational overview

Treatment of the detailed operation of the C40 device is not included in the scope of this document. See the *TMS320C4x User's Guide* (literature number SPRU063) for a detailed description of this DSP. See Figure 1 and Figure 2 for the memory map.

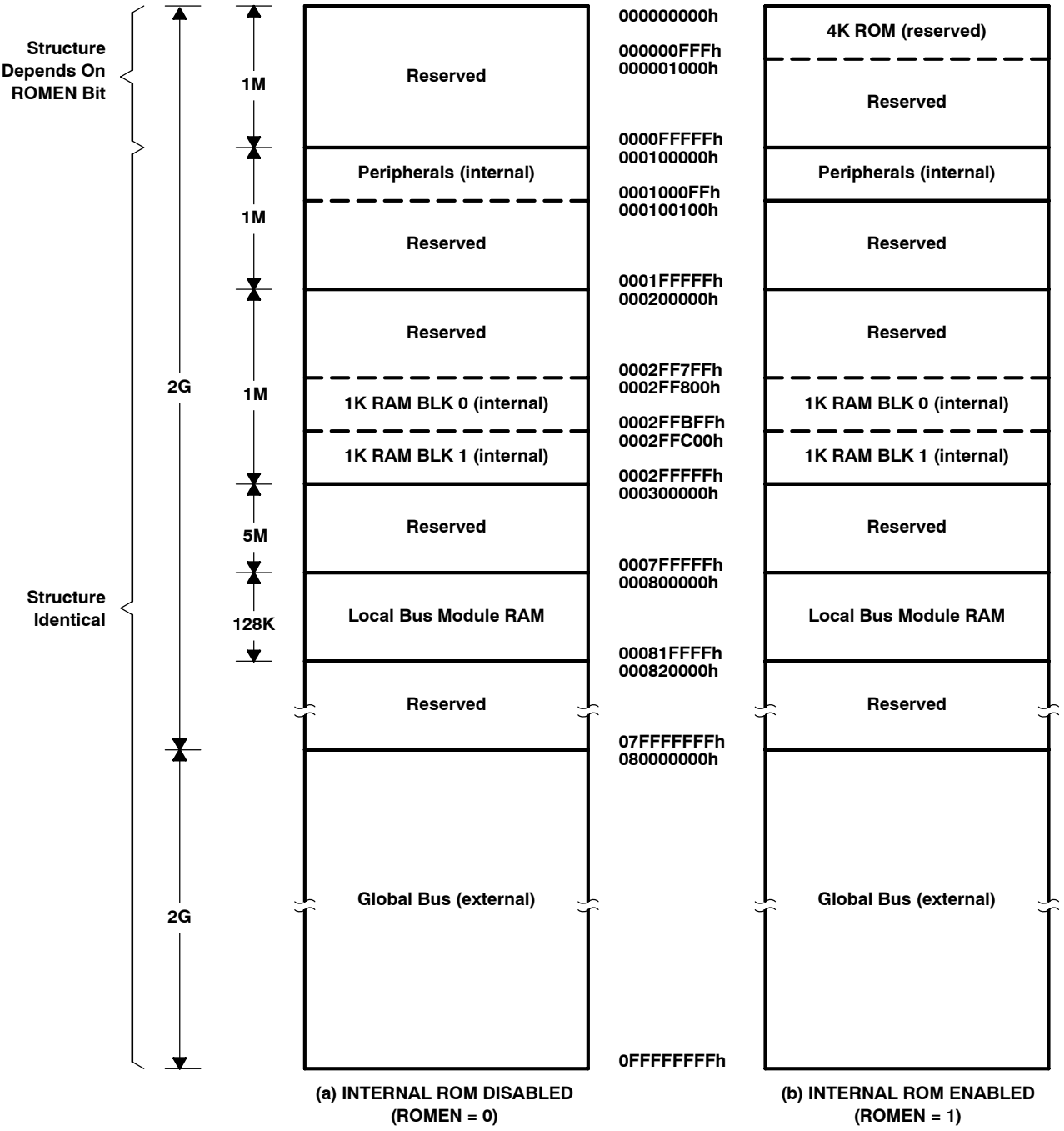


Figure 1. Memory Map for Each C40 Within the Multichip Module (42D)

operational overview (continued)

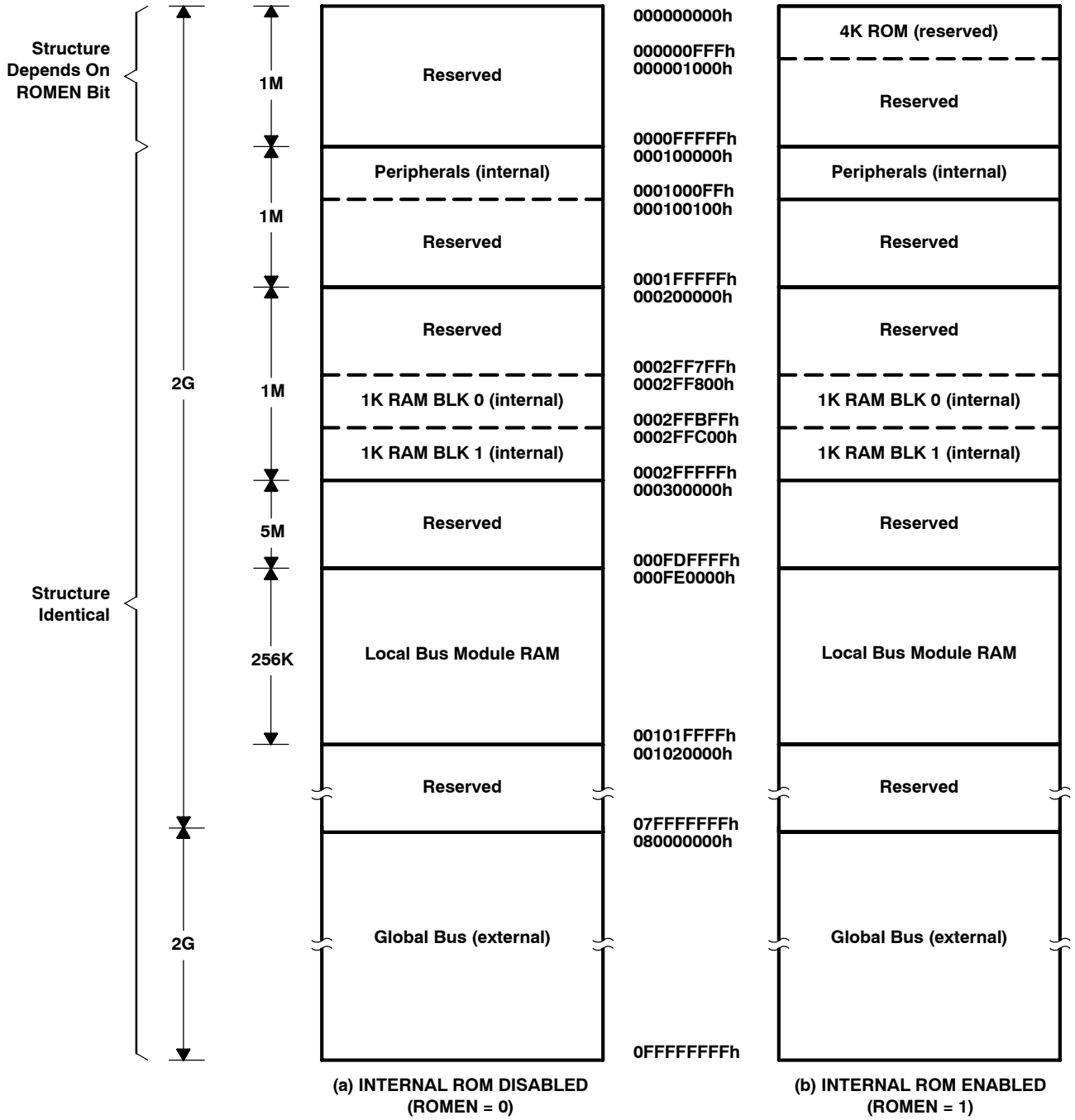


Figure 2. Memory Map for Each C40 Within the Multichip Module (42C)

application note

For all MCM42x product manufactured prior to August 1, 2001 (i.e., date codes older than 0131), users should reference the application note on page 10 of SGKS001B (July 1997 - Revised February 2000) for proper memory function.

The following application note applies to MCM42x product manufactured after August 1, 2001 (i.e., date codes newer than 0131). Changes to this application note from the previous data sheet revision impact the MCM42C only. Note: The information for the MCM42D below remains unchanged regardless of the date code.

For all MCM42C, the location of the local memory is different from that of the MCM42D. In addition, for proper use of the memory, it is necessary to understand how the memory is controlled.

For product manufactured with date codes newer than 0131, the following applies to the MCM42C only: The entire memory array is controlled by $\overline{\text{LSTRB0}}$. The value to be loaded to the STRB ACTIVE area (bits 28–24) should be 11110 (binary). This will require a code change for customers who developed code intended for use with MCM42C devices manufactured with date codes older than 0131.

For the MCM42D, $\overline{\text{LSTRB0}}$ controls the entire 128K. The default value loaded into the STRB ACTIVE area of the LMICR after reset is sufficient to control the memory. The default value is 11110, and tells the C40 that the entire local memory is controlled by $\overline{\text{LSTRB0}}$.

This subject is discussed in depth in Chapter 9 of the *1996 TMS320C4x User's Guide* (literature number SPRU063). In particular, section 9.3 discusses the proper use of the memory interface control registers.

reference documentation and data sheet scope

The SMJ320MCM42 is qualified to MIL-PRF-38535. Electrical continuity of the module is ensured through the use of IEEE-1149.1-compatible boundary-scan testing and functional checkout of the local SRAM space.

KGD refers to TI known-good-die strategy. TI KGDs are fully tested over the military temperature range per MIL-PRF-38535 QML. Electrical tests ensure compliance of the C40 KGD components to the SMJ320C40 data sheet (literature number SGUS017) over the operating temperature range. Module timings are virtually unchanged from the SMJ320C40 data sheet timings. An SMJ320C40 data sheet is provided for customer reference only and does not imply MCM compliance to published timings.

For a description of the C40 operation and application information, see the *TMS320C4x User's Guide* (literature number SPRU063).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 0.3 V to 7 V
Voltage range on any terminal . . . . . – 0.3 V to 7 V
Output voltage range, V_O . . . . . – 0.3 V to 7 V
Operating free-air temperature range (commercial [L version]), T_A . . . . . 0°C to 70°C
(military [M version]), T_A . . . . . – 55°C to 125°C
Junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage	42-33		4.5	5.5	V
		42-40		4.75	5.25	
V_{IH}	High-level input voltage	CLKIN_COMM		2.6	V_{CC} + 0.3	V
		$\overline{\text{CSTRBx}}$, $\overline{\text{CRDYx}}$, $\overline{\text{CREQx}}$, $\overline{\text{CACKx}}$		2.2	V_{CC} + 0.3	
		All others		2	V_{CC} + 0.3	
V_{IL}	Low-level input voltage			– 0.3	0.8	V
I_{OH}	High-level output current				– 300	μA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature range		L version	0	70	°C
			M version	– 55	125	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4	3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX		0.3	0.6	V
I_{CC}	Supply current	42D	V_{CC} = MAX		0.7	1.1	A
		42C			0.8	1.5	
I_Z	3-state current		V_I = V_{SS} to V_{CC}	– 20		20	μA
I_I	Input current		V_I = V_{SS} to V_{CC}	– 10		10	μA
I_{I2}	Input current, COMM signal (see Note 3)		V_I = V_{SS} to V_{CC}	– 20		20	μA
I_{IP}	Input current, internal pullup (see Note 4)		V_I = V_{SS} to V_{CC}	– 400		30	μA
I_{IP2}	Input current, dual internal pullup (see Note 5)		V_I = V_{SS} to V_{CC}	– 800		60	μA
I_{IC}	Input current, CLKIN_COMM		V_I = V_{SS} to V_{CC}	– 60		60	μA

† For conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 2. Electrical characteristics are calculated algebraically from the SMJ320C40 data sheet limits.
3. Includes signals EMU0_COMM, EMU1_COMM, and $\overline{\text{RESET\_COMM}}$
4. Applies to TDI_C40_#1
5. Includes signals TCK_COMM, TMS_COMM, and $\overline{\text{TRST\_COMM}}$

capacitance

Capacitance of a C40 die is specified by design to be 15 pF maximum for both inputs and outputs. Module networks add up to 5 pF. Characterization of die or substance capacitance is performed after any design change. Power measurements taken for a C40 die are made with an additional 80-pF load capacitance. Refer to the SMJ320C40 data sheet (literature number SGUS017) for the test load circuit.

operational timings and module testing

Texas Instruments processing assures that operation is verified to published data sheet specifications on the C40 in die form. All voltage, timing, speed, and temperature specifications are met before any die is placed into a multichip module. For this reason, all C40 voltage and timing parameters at the module level need not be verified.

Characterization of the 42 substrate shows that the module performs as an equivalent system of discretely packaged C40 devices. This performance is assured through a full-frequency functional checkout of the module that verifies selected worst-case timings. An additional propagation delay is introduced by the substrate. This value is assured by design to be less than 1 ns, but it is not tested. See the SMJ320C40 data sheet (literature number SGUS017) for a complete listing of timing diagrams and limits.

module test capability (future compatibility)

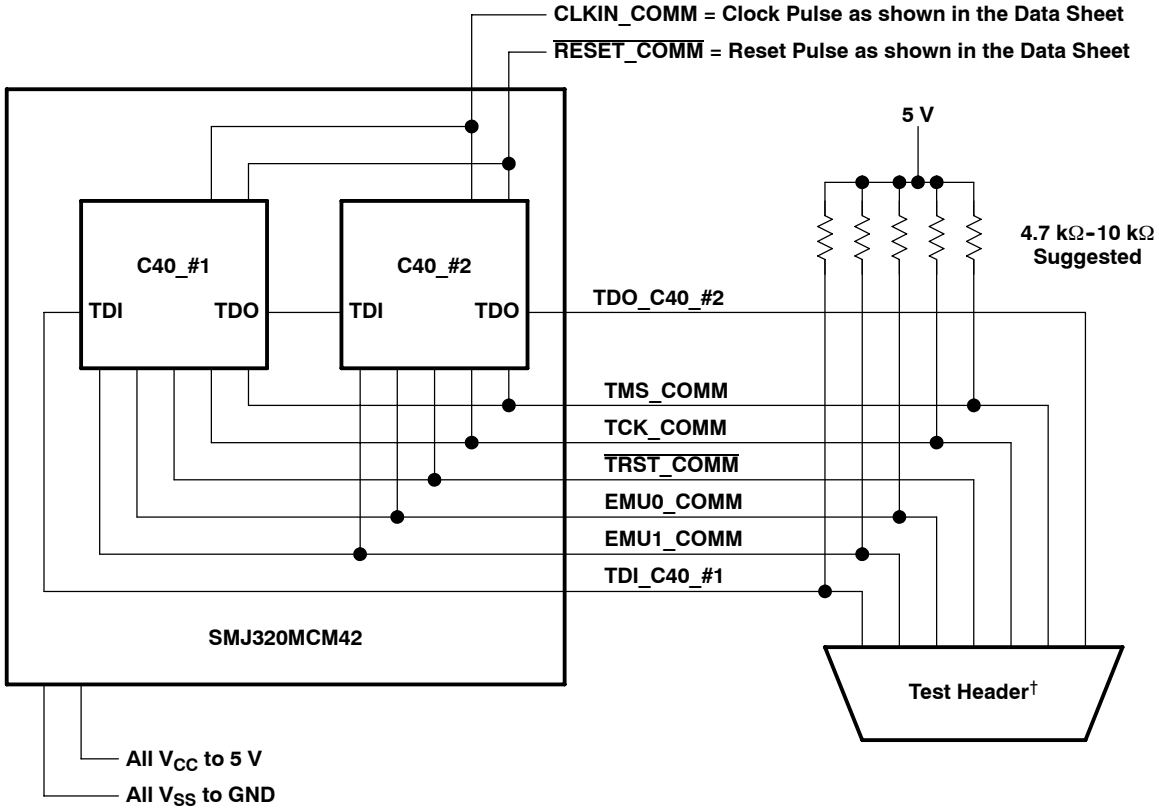
The C40 supports the IEEE-1149.1 testability standard, and the test access port (TAP) is brought out to the module footprint. TDI is connected to C40_#1, TDO of C40_#1 is connected to TDI of C40_#2, and TDO of C40_#2 is brought out to the TAP. TCK_COMM, TMS_COMM, and $\overline{\text{TRST\_COMM}}$ are routed to both C40s in the module. This configuration allows users to test the module using third-party JTAG testability tools or other boundary-scan control software. Proper software configuration allows users to debug or launch code on the module by way of the C40 emulator and extended development system (XDS™) pod. Both of these tools are used as part of outgoing module testing.

The 42 supports third-party JTAG diagnostic families of products for verification and debug of boundary-scan circuits, boards, and systems. Further information on JTAG testability tools is available through any TI sales representative or authorized TI distributor.

XDS is a trademark of Texas Instruments Incorporated.

module test circuit

Figure 3 illustrates the basic circuits for the 42. See the *TMS320C4x User's Guide* (literature number SPRU063) for more detailed information.



† The test header normally consists of the XDS510™ for the C40 emulation or ASSET hardware for interconnect testing.

Figure 3. Sample Test Circuit

XDS510 is a trademark of Texas Instruments Incorporated.

thermal analysis

Thermal conduction of components in the SMJ320MCM42 is dependent on thermal resistance of the material under each die as well as die area thermally connected to the heat-dissipating medium. Since these properties vary with layout and die size, C40 and SRAM components should be considered separately. Table 2 lists primary parameters required for thermal analysis of the module. T_J, the maximum junction temperature, is not to be exceeded for the C40s or the SRAM die.

Table 2. Thermal Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
T_J	Maximum allowable junction temperature under operating condition			150	°C
P_{MCM}	Module power dissipation		3.5	5.8	W
T_{JC_pkg}†	Average thermal impedance (junction to case) for the package		2.1		°C/W
T_{JA}	Thermal impedance (junction to ambient air, 0 cfm) of package		20.5		°C/W
T_{SOL}	Maximum solder temperature (10 s duration)			260	°C

† T_{JC} package data was taken under the following conditions: two C40s dissipating 1.05 W each and eight SRAMs dissipating 0.175 W each.

power estimation

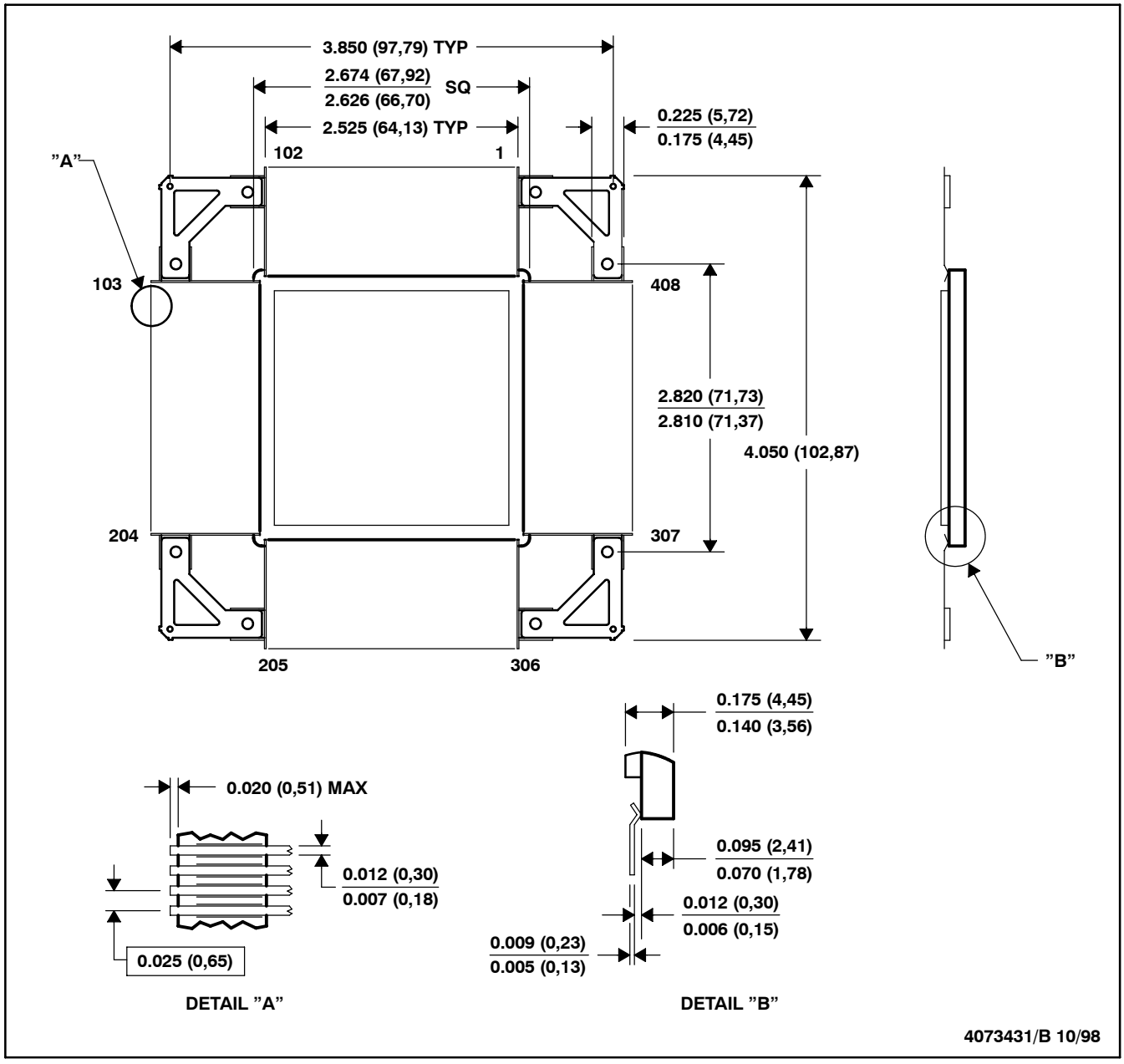
During the operation verification, the power requirements of the SMJ320MCM42 are characterized over the operating free-air temperature range. See the application report *Calculation of TMS320C40 Power Dissipation* (literature number SPRA032) as reference for power estimation of the C40 components.

Typical power dissipation is measured with both C40s executing a 64-point fast Fourier transform (FFT) algorithm. Input and output data arrays reside in module SRAM, and output data is written out to the global-address space. The global databus is loaded with 80-pF test loads, and both local and global writes are configured for zero-wait-state memory. Under typical conditions of 25°C, 5-V V_{CC}, and 40-MHz CLKIN frequency, the power dissipation is measured to be 3.5 W.

Maximum power dissipation is measured under worst-case conditions. The global databus is loaded with 80-pF test loads, and simultaneous zero-wait-state writes are performed to both local and global buses. Under worst-case environment conditions of – 55°C, 5.25-V V_{CC}, and 40-MHz CLKIN frequency, the power dissipation is determined to be 5.9 W. The algorithm executed during these tests consists of parallel writes of alternating 0xAAs and 0x55s to both local SRAM and global-address spaces. This algorithm is not considered to be a practical use of the C40's resources; therefore, the associated power measurement must be considered absolute maximum only.

MECHANICAL DATA

HFN (S-CQFP-F408) **CERAMIC QUAD FLATPACK WITH TIE-BAR**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9678901QXC	OBSOLETE	CFP	HFN	408		TBD	Call TI	Call TI	-55 to 125	5962-9678901QX C SMJ320MCM42DHF NM40	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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