micross components

VRAM
SMJ44C251B
MT42C4256

256K X 4 VRAM
256K x 4 DRAM
with 512K x 4 SAM

AVAILABLE AS MILITARY SPECIFICATIONS
- SMD 5962-89497
- MIL-STD-883

FEATURES
- Class B High-Reliability Processing
- DRAM: 262144 Words × 4 Bits
  SAM: 512 Words × 4 Bits
- Single 5-V Power Supply (±10% Tolerance)
- Dual Port Accessibility–Simultaneous and Asynchronous Access From the DRAM and SAM Ports
- Bidirectional-Data-Transfer Function Between the DRAM and the Serial-Data Register
- 4 × 4 Block-Write Feature for Fast Area Fill Operations; As Many as Four Memory Address Locations Written per Cycle From an On-Chip Color Register
- Write-Per-Bit Feature for Selective Write to Each RAM I/O; Two Write-Per-Bit Modes to Simplify System Design
- Enhanced Page-Mode Operation for Faster Access
- CAS-Before-RAS (CBR) and Hidden Refresh Modes
- All Inputs/Outputs and Clocks Are TTL Compatible
- Long Refresh Period: Every 8 ms (Max)
- Up to 33-MHz Uninterrupted Serial-Data Streams
- 3-State Serial I/Os Allow Easy Multiplexing of Video-Data Streams
- 512 Selectable Serial-Register Starting
- Split Serial-Data Register for Simplified Real-Time Register Reload

OPTIONS — MARKING

- **Timing**

100ns, 30ns/27ns	-10
120ns, 35ns/35ns	-12

- **Package(s)**

	MT Prefix	SMJ Prefix
Ceramic SOJ	DCJ	---
Ceramic DIP (400 mil)	C	JDM
Ceramic LCC	EC	HMM
Ceramic ZIP	CZ	SVM
Ceramic LCC	---	HJM
Ceramic Flat Pack	F	---

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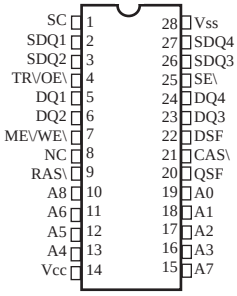
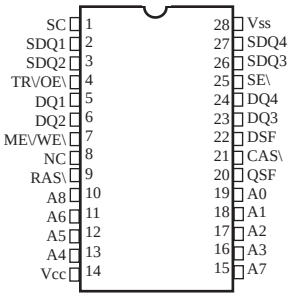
PIN ASSIGNMENT
(Top View)

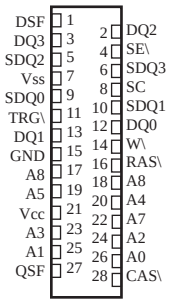
28-Pin DIP (C)
(400 MIL)



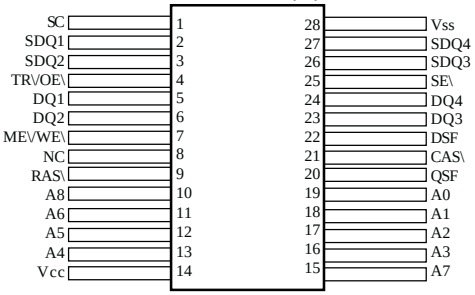
28-Pin SOJ (DCJ)
28-Pin LCC (EC)



28-Pin ZIP (CZ)



28-Pin FP (F)



PIN NAME (SMJ)	PIN NAME (MT)	DESCRIPTION
A0 - A8	A0 - A8	Address Inputs
CAS\	CAS\	Column Enable
DQ0 - DQ3	DQ1 - DQ4	DRAM Data In-Out/Write-Mask Bit
SE\	SE\	Serial Enable
RAS\	RAS\	Row Enable
SC	SC	Serial Data Clock
SDQ0 - SDQ3	SDQ1 - SDQ4	Serial Data In-Out
TRG\	TR\ /OE\	Transfer Register/Q Output Enable
W\	ME\ /WE\	Write-Mask Select/Write Enable
DSF	DSF	Special Function Select
QSF	QSF	Split-Register Activity Status
Vcc	Vcc	5V Supply
Vss	Vss	Ground
GND	NC	Ground (Important: Not Connected to internal Vss, Pin should be left open or tied to ground.

DESCRIPTION

The SMJ44C251B/MT42C4256 multiport video RAM is a high-speed, dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262144 words of 4 bits each interfaced to a serial-data register or serial-access memory (SAM) organized as 512 words of 4 bits each. The SMJ44C251B/MT42C4256 supports three types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer operations, the SMJ44C251B/MT42C4256 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

During a transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4-bit serial-data register can be loaded from the memory row (transfer read), or the contents of the 512 × 4-bit serial-data register can be written to the memory row (transfer write).

The SMJ44C251B/MT42C4256 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's 4 × 4 block-write mode. The block-write mode allows four bits of data (present in an on-chip color-data register) to be written to any combination of four adjacent column-address locations. As many as 16 bits of data can be written to memory during each CAS cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking any combination of the four input/outputs on any write cycle. The persistent write-per-bit feature uses a mask register that, once loaded, can be used on subsequent write cycles. The mask register eliminates having to provide mask data on every mask-write cycle.

The SMJ44C251B/MT42C4256 offers a split-register transfer read (DRAM to SAM) feature for the serial tester (SAM port). This feature enables real-time register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register reload (for example, reloads done during CRT retrace periods), the single-register mode of operation is retained to simplify design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

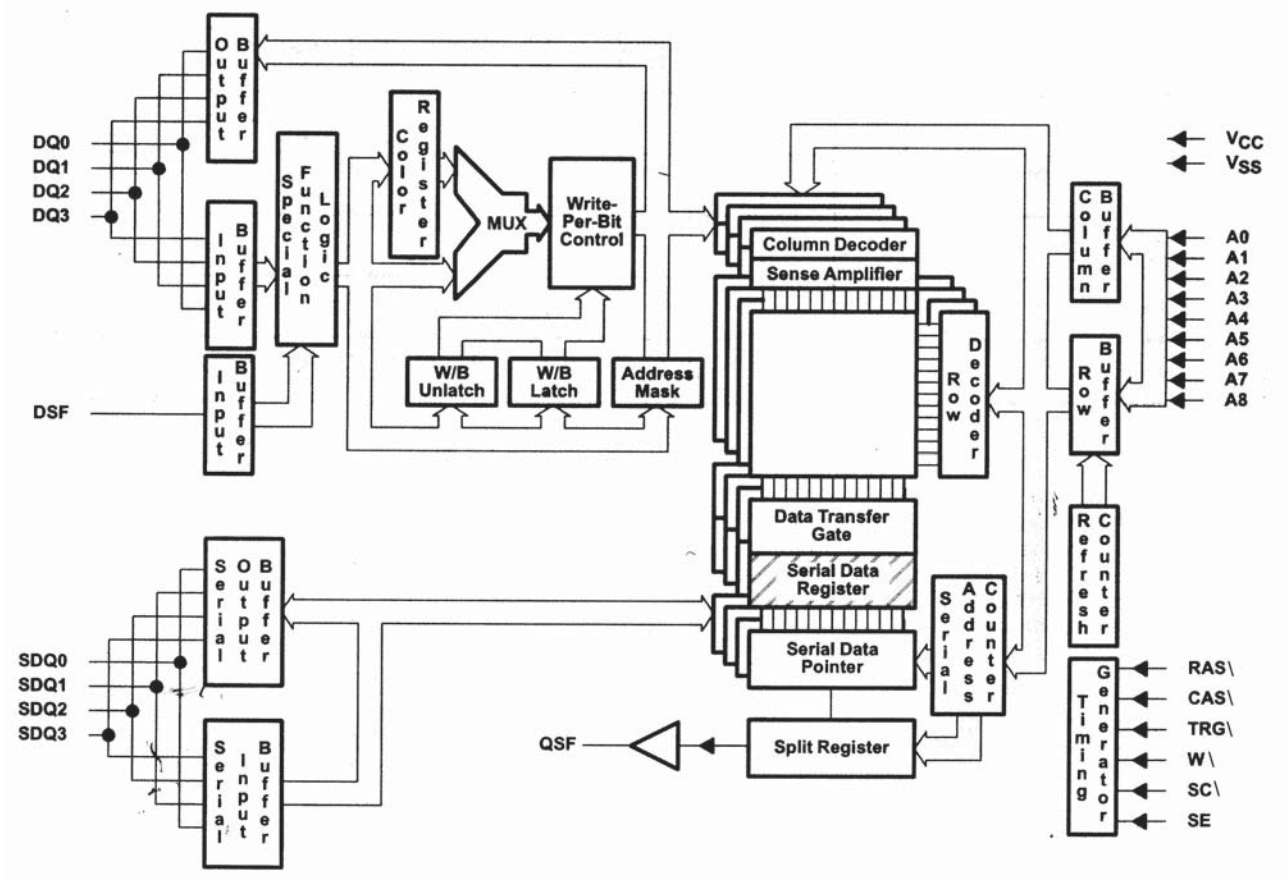
The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During the split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active at any given time in the split-register mode.

All inputs, outputs, and clock signals on the SMJ44C251B/MT42C4256 are compatible with Series 54 TTL devices. All address lines and data-in lines are latched on-chip to simplify system design. All data-out lines are unlatched to allow greater system flexibility.

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup, row-address hold, and address multiplex is eliminated, and a memory cycle time reduction of up to 3× can be achieved, compared to minimum RAS cycle times. The maximum number of columns that can be accessed is determined by the maximum RAS low time and page-mode cycle time used. The SMJ44C251B/MT42C4256 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single RAS-low period using relatively conservative page-mode cycle times.

The SMJ44C251B/MT42C4256 employs state-of-the-art technology for very high performance combined with improved reliability.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

FUNCTION	RAS\ FALL					CAS\ FALL	ADDRESS		DQ0 - DQ3		TYPE[3]
	CAS\	TRG\	W\[1]	DSF	SE\	DSF	RAS\	CAS\	RAS\	CAS\[2] W\	
CBR Refresh	L	X	X	X	X	X	X	X	X	X	R
Register-to-memory transfer (transfer write)	H	L	L	X	L	X	Row Addr	Tap Point	X	X	T
Alternate transfer write (independent of SE\)	H	L	L	H	X	X	Row Addr	Tap Point	X	X	T
Serial-write-mode enable (pseudo-transfer write)	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	T
Memory-to-register transfer (transfer read)	H	L	H	L	X	X	Row Addr	Tap Point	X	X	T
Split-register-transfer read (must reload tap)	H	L	H	H	X	X	Row Addr	Tap Point	X	X	T
Load and use write mask, Write data to DRAM	H	L	L	L	X	L	Row Addr	Col Addr	DQ Mask	Valid Data	R
Load and use write mask, Block write to DRAM	H	H	L	L	X	H	Row Addr	Blk Addr A2-A8	DQ Mask	Col Mask	R
Persistent write-per-bit, Write data to DRAM	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	R
Persistent write-per-bit, Block write to DRAM	H	H	L	H	X	H	Row Addr	Blk Addr A2-A8	X	Col Mask	R
Normal DRAM read/write (nonmasked)	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	R
Block write to DRAM (nonmasked)	H	H	H	L	X	H	Row Addr	Blk Addr A2-A8	X	Col Mask	R
Load write mask	H	H	H	H	X	L	Refresh Addr	X	X	DQ Mask	R
Load color register	H	H	H	H	X	H	Refresh Addr	X	X	Color Data	R

NOTES:

1. In persistent write-per-bit function, W\ must be high during the refresh cycle.
2. DQ0 - DQ3 are latched on the later of W\ or CAS\ falling edge. Col Mask = H: Write to address/column location enabled. DQ Mask = H: Write to I/O enabled.
3. R = random access operation, T = transfer operation.

LEGEND

H = HIGH
L = LOW
X = Don't Care

DETAILED SIGNAL DESCRIPTION VS. OPERATIONAL MODE

PIN	DRAM	TRANSFER	SAM
A0 - A8	Row, column address	Row, tap address	
CAS\	Column enable, output enable	Tap-address strobe	
DQi	DRAM data I/O, write mask bits		
DSF	Block-write enable Persistent write-per-bit enable Color-register load enable	Split-register enable Alternative write-transfer enable	
RAS\	Row enable	Row enable	
SE\		Serial-in mode enable	Serial enable
SC			Serial clock
SDQ			Serial-data I/O
TRG\	Q output enable	Transfer enable	
W\	Write enable, write-per-bit select	Transfer-write enable	
QSF			Split register Active status
NC/GND	Make no external connection or tie to system Vss		
Vcc	5V supply (typical)		
Vss	Device ground		

OPERATION

Depending on the type of operation chosen, the signals of the SMJ44C251B/MT42C4256 perform different functions. The "Detailed Signal Description vs. Operational Mode" table summarizes the signal descriptions and the operational modes they control.

The SMJ44C251B/MT42C4256 has three kinds of operations: random-access operations typical of a DRAM, transfer operations from memory arrays to the SAM, and serial-access operations through the SAM port. The signals used to control these operations are described here, followed by discussions of the operations themselves.

ADDRESS (A0–A8)

For DRAM operation, 18 address bits are required to decode one of the 262144 storage cell locations. Nine row- address bits are set up on A0–A8 and latched onto the chip on the falling edge of RAS\. Nine column-address bits are set up on A0–A8 and latched onto the chip on the falling edge of CAS\. All addresses must be stable on or before the falling edges of RAS\ and CAS\.

During the transfer operation, the states of A0–A8 are latched on the falling edge of RAS\ to select one of the 512 rows where the transfer occurs. To select one of 512 tap points (starting positions) for the serial-data input or output, the appropriate 9-bit column address (A0–A8) must be valid when CAS\ falls.

ROW-ADDRESS STROBE (RAS\)

RAS\ is similar to a chip enable because all DRAM cycles and transfer cycles are initiated by the falling edge of RAS\. RAS\ is a control input that latches the states of row address, W\, TRG\, SE\, CAS\, and DSF onto the chip to invoke DRAM and transfer functions.

COLUMN-ADDRESS STROBE (CAS\)

CAS\ is a control input that latches the states of column address and DSF to control DRAM and transfer functions. When CAS\ is brought low during a transfer cycle, it latches the new tap point for the serial-data input or output. CAS\ also acts as an output enable for the DRAM outputs DQ0–DQ3.

OUTPUT ENABLE/TRANSFER SELECT (TRG\)

TRG\ selects either DRAM or transfer operation as RAS\ falls. For DRAM operation, TRG\ must be held high as RAS\ falls. During DRAM operation, TRG\ functions as an output enable for the DRAM outputs DQ0–DQ3. For transfer operation, TRG\ must be brought low before RAS\ falls.

WRITE-MASK SELECT, WRITE ENABLE (W\)

In DRAM operation, W\ enables data to be written to the DRAM. W\ is also used to select the DRAM write-per-bit mode. Holding W\ low on the falling edge of RAS\ invokes the write-per-bit operation. The SMJ44C251B/MT42C4256 supports both the normal write-per-bit mode and the persistent write-per-bit mode.

CONTINUED

WRITE-MASK SELECT, WRITE ENABLE (W\) (continued)

For transfer operation, W\ selects either a read-transfer operation (DRAM to SAM) or a write-transfer operation (SAM to DRAM). During a transfer cycle, if W is high when RAS\ falls, a read transfer occurs; if W is low, a write transfer occurs.

SPECIAL FUNCTION SELECT (DSF)

DSF is latched on the falling edge of RAS\ or CAS\, similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- Persistent write-per-bit
- Block write
- Split-register transfer read
- Mask-register load for the persistent write-per-bit mode
- Color-register load for the block-write mode

DRAM DATA I/O, WRITE-MASK DATA (DQ0–DQ3)

DRAM data is written via DQ terminals during a write or read-modify-write cycle. In an early-write cycle, W\ is brought low prior to CAS\ and the data is strobed in by CAS\ with data setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, W\ is brought low after CAS\ and the data is strobed in by W\ with data setup and hold times referenced to this signal.

The 3-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as CAS\ and TRG\ are held high. Data does not appear at the outputs until both CAS\ and TRG\ are brought low. Once the outputs are valid, they remain valid while CAS\ and TRG\ are low. CAS\ or TRG\ going high returns the outputs to the high-impedance state. In a register-transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

The write-per-bit mask is latched into the device via the random DQ terminals by the falling edge of RAS\. This mask selects which of the four random I/Os are written.

SERIAL DATA I/O (SDQ0–SDQ3)

Serial inputs and serial outputs share common I/O terminals. Serial-input or serial-output mode is determined by the previous transfer cycle. If the previous transfer cycle was a read transfer, the data register is in serial-output mode. While in serial-output mode, data in SAM is accessed from the least significant bit to the most significant bit. The data registers operate modulo 512; so after bit 511 is accessed, the next bits to be accessed are 00, 01, 02, etc. If the previous transfer cycle was either a write transfer or a pseudo transfer, the data register is in serial-input mode and signal data can be input to the register.

SERIAL CLOCK (SC)

Serial data is accessed in or out of the data register on the rising edge of SC. The SMJ44C251B/MT42C4256 is designed to work with a wide range of clock-duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC clock operating frequency.

SERIAL ENABLE (SE\)

During serial-access operations SE\ is used as an enable/disable for SDQ in both the input and output modes. If SE\ is held as RAS\ falls during a write-transfer cycle, a pseudo-transfer write occurs. There is no actual transfer, but the data register switches from the output mode to the input mode.

NO CONNECT/GROUND (NC/GND)

NC/GND is reserved for the manufacturer's test operation. It is an input and should be tied to system ground or left floating for proper device operation.

SPECIAL FUNCTION OUTPUT (QSF)

During split-register operation the QSF output indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 256 bits of SAM. When QSF is high, the serial-address pointer is accessing the higher (most significant) 256 bits of SAM. QSF changes state upon crossing the boundary between the two SAM halves in the split-register mode.

During normal transfer operations QSF changes state upon completing a transfer cycle. This state is determined by the tap point being loaded during the transfer cycle.

POWER UP

To achieve proper device operation, an initial pause of 200ms is required after power-up, followed by a minimum of eight RAS\ cycles or eight CBR cycles, a memory-to-register transfer cycle, and two SC cycles.

RANDOM-ACCESS-OPERATION FUNCTIONS

FUNCTION	RAS\ FALL					CAS\ FALL	ADDRESS		DQ0 - DQ3	
	CAS\	TRG\	W\[1]	DSF	SE\	DSF	RAS\	CAS\	RAS\	CAS\[2] W\
CBR Refresh	L	X	X	X	X	X	X	X	X	X
Load and use write mask, Write data to DRAM	H	H	L	L	X	L	Row Addr	Col Addr	DQ Mask	Valid Data
Load and use write mask, Block write to DRAM	H	H	L	L	X	H	Row Addr	Blk Addr A2-A8	DQ Mask	Col Mask
Persistent write-per-bit, Write data to DRAM	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data
Persistent write-per-bit, Block write to DRAM	H	H	L	H	X	H	Row Addr	Blk Addr A2-A8	X	Col Mask
Normal DRAM read/write (nonmasked)	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data
Block write to DRAM (nonmasked)	H	H	H	L	X	H	Row Addr	Blk Addr A2-A8	X	Col Mask
Load write mask	H	H	H	H	X	L	Refresh Addr	X	X	DQ Mask
Load color register	H	H	H	H	X	H	Refresh Addr	X	X	Color Data

NOTES:
1. In persistent write-per-bit function, W must be high during the refresh cycle.
2. DQ0–DQ3 are latched on the later of W or CAS falling edge. Col Mask = H: Write to address/column location enabled. DQ Mask = H: Write to I/O enabled

LEGEND:
H = High
L = Low
X = Don't care

RANDOM-ACCESS OPERATION

The random-access operation functions are summarized in the "Random-Access-Operation Function" table and described in the following sections.

ENHANCED PAGE-MODE

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row address setup-and-hold and address multiplex. The maximum RAS\ low time and the CAS\ page cycle time used determine the number of columns that can be accessed.

Unlike conventional page-mode operation, the enhanced page mode allows the SMJ44C251B/MT42C4256 to operate at a
higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when CAS\ transitions low. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of CAS\. In this case, data can be obtained after $t_{a(C)}$ max (access time from CAS low), if $t_{a(CA)}$ max (access time from column address) has been satisfied.

REFRESH

There are three types of refresh available on the SMJ44C251B/MT42C4256: RAS\-only refresh, CBR refresh, and hidden refresh.

RAS\-ONLY REFRESH

A refresh operation must be performed to each row at least once every 8 ms to retain data. Unless CAS\ is applied, the output buffers are in the high-impedance state, so the RAS\-only refresh sequence avoids any output during refresh. Externally generated addresses must be supplied during RAS-only refresh. Strobing each of the 512 row addresses with RAS causes

(continued)

RAS\-ONLY REFRESH (continued)

all bits in each row to be refreshed. CAS\ can remain high (inactive) for this refresh sequence to conserve power.

CAS\-BEFORE-RAS\ (CBR) REFRESH

CBR refresh is accomplished by bringing CAS\ low earlier than RAS\. The external row address is ignored and the refresh row address is generated internally when using CBR refresh. Other cycles can be performed in between CBR cycles without disturbing the internal address generation.

HIDDEN REFRESH

A hidden refresh is accomplished by holding CAS\ low in the DRAM-read cycle and cycling RAS\. The output data of the DRAM-read cycle remains valid while the refresh is being carried out. Like the CBR refresh, the refreshed row addresses are generated internally during the hidden refresh.

WRITE-PER-BIT

The write-per-bit feature allows masking of any combination of the four DQs on any write cycle (see Figure 1). The write-per-bit operation is invoked only when W\ is held low on the falling edge of RAS\. If W\ is held high on the falling edge of RAS\, write-per-bit is not enabled and the write operation is performed to all four DQs. The SMJ44C251B/MT42C4256 offers two write-per-bit modes: the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

NONPERSISTENT WRITE-PER-BIT

When DSF is low on the falling edge of RAS\, the write mask is reloaded. A 4-bit code (the write-per-bit mask) is input to the device via the random DQ terminals and latched on the falling edge of RAS\. The write-per-bit mask selects which of the four random I/Os are written and which are not. After RAS\ has latched the on-chip write-per-bit mask, input data is driven onto the DQ terminals and is latched on the later falling edge of CAS\ or W\. When a data low is strobed into a particular I/O on the falling edge of RAS\, data is not written to that I/O. When a data high is strobed into a particular I/O on the falling edge of RAS\, data is written to that I/O.

PERSISTENT WRITE-PER-BIT

When DSF is high on the falling edge of RAS\, the write-per-bit mask is not reloaded: it retains the value stored during the last write-per-bit mask reload. This mode of operation is known as persistent write-per-bit because the write-per-bit mask is persistent over an arbitrary number of write cycles. The write-per-bit mask reload can be done during the nonpersistent write-per-bit cycle or by the mask-register-load cycle.

BLOCK WRITE

The block-write mode allows data (present in an on-chip color register) to be written into four consecutive column-address locations. The 4-bit color register is loaded by the color-register-load cycle. Both write-per-bit modes can be applied in the block-write cycle. The block-write mode also offers the 4 × 4 column-mask capability.

LOAD COLOR REGISTER

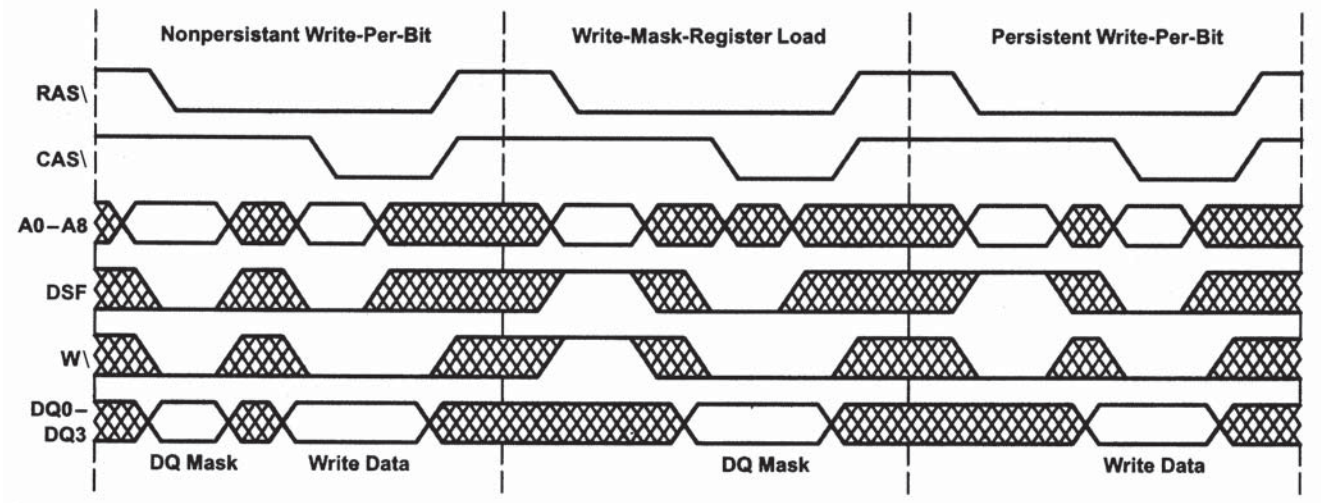
The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of RAS\ and CAS\. A 4-bit code is input to the color register via the random I/O terminals and latched on the later of the falling edge of CAS\ or W\. After the color register is loaded, it retains data until power is lost or until another load-color-register cycle is executed.

BLOCK WRITE CYCLE

After the color register is loaded, the block-write cycle can begin as a normal DRAM write cycle with DSF held high on the falling edge of CAS\ (see Figures 2, 3, and 4). When the block-write cycle is invoked, each data bit in the 4-bit color register is written to selected bits of the four adjacent columns of the corresponding random I/O.

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the falling edge of CAS\. The two least significant addresses (A0–A1) are replaced by four DQ bits (DQ0–DQ3), which are also latched on the later of the falling edge of CAS\ or W\. These four bits are used as a column mask, and they indicate which of the four column-address locations addressed by A2–A8 are written with the contents of the color register during the block-write cycle. DQ0 enables a write to column-address A1 = 0 (low), A0 = 0 (low); DQ1 enables a write to column-address A1 = 0 (low), A0 = 1 (high); DQ2 enables a write to column-address A1 = 1 (high), A0 = 0 (low); DQ3 enables a write to column-address A1 = 1 (high), A0 = 1 (high). A high logic level enables a write, and a low logic level disables the write. A maximum of 16 bits (4 × 4) can be written to memory during each CAS\ cycle in the block-write mode.

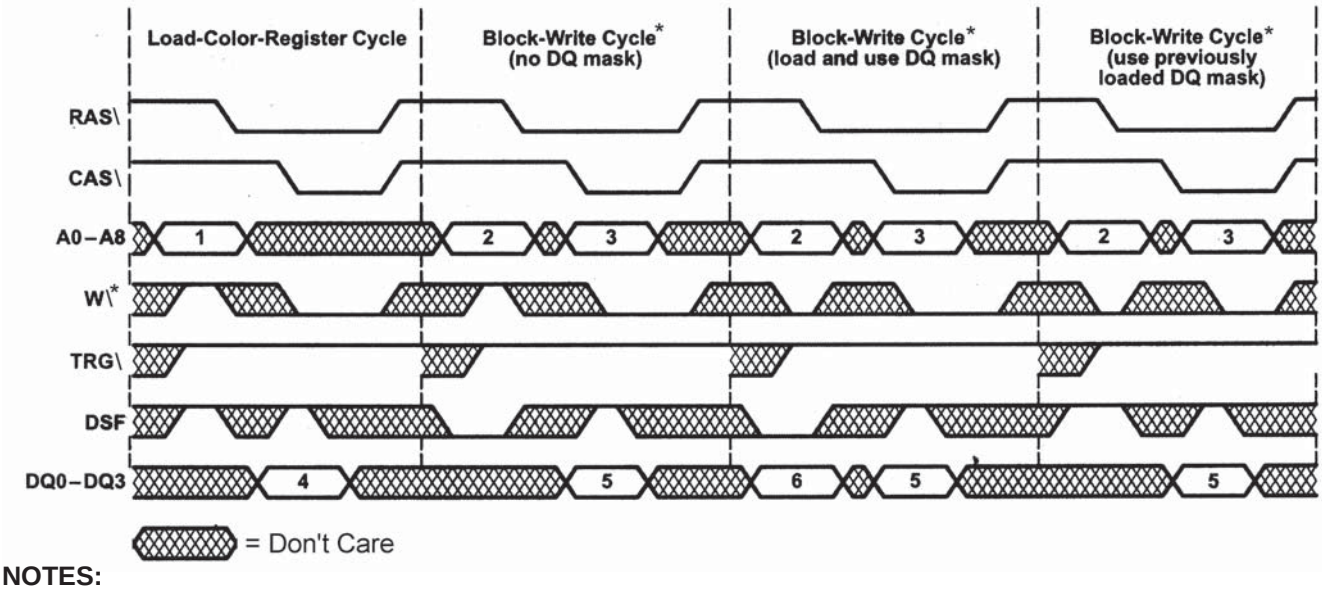
FIGURE 1: EXAMPLE OF WRITE-PER-BIT OPERATIONS



DQ Mask = H: Write to I/O enable

= L: Write to I/O disable

FIGURE 2: EXAMPLE BLOCK-WRITE DIAGRAM OPERATIONS



NOTES:

* W\ must be low during the block-write cycle.

DQ0–DQ3 are latched on the later of W\ or CAS\ falling edge except in block 6 (see legend).

LEGEND:

1. Refresh address
2. Row address
3. Block address (A2 –A8)
4. Color-register data
5. Column-mask data
6. DQ-mask data. DQ0–DQ3 are latched on the falling edge of RAS\.

FIGURE 3: BLOCK-WRITE CIRCUIT BLOCK DIAGRAM

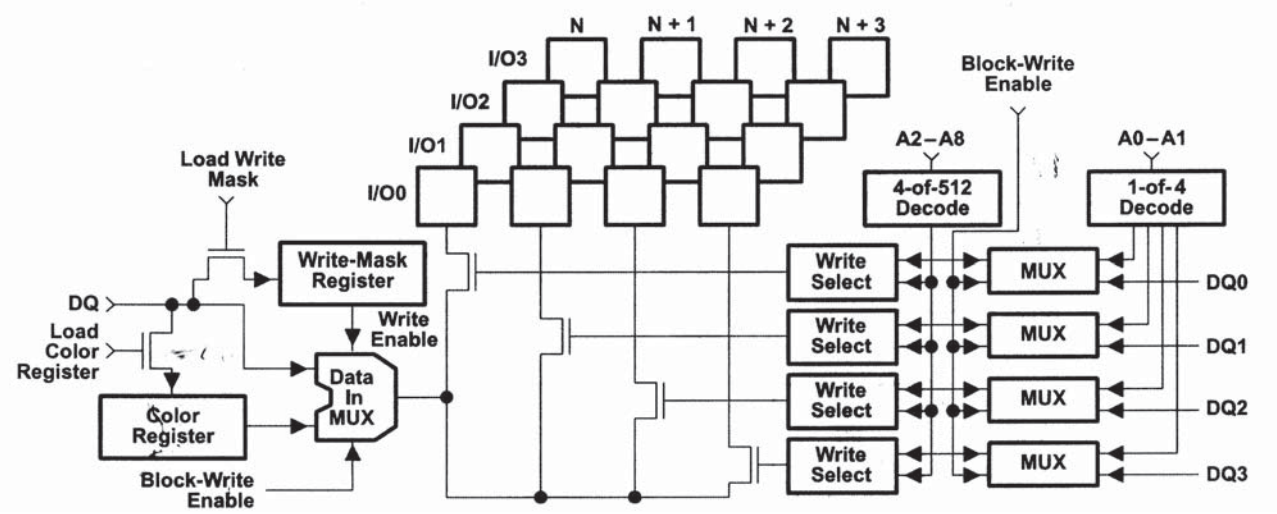


FIGURE 4: EXAMPLE OF BLOCK WRITE OPERATION WITH DQ MASK AND ADDRESS MASK

	DQ MASK	COLUMN MASK	COLOR REGISTER DATA
DQ0	1	0	0
DQ1	1	1	0
DQ2	0	1	1
DQ3	1	1	1

Block Write

	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4
DQ0	Masked	0	0	0
DQ1	Masked	0	0	0
DQ2	Masked	Masked	Masked	Masked
DQ3	Masked	1	1	1

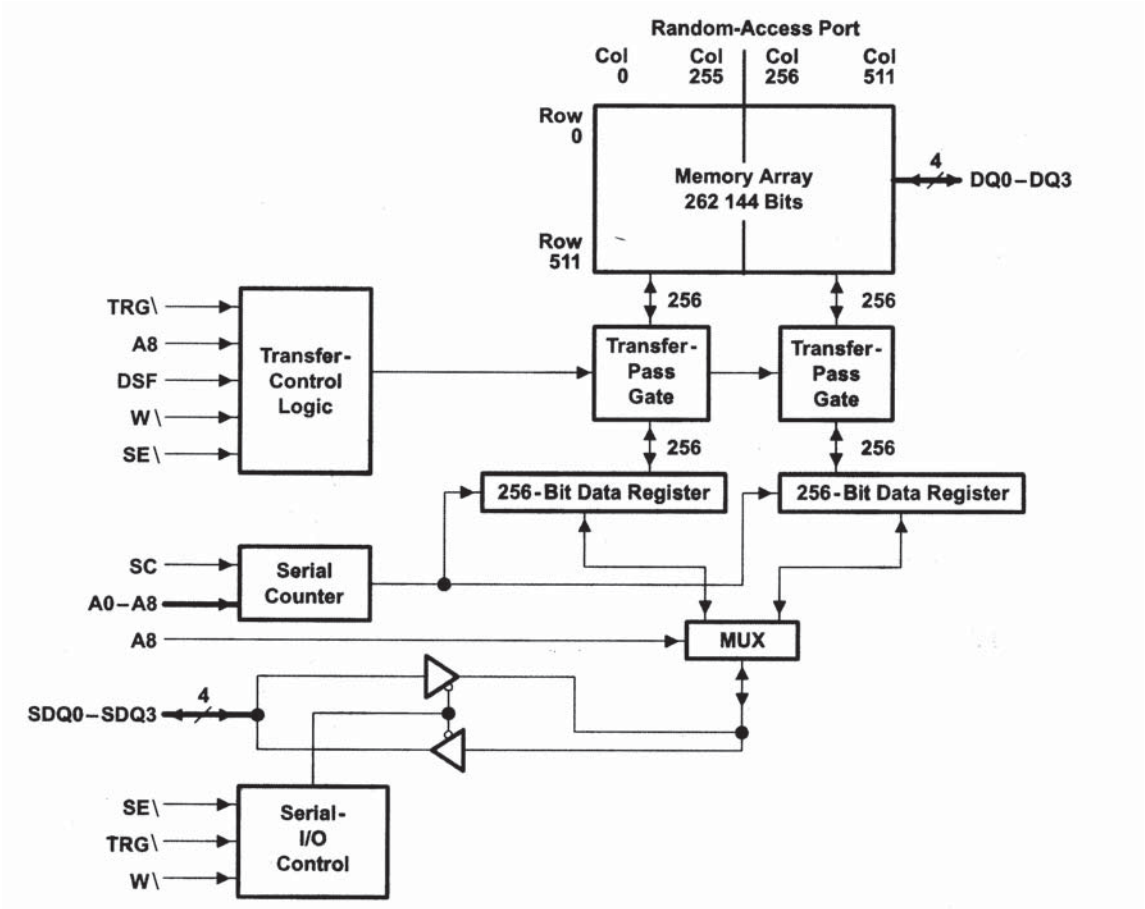
TRANSFER OPERATION

Transfer operations between the memory arrays (DRAM) and the data registers (SAM) are invoked by bringing TRG\ low before RAS\ falls. The states of W\, SE\, and DSF, which are also latched on the falling edge of RAS\, determine which transfer operation is invoked. Figure 5 shows an overview of data flow between the random and the serial interfaces.

As shown in the "Transfer-Operation Functions" table, the SMJ44C251B/MT42C4256 supports five basic modes of transfer operation:

- Register-to-memory transfer (normal write transfer, SAM to DRAM)
- Alternate-write transfer (independent of the state of SE\)
- Memory-to-register transfer (pseudo-transfer write). Switches serial port from serial-out mode to serial-in mode. No actual data transfer takes place between the DRAM and the SAM.
- Memory-to-register transfer (normal-read transfer, transfer entire contents of DRAM row to SAM)
- Split-register-read transfer (divides the SAM into a low and a high half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

FIGURE 5: BLOCK DIAGRAM SHOWING ONE RANDOM AND ONE SERIAL-I/O INTERFACE



TRANSFER-OPERATION FUNCTIONS

FUNCTION	RAS\ FALL					CAS\ FALL	ADDRESS		DQ0 - DQ3	
	CAS\	TRG\	W\	DSF	SE\	DSF	RAS\	CAS\	RAS\	CAS\ W\
Register-to-memory transfer (normal write transfer)	H	L	L	X	L	X	Row Addr	Tap Point	X	X
Alternate-write transfer (independent of SE\)	H	L	L	H	X	X	Row Addr	Tap Point	X	X
Serial-write-mode enable (pseudo-transfer write)	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X
Memory-to-register transfer (normal read transfer)	H	L	H	L	X	X	Row Addr	Tap Point	X	X
Split-register-read transfer (must reload tap)	H	L	H	H	X	X	Row Addr	Tap Point	X	X

LEGEND:
H = High
L = Low
X = Don't Care

WRITE TRANSFER

All write-transfer cycles (except the pseudo write transfer) transfer the entire content of SAM to the selected row in the DRAM. To invoke a write-transfer cycle, W\ must be low when RAS\ falls. There are three possible write-transfer operations: normal-write transfer, alternate-write transfer, and pseudo-write transfer. All write-transfer cycles switch the serial port to the serial-in mode.

NORMAL-WRITE TRANSFER (SAM-to-DRAM transfer)

A normal-write transfer cycle loads the contents of the serial-data register to a selected row in the memory array. TRG\, W\, and SE\ are brought low and latched at the falling edge of RAS\. Nine row-address bits (A0–A8) are also latched at the falling edge of RAS\ to select one of the 512 rows available as the destination of the data transfer. The nine column-address bits (A0–A8) are latched at the falling edge of CAS\ to select one of the 512 tap points in SAM that are available for the next serial input.

During a write-transfer operation before RAS\ falls, the serial-input operation must be suspended after a minimum delay of $t_{d(SCRL)}$ but can be resumed after a minimum delay of $t_{d(RHSC)}$ after RAS goes high (see Figure 6).

ALTERNATE-WRITE TRANSFER (refer to Figure 30)

When DSF is brought high and latched at the falling edge of RAS\ in the normal-write-transfer cycle, the alternate-write transfer occurs.

PSEUDO-WRITE TRANSFER (write-mode control) (refer to Figure 28)

To invoke the pseudo-write transfer (write-mode control cycle), SE\ is brought high and latched at the falling edge of RAS\. The pseudo-write transfer does not actually invoke any data transfer but switches the mode of the serial port from the serial-out (read) mode to the serial-in (write) mode.

Before serial data can be clocked into the serial port via the SDQ terminals and the SC input, the SDQ terminals must be switched into input mode. Because the transfer does not occur during the pseudo-transfer write, the row address (A0–A8) is in the don't care state and the column address (A0–A8), which is latched on the falling edge of CAS\, selects one of the 512 tap points in the SAM that are available for the next serial input.

READ TRANSFER (DRAM-to-SAM transfer) (refer to Figure 7)

During a read-transfer cycle, data from the selected row in DRAM is transferred to SAM. There are two read-transfer operations: normal-read transfer and split-register-read transfer.

NORMAL-READ TRANSFER (refer to Figure 7)

The normal-read-transfer operation loads data from a selected row in DRAM into SAM. TRG\ is brought low and latched at the falling edge of RAS\. Nine row-address bits (A0–A8) are also latched at the falling edge of RAS\ to select one of the 512 rows available for transfer. The nine column-

(continued)

NORMAL-READ TRANSFER
(refer to Figure 7)

address bits (A0– A8) are latched at the falling edge of CAS\ to select one of the SAM's 512 available tap points where the serial data is read out.

A normal-read transfer can be performed in three ways: early-load read transfer, real-time or midline-load read transfer, and late-load read transfer. Each of these offers the flexibility of controlling the TRG\ trailing edge in the read-transfer cycle (see Figure 7).

FIGURE 6: NORMAL-WRITE-TRANSFER-CYCLE TIMING

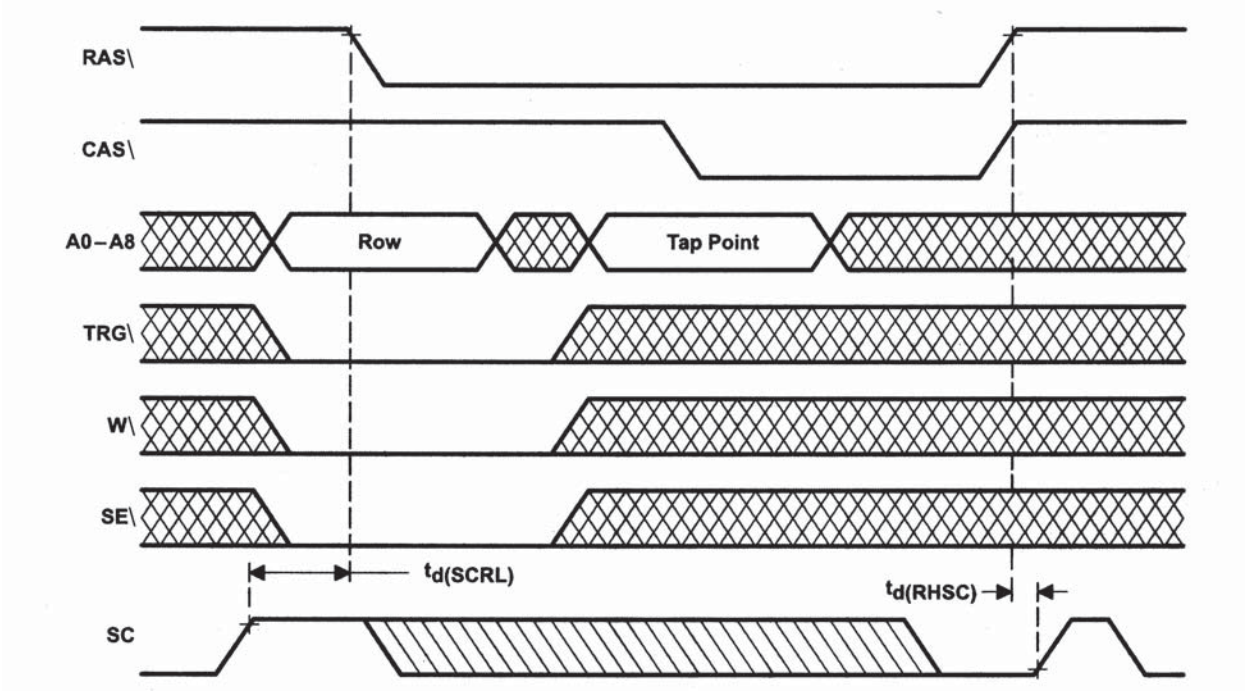
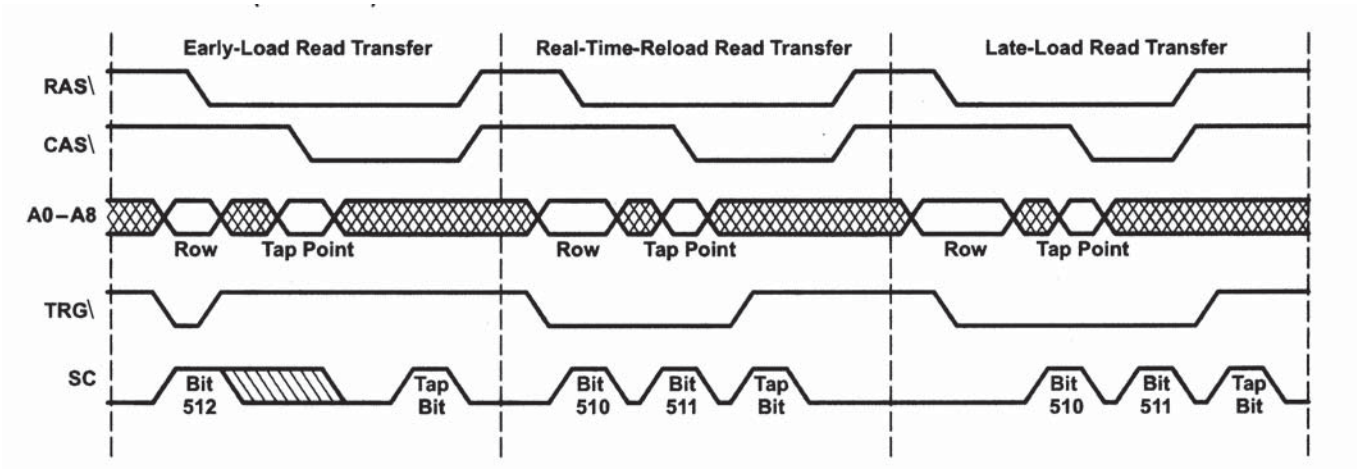


FIGURE 7: NORMAL-READ-TRANSFER TIMINGS



SPLIT-REGISTER-READ TRANSFER

In split-register-read-transfer operation, the serial-data register is split into halves. The low half contains bits 0–255, and the high half contains 256–511. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

To invoke a split-register read-transfer cycle, DSF is brought high, TRG\ is brought low, and both are latched at the falling edge of RAS\. Nine row-address bits (A0–A8) are also latched at the falling edge of RAS\ to select one of the 512 rows available for the transfer. The nine column-address bits (A0–A8) are latched at the falling edge of CAS\, where address bits A0 –A7 select one of the 255 tap points in the specified half of SAM and address bit A8 selects which half is to be transferred. If A8 is a logic low, the low half is transferred. If A8 is a logic high, the high half is transferred. SAM locations 255 and 511 cannot be used as tap points.

A normal-read transfer must precede the split-register-read transfer to ensure proper operation. After the normal-read-transfer cycle, the first split-register read transfer can follow immediately without any minimum SC requirement. However, there is a minimum requirement of a rising edge of SC between split-register read-transfer cycles.

QSF indicates which half of the SAM is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 256 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 256 bits of the SAM. QSF changes state upon completing a normal-read-transfer cycle. The tap point loaded during the current transfer cycle determines the state of QSF. In split-register read-transfer mode, QSF changes state when a boundary between the two register halves is reached (see Figure 8 and Figure 9).

FIGURE 8: EXAMPLE OF A SPLIT-REGISTER READ-TRANSFER CYCLE AFTER A NORMAL READ-TRANSFER CYCLE

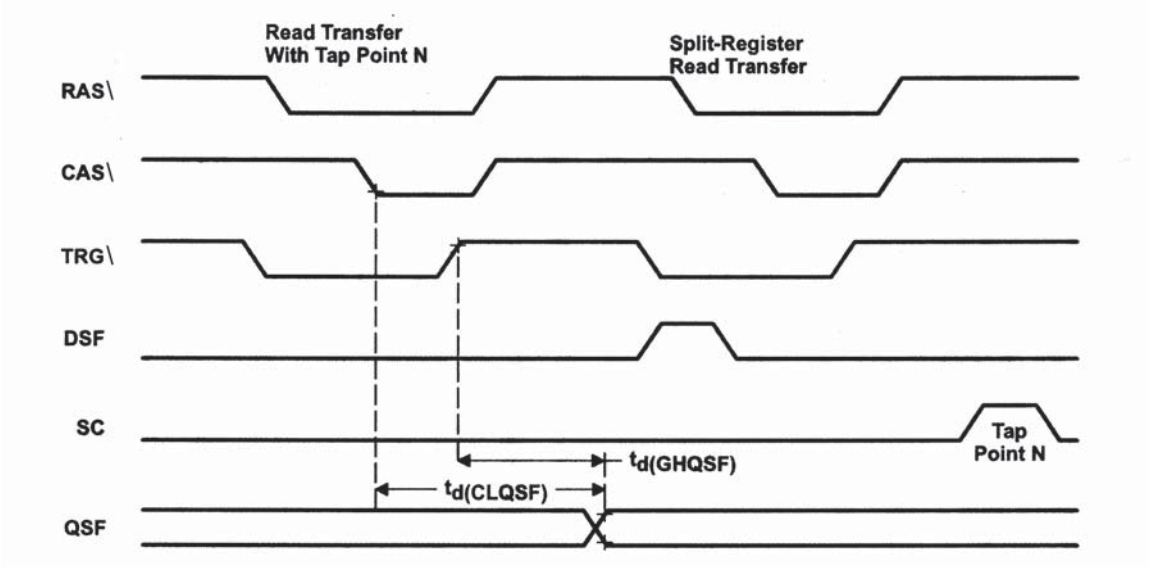
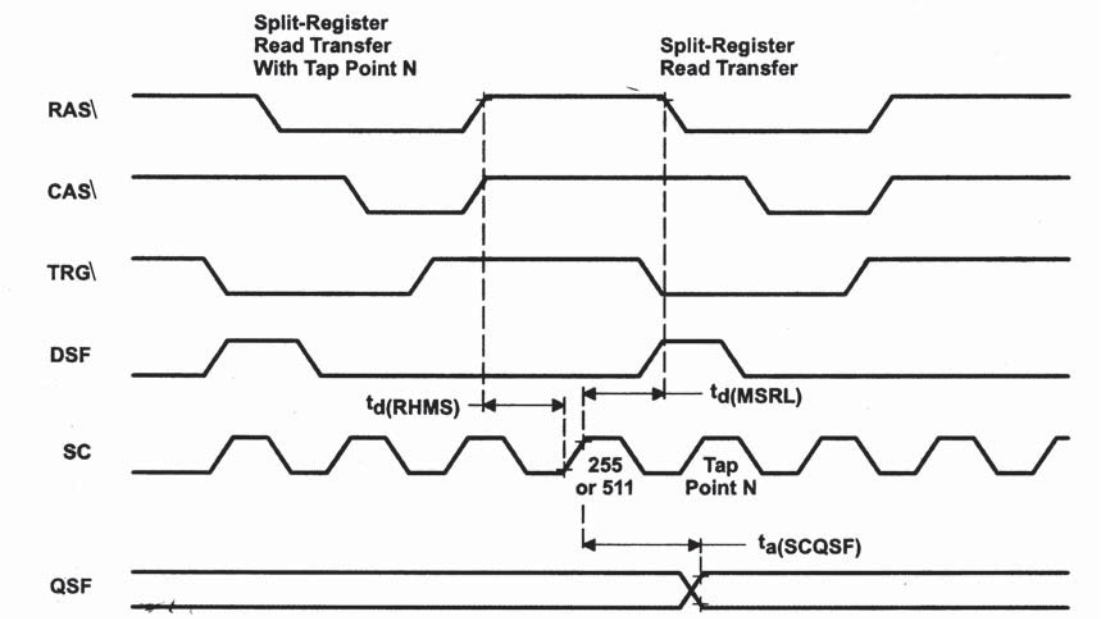


FIGURE 9: A SPLIT-REGISTER READ-TRANSFER CYCLE AFTER A SPLIT-REGISTER READ-TRANSFER CYCLE

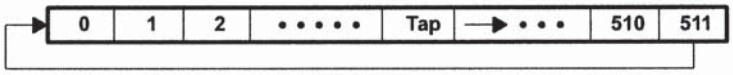


SERIAL-ACCESS OPERATION

The serial-read and serial-write operations can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. The preceding transfer operation determines the input or output state of the SAM port. If the preceding transfer operation is a read-transfer operation, the SAM port is in the output mode. If the preceding transfer operation is a write- or pseudo-write-transfer operation, the SAM port is in the input mode.

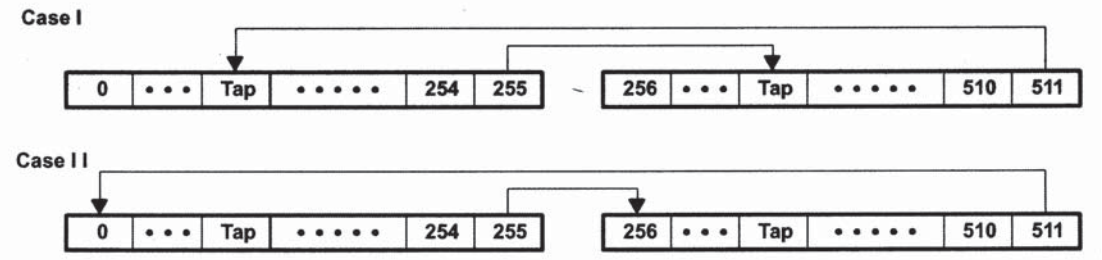
Serial data can be read out of or written into SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 511), then wrapping around to the least significant bit (bit 0) (see Figure 10).

FIGURE 10: SERIAL POINTER DIRECTION FOR SERIAL READ/WRITE



For split-register read-transfer operation, serial data can be read out from the active half of SAM by clocking SC starting at the tap point loaded by the preceding split-register-transfer cycle, then proceeding sequentially to the most significant bit of the half, bit 255 or bit 511. If there is a split-register-read transfer to the inactive half during this period, the serial pointer points next to the tap-point location loaded by that split register (see Figure 11, Case I). If there is no split-register read transfer to the inactive half during this period, the serial pointer points next to bit 256 or bit 0, respectively (see Figure 11, Case II).

FIGURE 11: SERIAL POINTER FOR SPLIT-REGISTER READ



ABSOLUTE MAXIMUM RATINGS*

Supply voltage range, V_{CC}[1].....-1V to 7V
Voltage range on any pin[1].....-1V to 7V
Short-circuit output current.....50mA
Power dissipation.....1W
Operating free-air temperature range, T_A.....-55°C to 125°C
Storage temperature range, T_{STG}.....-65°C to 150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NOTE: 1. All voltage values are with respect to Vss.

RECOMMENDED OPERATING CONDITIONS

SYM	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{SS}	Supply Voltage		0		V
V_{IH}	High-level input voltage	2.9		6.5	V
V_{IL}	Low-level input voltage**	-1		0.6	V
T_A	Operating free-air temperature	-55		125	°C
T_C	Operating case temperature			125	°C

NOTE: **The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGES AND OPERATING FREE-AIR TEMPERATURE (UNLESS OTHERWISE NOTED)

PARAMETER	SYM	CONDITIONS	MIN	MAX	UNIT
High-level output voltage	V_{OH}	I_{OH} = -5mA	2.4		V
Low-level output voltage[1]	V_{OL}	I_{OL} = 4.2mA		0.4	V
Input leakage current	I_I	V_{CC} = 5V, V_I = 0V to 5.8V, All others open		±10	µA
Output leakage current[2]	I_O	V_{CC} = 5.5V, V_O = 0V to V_{CC}		±10	µA

				-10		-12		
PARAMETER[3]	SYM	CONDITIONS	SAM PORT	MIN	MAX	MIN	MAX	UNITS
Operating current	I_{CC1}	$t_{c(rd)}$ and $t_{c(W)}$ = MIN	Standby		100		90	mA
Operating current	I_{CC1A}	$t_{c(SC)}$ = MIN	Active		110		100	mA
Standby current	I_{CC2}	All clocks = V_{CC}	Standby		15		15	mA
Standby current	I_{CC2A}	$t_{c(SC)}$ = MIN	Active		35		35	mA
RAS\-only refresh current	I_{CC3}	$t_{c(rd)}$ and $t_{c(W)}$ = MIN	Standby		100		90	mA
RAS\-only refresh current	I_{CC3A}	$t_{c(SC)}$ = MIN	Active		110		100	mA
Page-mode current	I_{CC4}	$t_{c(P)}$ = MIN	Standby		65		60	mA
Page-mode current	I_{CC4A}	$t_{c(SC)}$ = MIN	Active		70		65	mA
CAS\-before-RAS\ current	I_{CC5}	$t_{c(rd)}$ and $t_{c(W)}$ = MIN	Standby		90		80	mA
CAS\-before-RAS\ current	I_{CC5A}	$t_{c(SC)}$ = MIN	Active		110		100	mA
Data-transfer current	I_{CC6}	$t_{c(rd)}$ and $t_{c(W)}$ = MIN	Standby		100		90	mA
Data-transfer current	I_{CC6A}	$t_{c(SC)}$ = MIN	Active		110		100	mA

NOTES:

1. The SMJ44C251B may exhibit simultaneous switching noise as described in the Texas Instruments *Advanced CMOS Logic Designer's Handbook*. This phenomenon is exhibited on the DQ terminals when the SDQ terminals are switched and on the SDQ terminals when the DQ terminals are switched. This may cause V_{OL} and V_{OH} to exceed the data-book limit for a short period of time, depending upon output loading and temperature. Care should be taken to provide proper termination, decoupling, and layout of the device to minimize simultaneous switching effects.
2. SE\ is disabled for SDQ output leakage tests.
3. I_{CC} (standby) denotes that the SAM port is inactive (standby) and the DRAM port is active (except for I_{CC2}).
   I_{CCA} (active) denotes that the SAM port is active and the DRAM port is active (except for I_{CC2}).
   I_{CC} is measured with no load on DQ or SDQ.
4. For conditions shown as MIN/ MAX, use the appropriate value specified in the timing requirements.

CAPACITANCE OVER RECOMMENDED RANGES OF SUPPLY VOLTAGES AND OPERATING FREE-AIR TEMPERATURE, f = 1MHz[1]

PARAMETER	SYM	MIN	MAX	UNIT
Input capacitance, A0 - A8	$C_{i(A)}$		7	pF
Input capacitance, CAS\ and RAS\	$C_{i(RC)}$		7	pF
Output capacitance, SDQs and DQs	$C_{o(O)}$		9	pF
Output capacitance, SQSF	$C_{o(QSF)}$		9	pF

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGES AND OPERATING FREE-AIR TEMPERATURE[2]

			-10		-12		
PARAMETER	SYM/ALT. SYM	CONDITIONS[4]	MIN	MAX	MIN	MAX	UNIT
Access time from CAS\	$t_{a(C)}/t_{CAC}$	$t_{d(RLCL)}$ = MAX		25		30	ns
Access time from column address	$t_{a(CA)}/t_{CAA}$	$t_{d(RLCL)}$ = MAX		50		60	ns
Access time from CAS\ high	$t_{a(CP)}/t_{CPA}$	$t_{d(RLCL)}$ = MAX		55		65	ns
Access time from RAS\	$t_{a(R)}/t_{RAC}$	$t_{d(RLCL)}$ = MAX		100		120	ns
Access time of DQ0 - DQ3 from TRG\ low	$t_{a(G)}/t_{OEA}$			25		30	ns
Access time of SDQ0 - SDQ3 from SC high	$t_{a(SQ)}/t_{SCA}$	C_L = 30pF		30		35	ns
Access time of SDQ0 - SDQ3 from SE\ low	$t_{a(SE)}/t_{SEA}$	C_L = 30pF		20		25	ns
Disable time, random output from CAS\ high[3]	$t_{dis(CH)}/t_{OFF}$	C_L = 100pF	0	20	0	20	ns
Disable time, random output from TRG\ high[3]	$t_{dis(G)}/t_{OEZ}$	C_L = 100pF	0	20	0	20	ns
Disable time, random output from SE\ high[3]	$t_{dis(SE)}/t_{SEZ}$	C_L = 30pF	0	20	0	20	ns

NOTES:

1. Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1-MHz signal applied to the terminal under test. All other terminals are open.
2. Switching times assume C_L = 100 pF unless otherwise noted (see Figure 12).
3. $t_{dis(CH)}$, $t_{dis(G)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.
4. For conditions shown as MIN/ MAX, use the appropriate value specified in the timing requirements.

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGES AND OPERATING FREE-AIR TEMPERATURE[1]

		-10		-12		
PARAMETER	SYM/ALT. SYM	MIN	MAX	MIN	MAX	UNIT
Cycle time, read[2]	$t_{c(rd)}/t_{RC}$	190		220		ns
Cycle time, write[2]	$t_{c(W)}/t_{WC}$	190		220		ns
Cycle time, read-modify-write[2]	$t_{c(rdW)}/t_{RMW}$	250		290		ns
Cycle time, page-mode read or write[2]	$t_{c(P)}/t_{PC}$	60		70		ns
Cycle time, page-mode read-modify-write[2]	$t_{c(rdWP)}/t_{PRMW}$	105		125		ns
Cycle time, read transfer[2]	$t_{c(TRD)}/t_{RC}$	190		220		ns
Cycle time, write transfer[2]	$t_{c(TW)}/t_{WC}$	190		220		ns
Cycle time, serial clock[2]	$t_{c(SC)}/t_{SCC}$	30		35		ns
Pulse duration, CAS\ high	$t_{w(CH)}/t_{CPN}$	20		30		ns
Pulse duration, CAS\ low[4]	$t_{w(CL)}/t_{CAS}$	25	75000	30	75000	ns
Pulse duration, RAS\ high	$t_{w(RH)}/t_{RP}$	80		90		ns
Pulse duration, RAS\ low[5]	$t_{w(RL)}/t_{RAS}$	100	75000	120	75000	ns
Pulse duration,W\ low	$t_{w(WL)}/t_{WP}$	25		25		ns
Pulse duration, TRG\ low	$t_{w(TRG)}$	25		30		ns
Pulse duration, SC high	$t_{w(SCH)}/t_{SC}$	10		12		ns
Pulse duration, SC low	$t_{w(SCL)}/t_{SCP}$	10		12		ns
Pulse duration, SE\ low	$t_{w(SEL)}/t_{SE}$	35		40		ns
Pulse duration, SE\ high	$t_{w(SEH)}/t_{SEP}$	35		40		ns
Pulse duration, TRG\ high	$t_{w(GH)}/t_{TP}$	30		20		ns
Pulse duration, RAS\ low (page mode)	$t_{w(RL)P}$	100	75000	120	75000	ns
Setup time, column address	$t_{su(CA)}/t_{ASC}$	0		0		ns
Setup time, DSF before CAS\ low	$t_{su(SFC)}/t_{FSC}$	0		0		ns
Setup time, row address	$t_{su(RA)}/t_{ASR}$	0		0		ns
Setup time, W\ before RAS\ low	$t_{su(WMR)}/t_{WSR}$	0		0		ns
Setup time, DQ before RAS\ low	$t_{su(DQR)}/t_{MS}$	0		0		ns
Setup time, TRG\ before RAS\ low	$t_{su(TRG)}/t_{THS}$	0		0		ns
Setup time, SE\ before RAS\ low[6]	$t_{su(SE)}/t_{ESR}$	0		0		ns
Setup time, serial write disable	$t_{su(SESC)}/t_{SWIS}$	10		15		ns
Setup time, DSF before RAS\ low	$t_{su(SFR)}/t_{FSR}$	0		0		ns
Setup time, data before CAS\ low	$t_{su(DCL)}/t_{DSC}$	0		0		ns
Setup time, data before W\ low	$t_{su(DWL)}/t_{DSW}$	0		0		ns
Setup time, read command	$t_{su(rd)}/t_{RCS}$	0		0		ns
Setup time, early write command before CAS\ low	$t_{su(WCL)}/t_{WCS}$	0		0		ns
Setup time, write before CAS\ high	$t_{su(WCH)}/t_{CWL}$	25		30		ns
Setup time, write before RAS\ high with TRG\ = W\ = low	$t_{su(WRH)}/t_{RWL}$	25		30		ns

TIMING REQUIREMENTS (continued)[1]

		-10		-12		
PARAMETER	SYM/ALT. SYM	MIN	MAX	MIN	MAX	UNIT
Setup time, SDQ before SC high	$t_{su(SDS)}/t_{SDS}$	0		0		ns
Hold time, column address after CAS\ low	$t_{h(CLCA)}/t_{CAH}$	20		20		ns
Hold time, DSF after CAS\ low	$t_{h(SFC)}/t_{CFH}$	20		20		ns
Hold time, row address after RAS\ low	$t_{h(RA)}/t_{RAH}$	15		15		ns
Hold time, TRG\ after RAS\ low	$t_{h(TRG)}/t_{TLH}$	15		15		ns
Hold time, SE\ after RAS\ low with TRG\ = W\ = low[6]	$t_{h(SE)}/t_{REH}$	15		15		ns
Hold time, write mask, transfer enable after RAS\ low	$t_{h(RWM)}/t_{RWH}$	15		15		ns
Hold time, DQ after RAS\ low (write-mask operation)	$t_{h(RDQ)}/t_{MH}$	15		15		ns
Hold time, DSF after RAS\ low	$t_{h(SFR)}/t_{RFH}$	15		15		ns
Hold time, column address after RAS\ low[7]	$t_{h(RLCA)}/t_{AR}$	45		45		ns
Hold time, data after CAS\ low	$t_{h(CLD)}/t_{DH}$	20		25		ns
Hold time, data after RAS\ low[7]	$t_{h(RLD)}/t_{DHR}$	45		50		ns
Hold time, data after W\ low	$t_{h(WLD)}/t_{DH}$	20		25		ns
Hold time, read after CAS\ high[8]	$t_{h(CHrd)}/t_{RCH}$	0		0		ns
Hold time, read after RAS\ high[8]	$t_{h(RHrd)}/t_{RRH}$	10		10		ns
Hold time, write after CAS\ low	$t_{h(CLW)}/t_{WCH}$	30		35		ns
Hold time, write after RAS\ low[7]	$t_{h(RLW)}/t_{WCR}$	50		55		ns
Hold time, TRG\ after W\ low[9]	$t_{h(WLG)}/t_{OEH}$	25		30		ns
Hold time, SDQ after SC high	$t_{h(SDS)}/t_{SDH}$	5		5		ns
Hold time, SDQ after SC high	$t_{h(SHSQ)}/t_{SOH}$	5		5		ns
Hold time, DSF after RAS\ low	$t_{h(RSF)}/t_{FHR}$	45		45		ns
Hold time, serial-write disable	$t_{h(SCSE)}/t_{SWIH}$	20		20		ns
Delay time, RAS\ low to CAS\ high	$t_{d(RLCH)}/t_{CSH}$	100		120		ns
Delay time, CAS\ high to RAS\ low	$t_{d(CHRL)}/t_{CRP}$	0		0		ns
Delay time, CAS\ low to RAS\ high	$t_{d(CLRH)}/t_{RSH}$	25		30		ns
Delay time, CAS\ low to W\ low[10,11]	$t_{d(CLWL)}/t_{CWD}$	55		65		ns
Delay time, RAS\ low to CAS\ low[12]	$t_{d(RLCL)}/t_{RCD}$	25	75	25	90	ns
Delay time, column address to RAS\ high	$t_{d(CARH)}/t_{RAL}$	50		60		ns
Delay time, RAS\ low to W\ low[10]	$t_{d(RLWL)}/t_{RWD}$	130		155		ns
Delay time, column address to W\ low[10]	$t_{d(CAWL)}/t_{AWD}$	85		100		ns
Delay time, RAS\ low to CAS\ high[13]	$t_{d(RLCH)RF}/t_{CHR}$	25		25		ns
Delay time, CAS\ low to RAS\ low[13]	$t_{d(CLRL)RF}/t_{CSR}$	10		10		ns
Delay time, RAS\ high to CAS\ low[13]	$t_{d(RHCL)RF}/t_{RPC}$	10		10		ns
Delay time, CAS\ low to TRG\ high for DRAM read cycles	$t_{d(CLGH)}$	25		30		ns

TIMING REQUIREMENTS (continued)[1]

		-10		-12		
PARAMETER	SYM/ALT. SYM	MIN	MAX	MIN	MAX	UNIT
Delay time, TRG\ high before data applied at DQ	$t_{d(GHD)}/t_{OED}$	25		30		ns
Delay time, RAS\ low to TRG\ high (real-time-reload read-transfer cycle only)	$t_{d(RLTH)}/t_{RTH}$	90		95		ns
Delay time, RAS\ low to first SC high after TRG\ high[14]	$t_{d(RLSH)}/t_{RSD}$	130		140		ns
Delay time, CAS\ low to first SC high after TRG\ high[14]	$t_{d(CLSH)}/t_{CSD}$	40		45		ns
Delay time, SC high to TRG\ high[14,15,16]	$t_{d(SCTR)}/t_{TSL}$	15		20		ns
Delay time, TRG\ high to RAS\ high[15,16]	$t_{d(THRH)}/t_{TRD}$	-10		-10		ns
Delay time, SC high to RAS\ low with TRG\ = W\ = low[6, 17, 18]	$t_{d(SCRL)}/t_{SRS}$	10		20		ns
Delay time, SC high to SE\ high in serial-input mode	$t_{d(SCSE)}$	20		20		ns
Delay time, RAS\ high to SC high[6]	$t_{d(RHSC)}/t_{SRD}$	25		30		ns
Delay time, TRG\ high to RAS\ low[19]	$t_{d(THRL)}/t_{TRP}$	$t_{w(RH)}$		$t_{w(RH)}$		ns
Delay time, TRG\ high to SC high[15, 16]	$t_{d(THSC)}/t_{TSD}$	35		40		ns
Delay time, SE\ low to SC high[20]	$t_{d(SESC)}/t_{SWS}$	10		15		ns
Delay time, RAS\ high to last (most significant) rising edge of SC before boundary switch during split-register read-transfer cycles	$t_{d(RHMS)}$	15		20		ns
Delay time, CAS\ low to TRG\ high in real-time read-transfer cycles	$t_{d(CLGH)}/t_{CTH}$	5		5		ns
Delay time, column address to first SC in early-load read-transfer cycles	$t_{d(CASH)}/t_{ASD}$	45		50		ns
Delay time, column address to TRG\ high in real-time read-transfer cycles	$t_{d(CAGH)}/t_{ATH}$	10		10		ns
Delay time, RAS\ low to column address[12]	$t_{d(RLCA)}/t_{RAD}$	15	50	15	60	ns
Delay time, data to CAS\ low	$t_{d(DCL)}/t_{DZC}$	0		0		ns
Delay time, data to TRG\ low	$t_{d(DGL)}/t_{DZO}$	0		0		ns
Delay time, RAS\ low to serial-input data	$t_{d(RLSD)}/t_{SDD}$	50		50		ns
Delay time, TRG\ low to RAS\ high	$t_{d(GLRH)}/t_{ROH}$	25		30		ns
Delay time, last (most significant) rising edge of SC to RAS\ low before boundary switch during split-register read-transfer cycles	$t_{d(MSRL)}$	25		25		ns
Delay time, last (255 or 511) rising edge of SC to QSF switching a the boundary during split-register read transfer cycles[21]	$t_{d(SCQSF)}/t_{SQD}$		40		40	ns
Delay time, CAS\ low to QSF switching in read-transfer or write-transfer cycles[21]	$t_{d(CLQSF)}/t_{CQD}$		35		35	ns
Delay time, TRG\ high to QSF switching in read-transfer or write-transfer cycles[21]	$t_{d(GHQSF)}/t_{TQD}$		30		30	ns
Delay time, RAS\ low to QSF switching in read-transfer or write-transfer cycles[21]	$t_{d(RLQSF)}/t_{RQD}$		75		75	ns
Refresh time interval, memory	t_{rf}/t_{REF}		8		8	ms
Transition time	t_t/t_T	3	50	3	50	ns

NOTES:

1. Timing measurements are referenced to V_{IL} max and V_{IH} min.
2. All cycle times assume t_t = 5 ns.
3. When the odd tap is used (tap address can be 0–511, and odd taps are 1, 3, 5, etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.
4. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional CAS\ low time [$t_{w(CL)}$].
5. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional RAS\ low time [$t_{w(RL)}$].
6. Register-to-memory (write) transfer cycles only
7. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
8. Either $t_{h(RHrd)}$ or $t_{(CHrd)}$ must be satisfied for a read cycle.
9. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
10. Read-modify-write operation only
11. TRG\ must disable the output buffers prior to applying data to the DQ terminals.
12. The maximum value is specified only to assure RAS\ access time.
13. CAS\-before-RAS\ refresh operation only
14. Early-load read-transfer cycle only
15. Real-time-reload read-transfer cycle only
16. Late-load read-transfer cycle only
17. In a read-transfer cycle, the state of SC when RAS\ falls is a don't care condition. However, to assure proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when RAS\ goes low.
18. In a memory-to-register (read) transfer cycle, $t_{d(SCRL)}$ applies only when the SAM was previously in serial-input mode.
19. Memory-to-register (read) and register-to-memory (write) transfer cycles only
20. Serial data-in cycles only
21. Switching times assume C_L = 100 pF unless otherwise noted (see Figure 12).

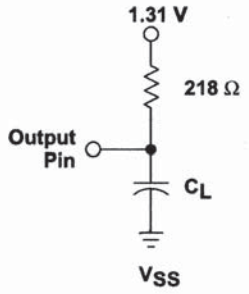


FIGURE 12: LOAD CIRCUIT

FIGURE 13: Read-Cycle Timing

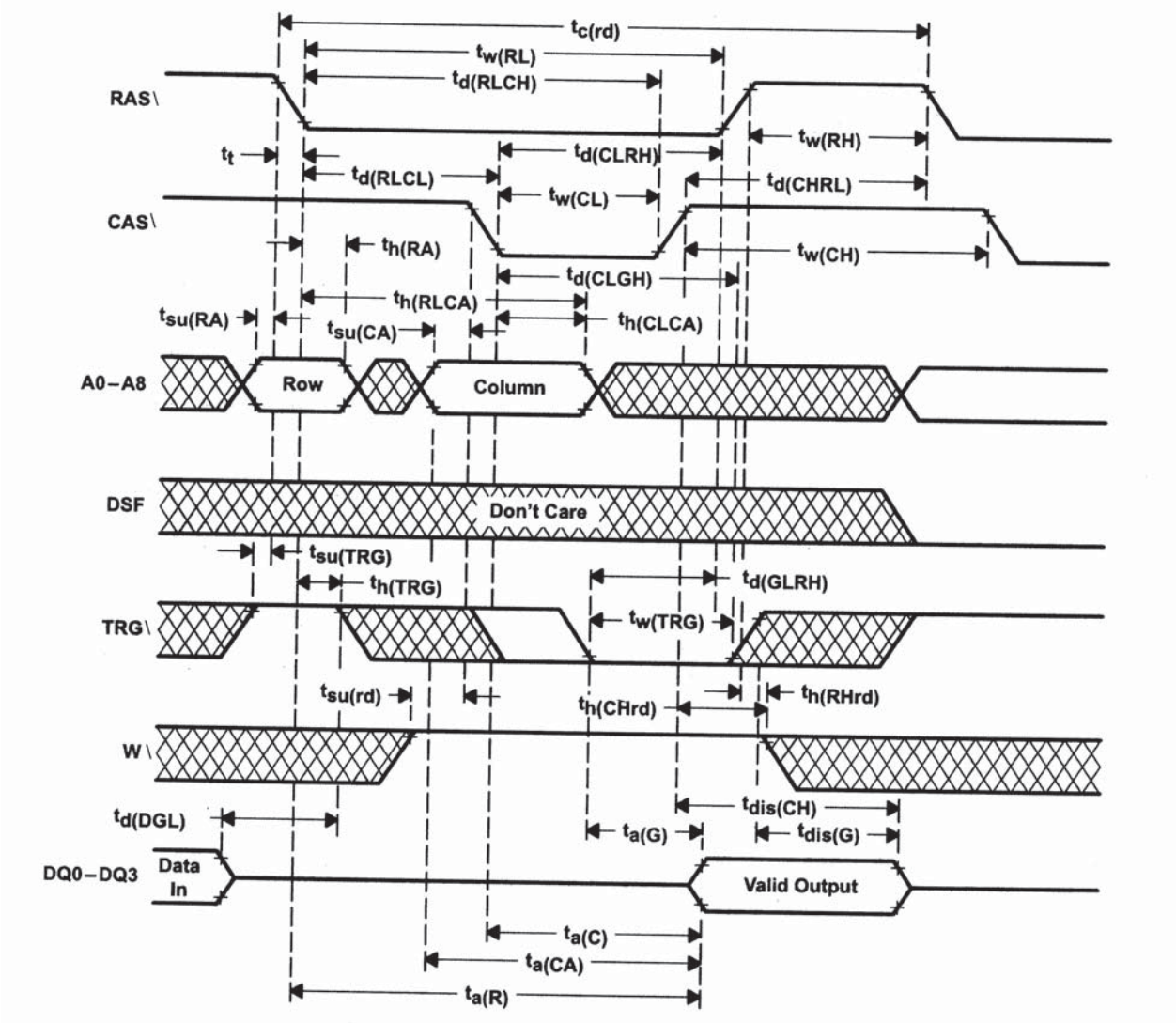
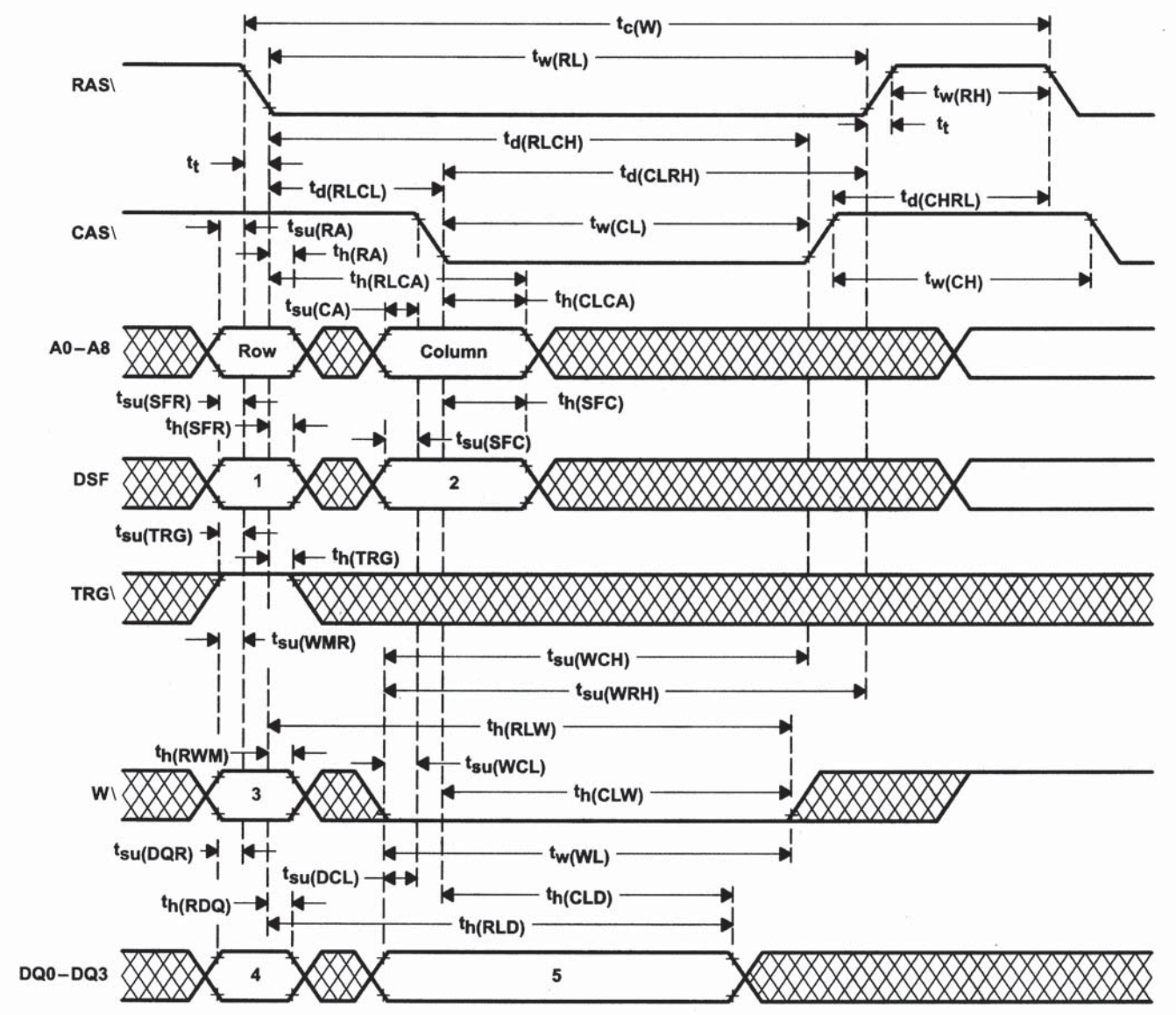


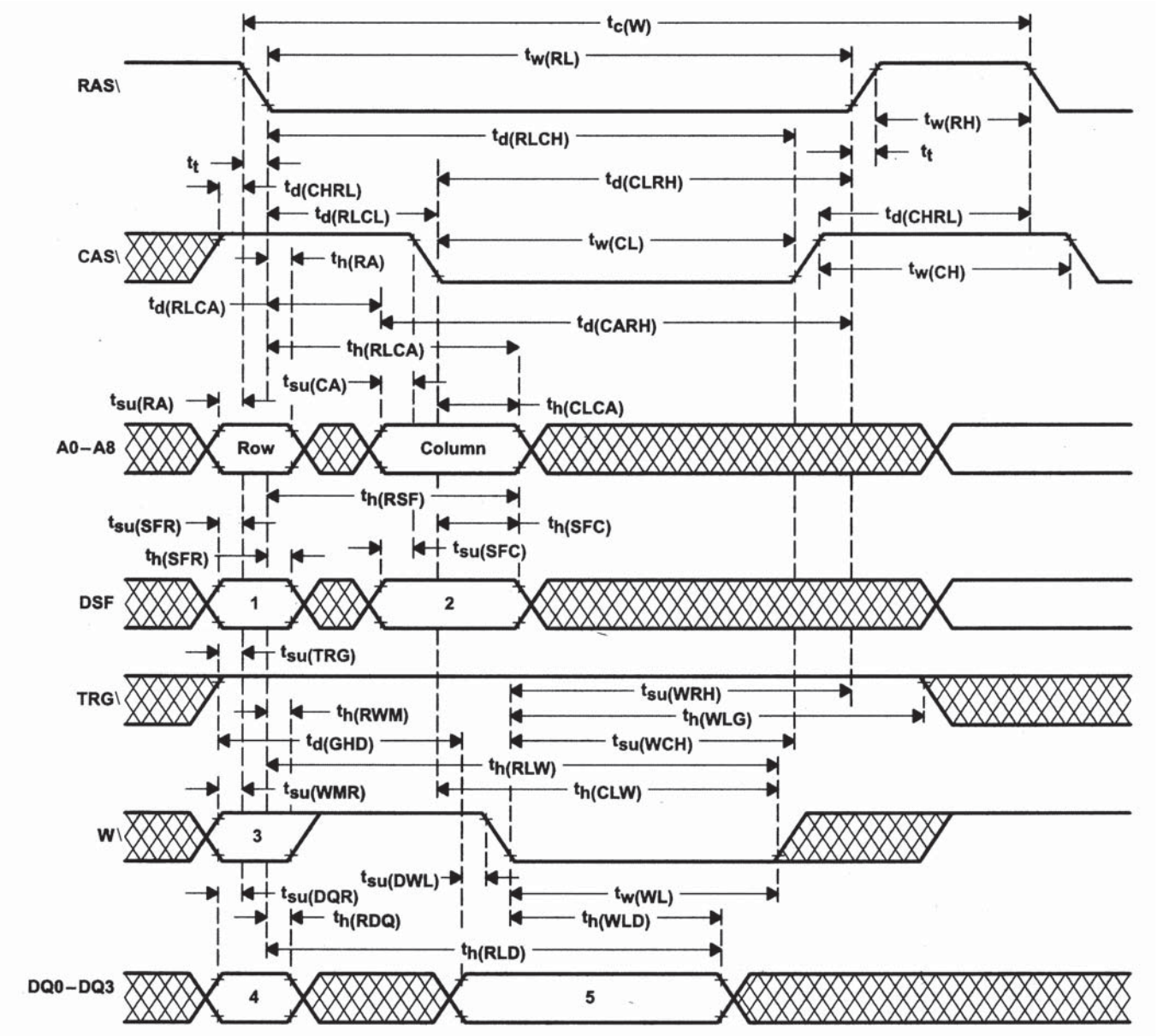
FIGURE 14: Early-Write-Cycle Timing



WRITE-CYCLE STATE TABLE

CYCLE	STATE				
	1	2	3	4	5
Write Operation	L	L	H	Don't Care	Valid Data
Write-mask load/use, Write DQs to I/Os	L	L	L	Write Mask	Valid Data
Use previous write mask, Write DQs to I/Os	H	L	L	Don't Care	Valid Data
Load write mask on later of W\ fall and CAS\ fall	H	L	H	Don't Care	Write Mask

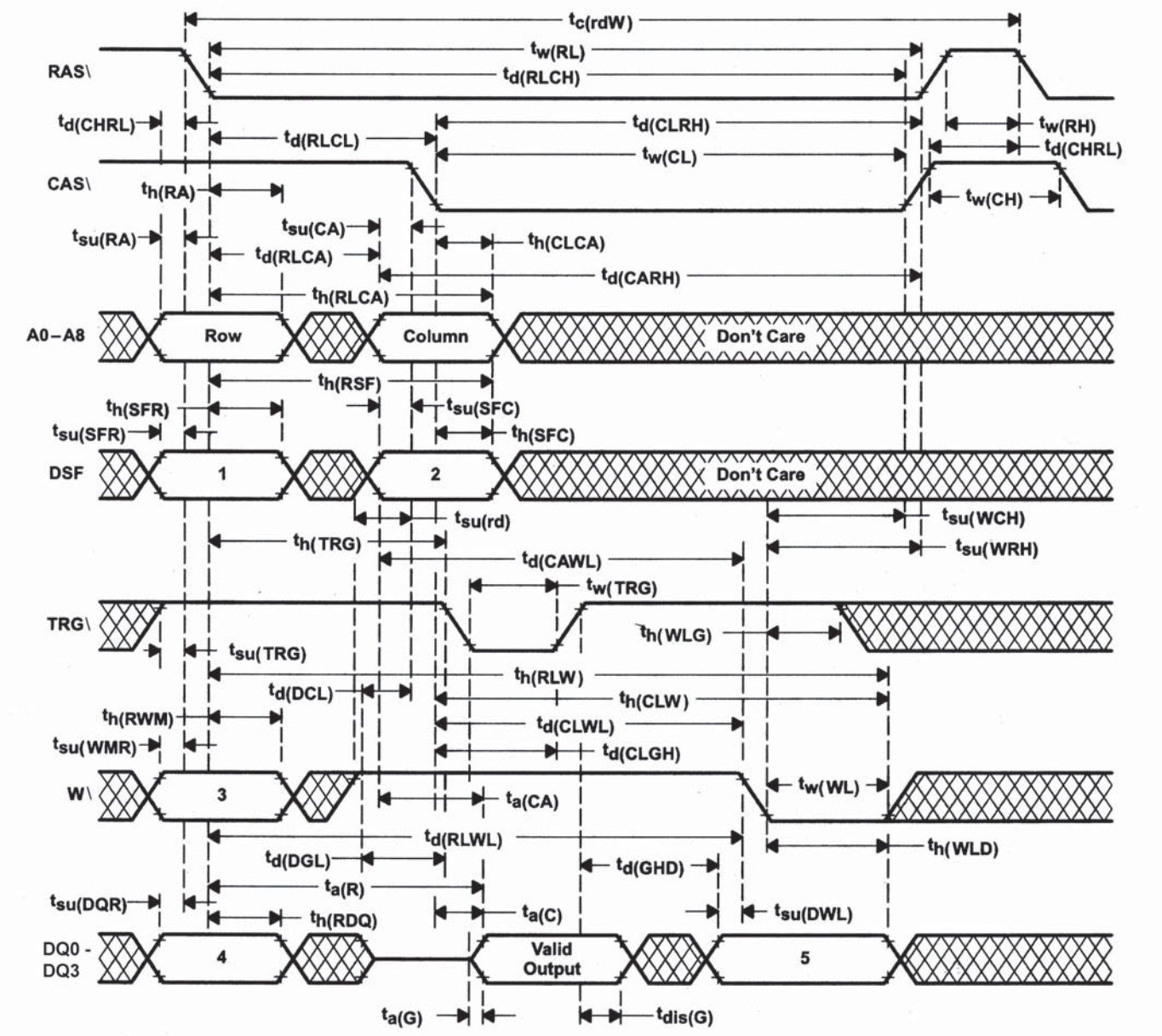
FIGURE 15: Delayed-Write-Cycle Timing (Output-Enable-Controlled Write)



WRITE-CYCLE STATE TABLE

CYCLE	STATE				
	1	2	3	4	5
Write Operation	L	L	H	Don't Care	Valid Data
Write-mask load/use, Write DQs to I/Os	L	L	L	Write Mask	Valid Data
Use previous write mask, Write DQs to I/Os	H	L	L	Don't Care	Valid Data
Load write mask on later of W\ fall and CAS\ fall	H	L	H	Don't Care	Write Mask

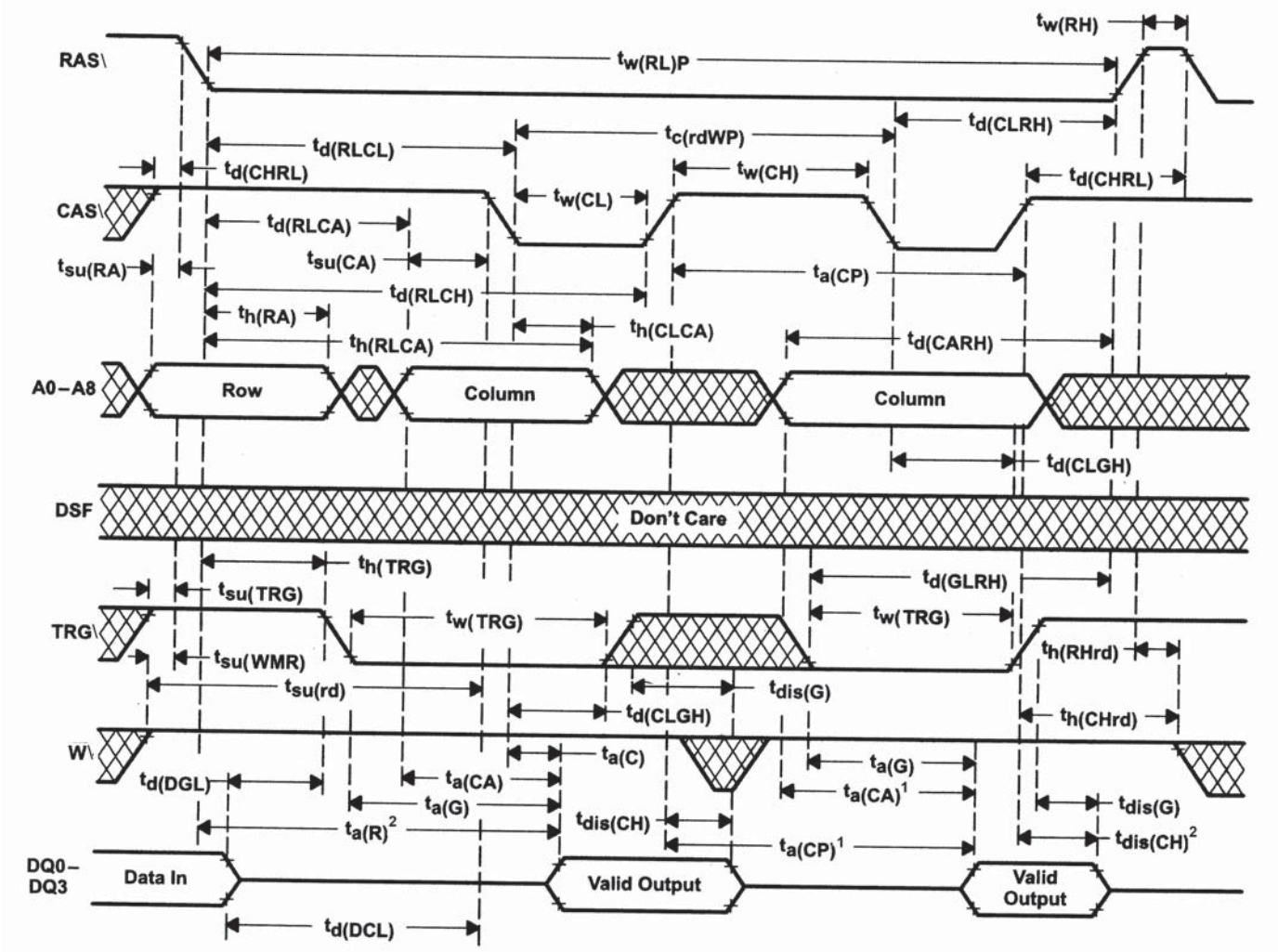
FIGURE 16: Read-Write/Read-Modify-Write-Cycle Timing



WRITE-CYCLE STATE TABLE

CYCLE	STATE				
	1	2	3	4	5
Write Operation	L	L	H	Don't Care	Valid Data
Write-mask load/use, Write DQs to I/Os	L	L	L	Write Mask	Valid Data
Use previous write mask, Write DQs to I/Os	H	L	L	Don't Care	Valid Data
Load write mask on later of W\ fall and CAS\ fall	H	L	H	Don't Care	Write Mask

FIGURE 17: Enhanced-Page-Mode Read-Cycle Timing

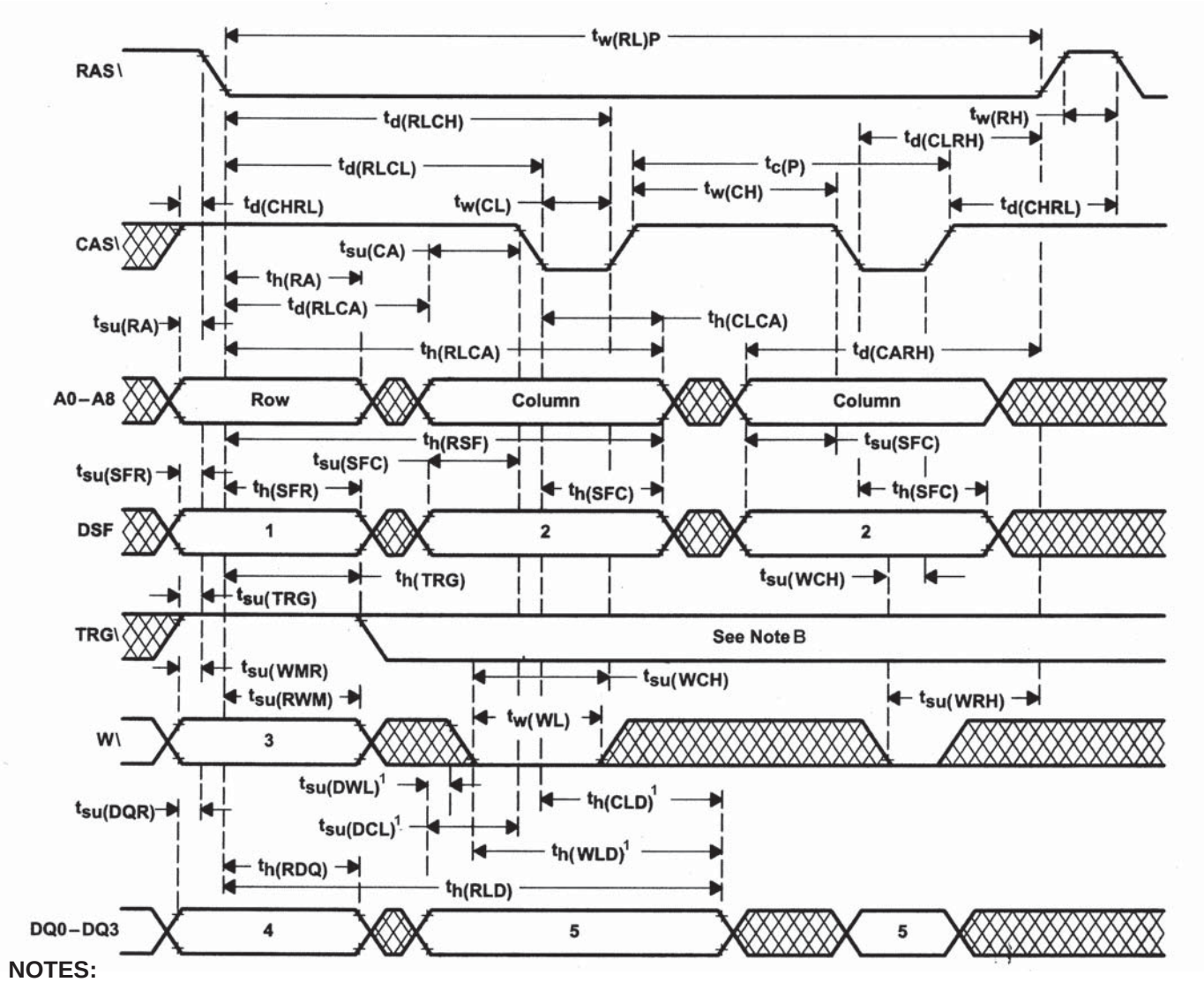


NOTES:

1. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
2. Output can go from the high-impedance state to an invalid data state prior to the specified access time.

NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edges of RAS\ and CAS\ to select the desired write mode (normal, block write, etc.)

FIGURE 18: Enhanced-Page-Mode Write-Cycle Timing



NOTES:

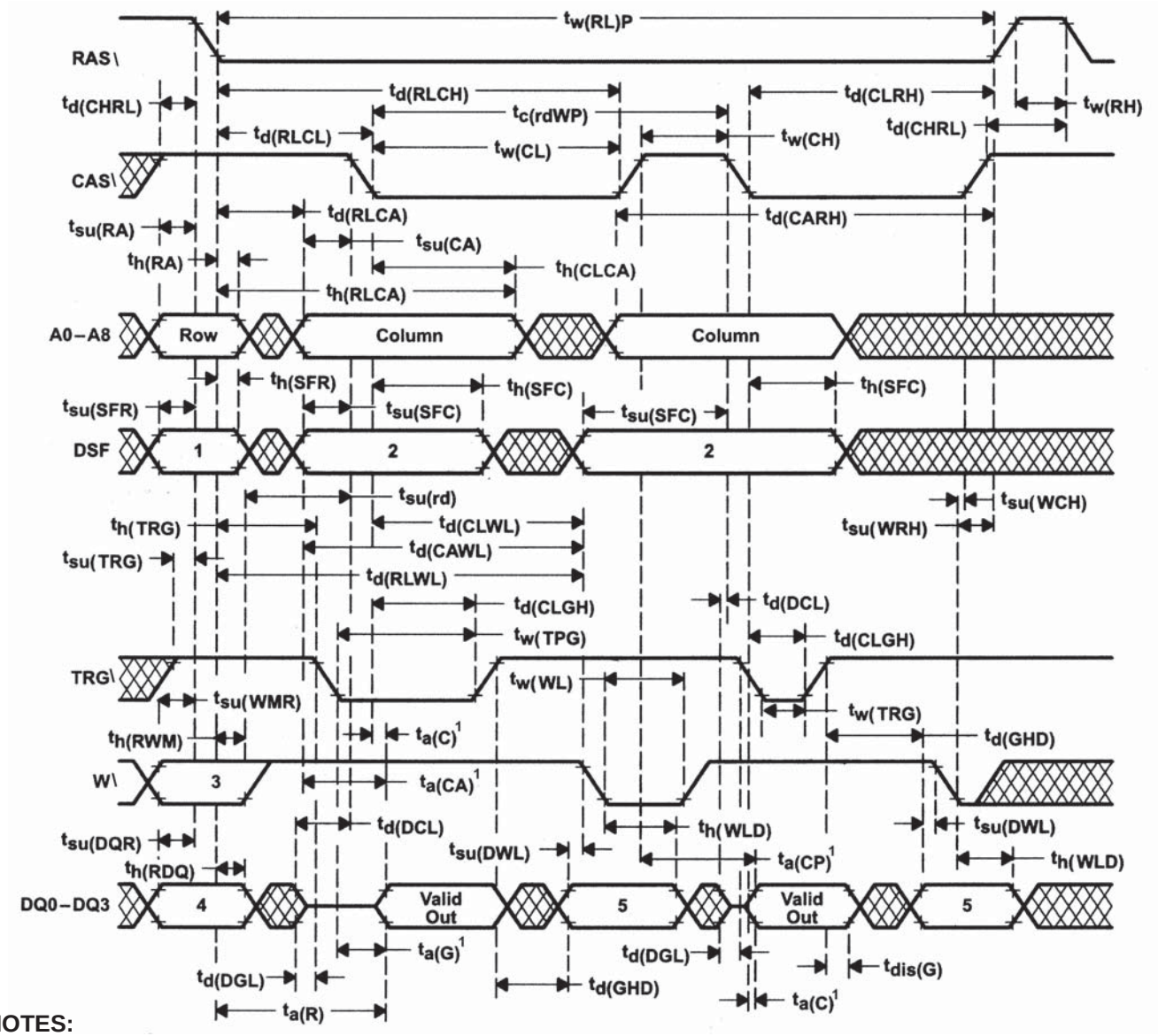
1. Referenced to CAS or W, whichever occurs last

NOTE B: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. TRG\ must remain high throughout the entire page-mode operation to assure page-mode cycle time if the late-write feature is used. If the early-write-cycle timing is used, the state of TRG\ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of RAS\.

WRITE-CYCLE STATE TABLE

CYCLE	STATE				
	1	2	3	4	5
Write Operation	L	L	H	Don't Care	Valid Data
Write-mask load/use, Write DQs to I/Os	L	L	L	Write Mask	Valid Data
Use previous write mask, Write DQs to I/Os	H	L	L	Don't Care	Valid Data
Load write mask on later of W\ fall and CAS\ fall	H	L	H	Don't Care	Write Mask

FIGURE 19: Enhanced-Page-Mode Read-Modify-Write-Cycle Timing



NOTES:

1. Output can go from the high-impedance state to an invalid data state prior to the specified access time.

NOTE C: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

WRITE-CYCLE STATE TABLE

CYCLE	STATE				
	1	2	3	4	5
Write Operation	L	L	H	Don't Care	Valid Data
Write-mask load/use, Write DQs to I/Os	L	L	L	Write Mask	Valid Data
Use previous write mask, Write DQs to I/Os	H	L	L	Don't Care	Valid Data
Load write mask on later of W\ fall and CAS\ fall	H	L	H	Don't Care	Write Mask

FIGURE 20: Load-Color-Register-Cycle Timing (Early-Write Load)

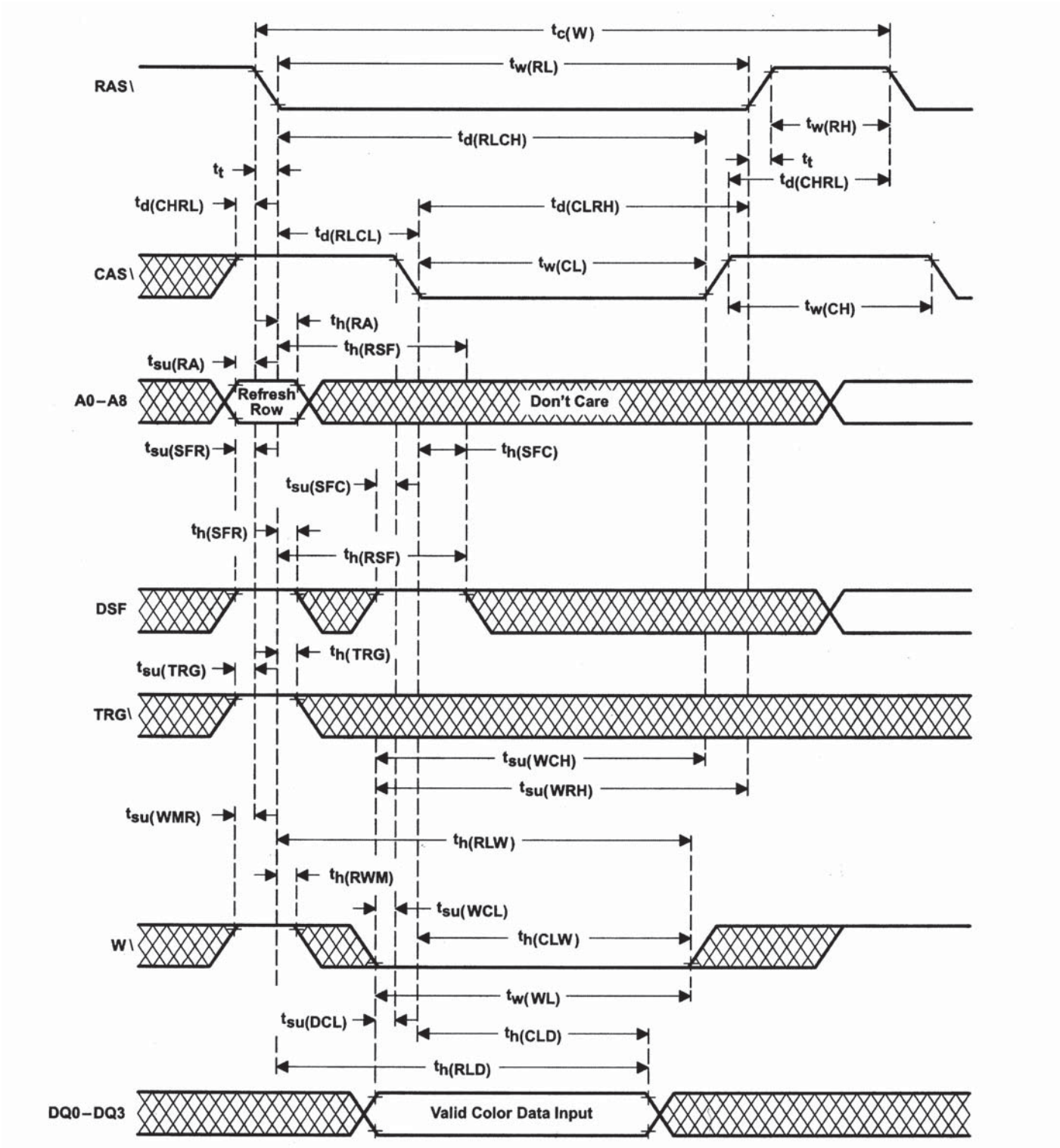


FIGURE 21: Load-Color-Register-Cycle Timing (Delayed-Write Load)

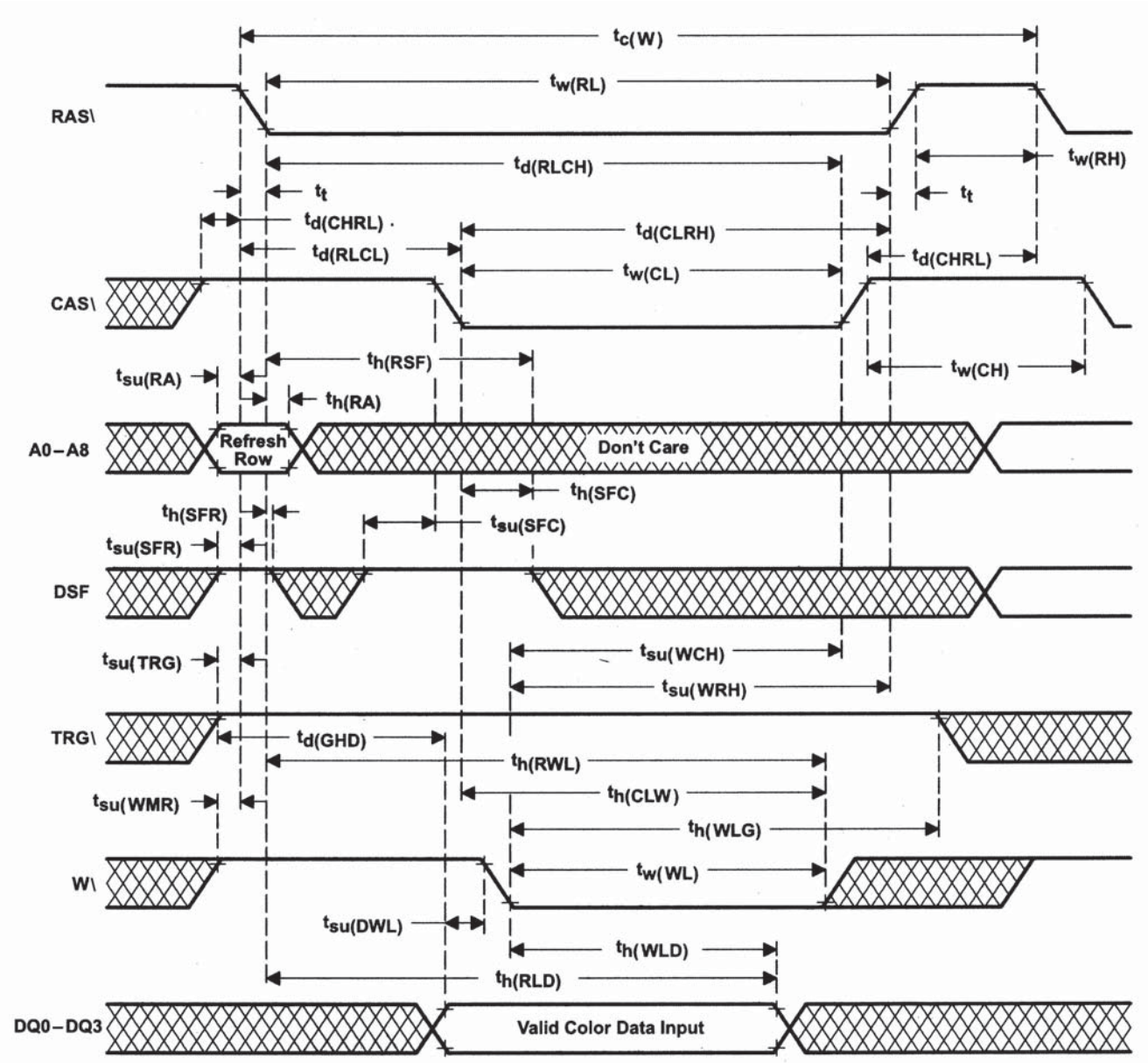
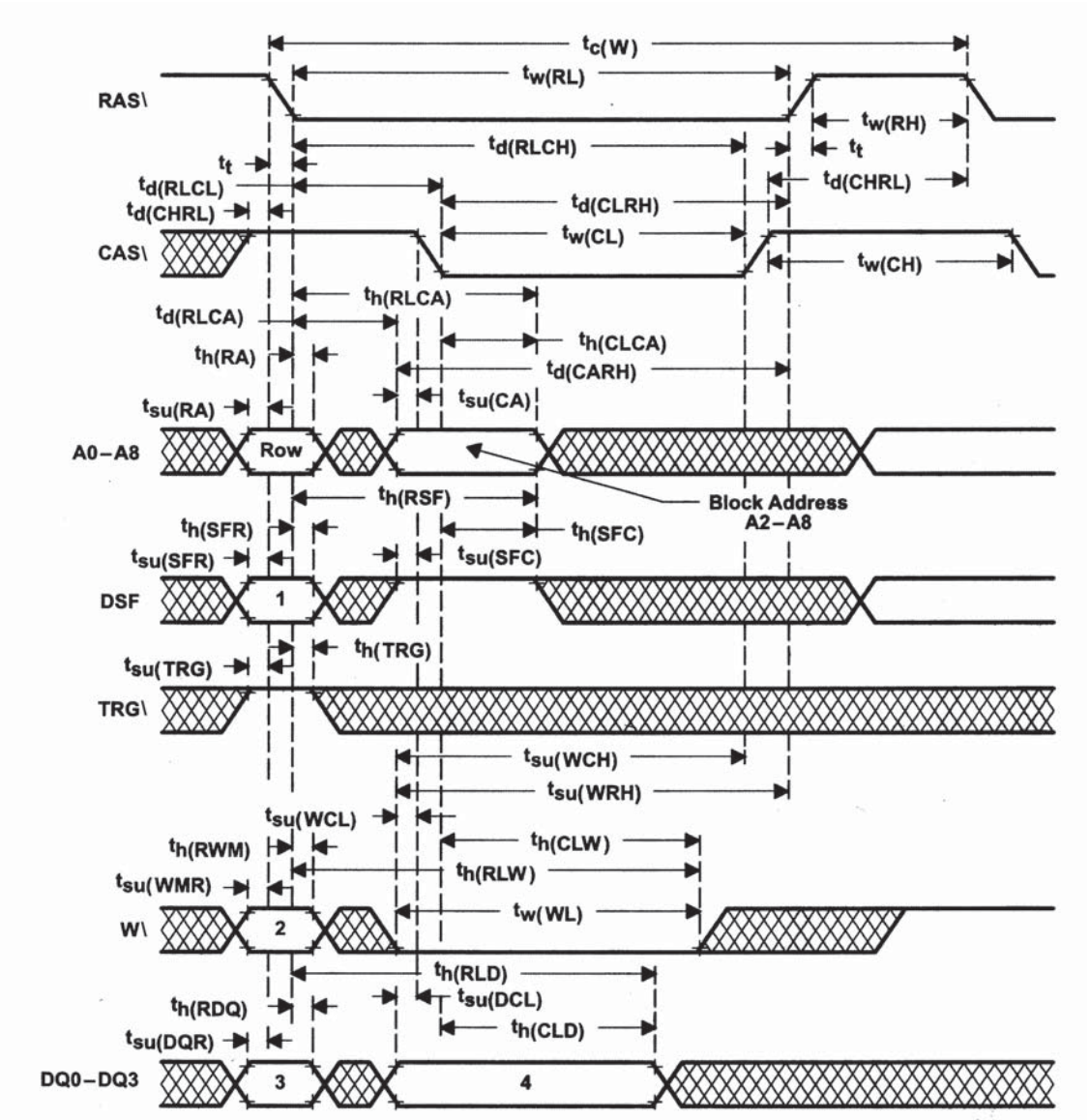


FIGURE 22: Block-Write-Cycle Timing (Early Write)



BLOCK-WRITE-CYCLE STATE TABLE

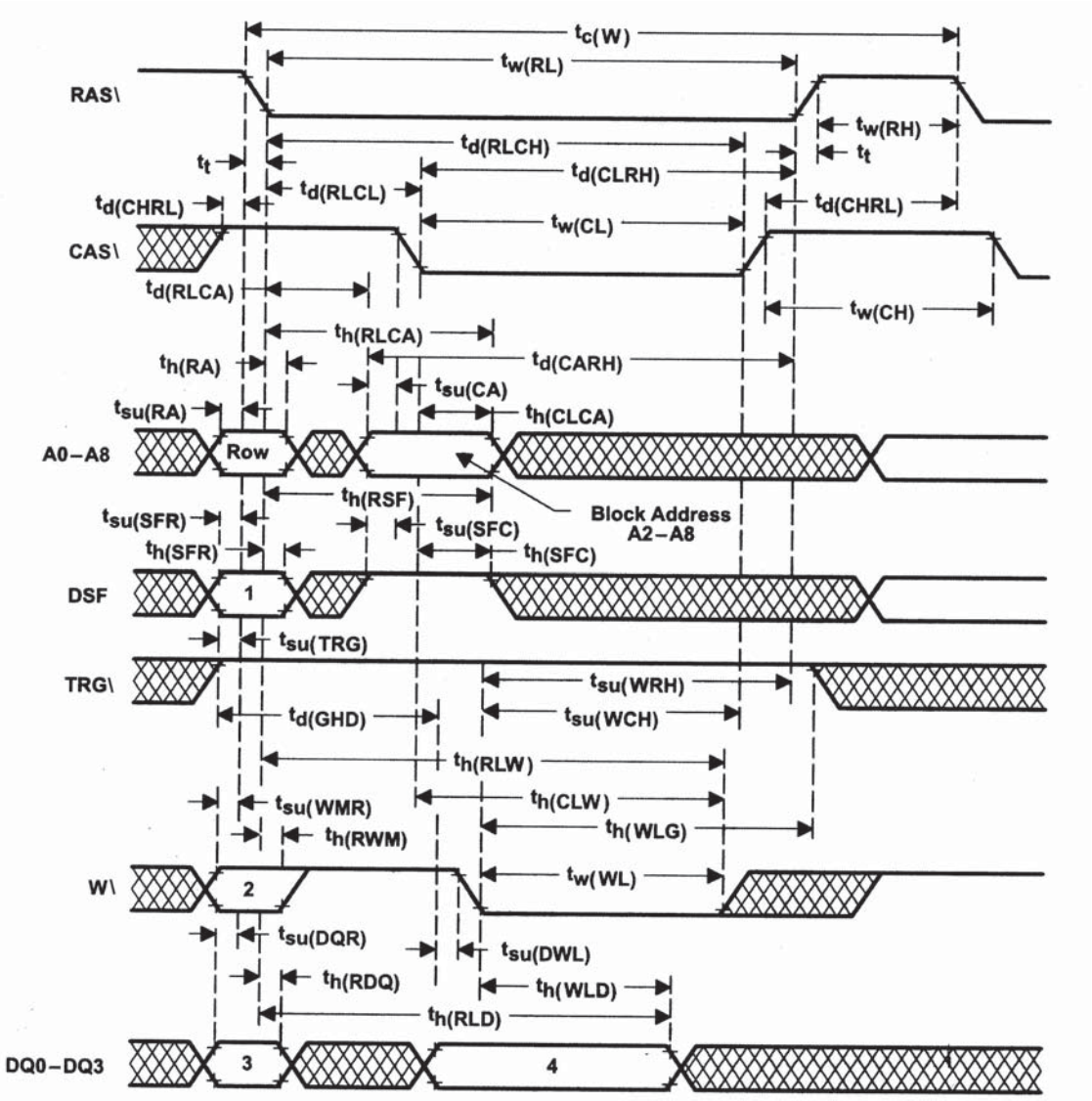
CYCLE	STATE			
	1	2	3	4
Write-mask load/use, Block write	L	L	Write Mask	Column Mask
Use previous write mask, Block write	H	L	Don't Care	Column Mask
Write mask disable, Block write to all I/Os	L	H	Don't Care	Column Mask

Write mask data 0: I/O write disable
1: I/O write enable

Column mask data DQn = 0 column write disable
(n = 0, 1, 2, 3) 1 column write enable

DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

FIGURE 23: Block-Write-Cycle Timing (Delayed-Write)



BLOCK-WRITE-CYCLE STATE TABLE

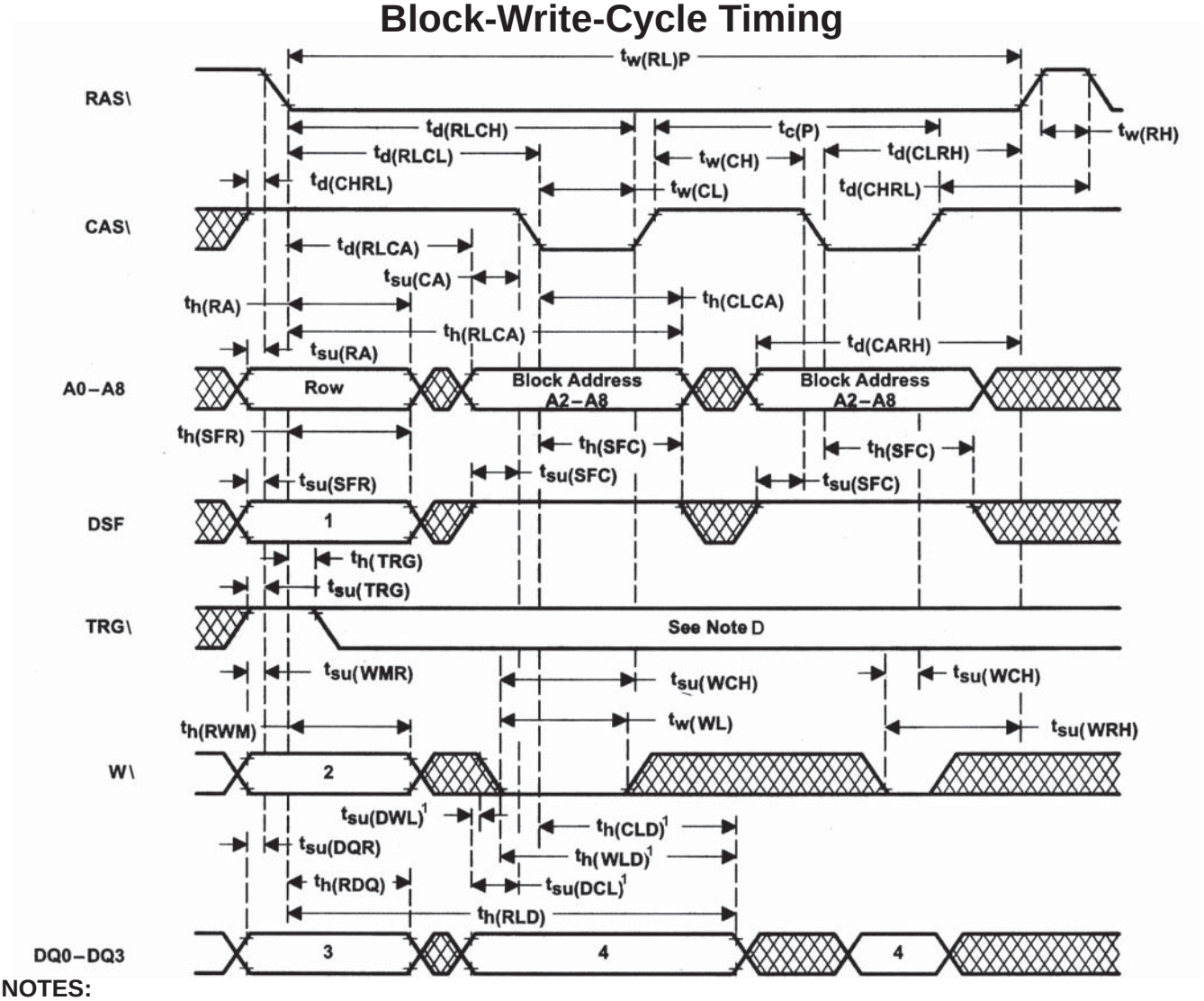
CYCLE	STATE			
	1	2	3	4
Write-mask load/use, Block write	L	L	Write Mask	Column Mask
Use previous write mask, Block write	H	L	Don't Care	Column Mask
Write mask disable, Block write to all I/Os	L	H	Don't Care	Column Mask

Write mask data 0: I/O write disable
1: I/O write enable

Column mask data DQn = (n = 0, 1, 2, 3)
0 column write disable
1 column write enable

DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

FIGURE 24: Enhanced-Page-Mode Block-Write-Cycle Timing



NOTES:

1. Referenced to CAS\ or W\, whichever occurs last

NOTE D: TRG\ must remain high throughout the entire page-mode operation to assure page-mode cycle time if the late write feature is used. If the early-write-cycle timing is used, the state of TRG\ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of RAS\.

ENHANCED-PAGE-MODE BLOCK-WRITE-CYCLE STATE TABLE

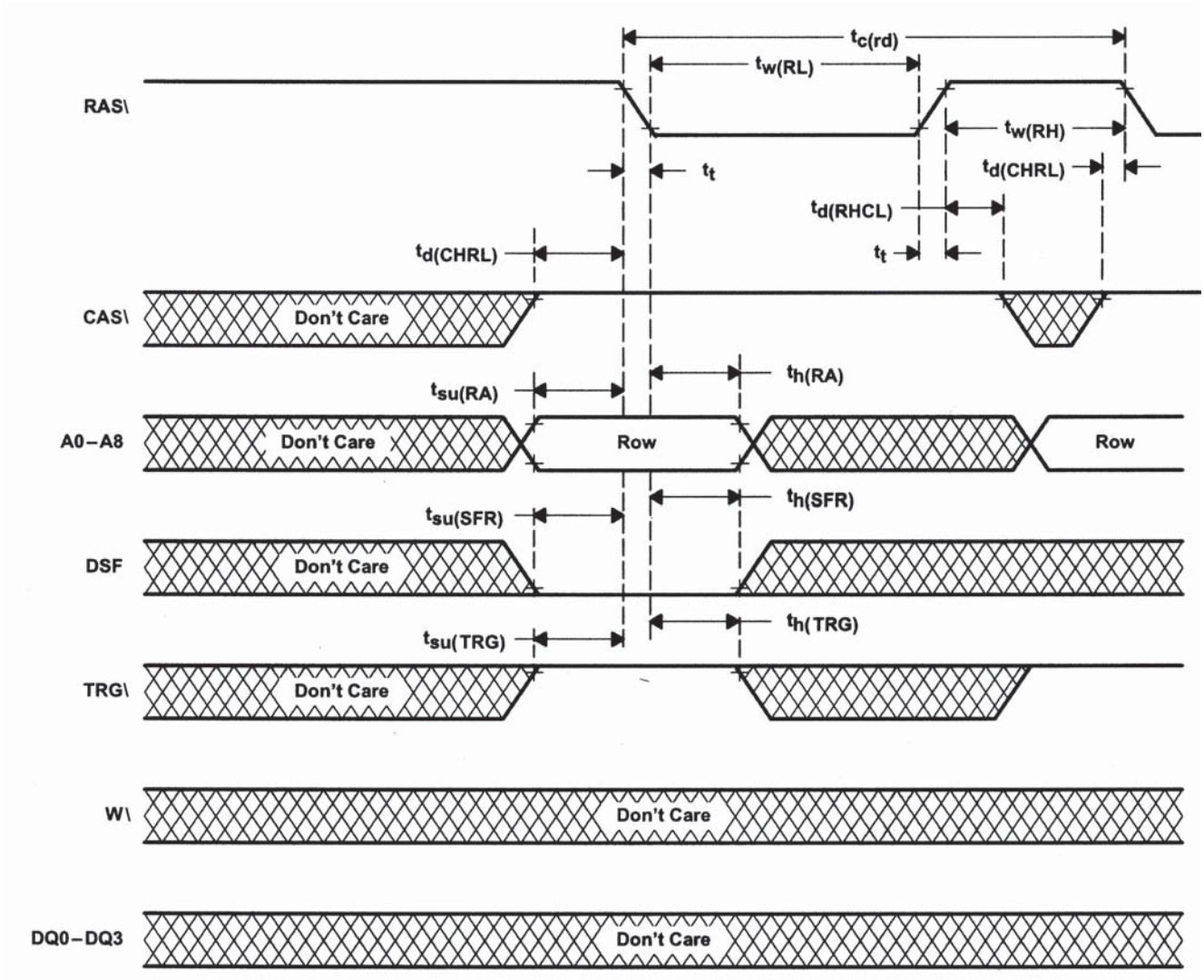
CYCLE	STATE			
	1	2	3	4
Write-mask load/use, Block write	L	L	Write Mask	Column Mask
Use previous write mask, Block write	H	L	Don't Care	Column Mask
Write mask disable, Block write to all I/Os	L	H	Don't Care	Column Mask

Write mask data 0: I/O write disable
1: I/O write enable

Column mask data DQn = (n = 0, 1, 2, 3) 0 column write disable
1 column write enable

DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

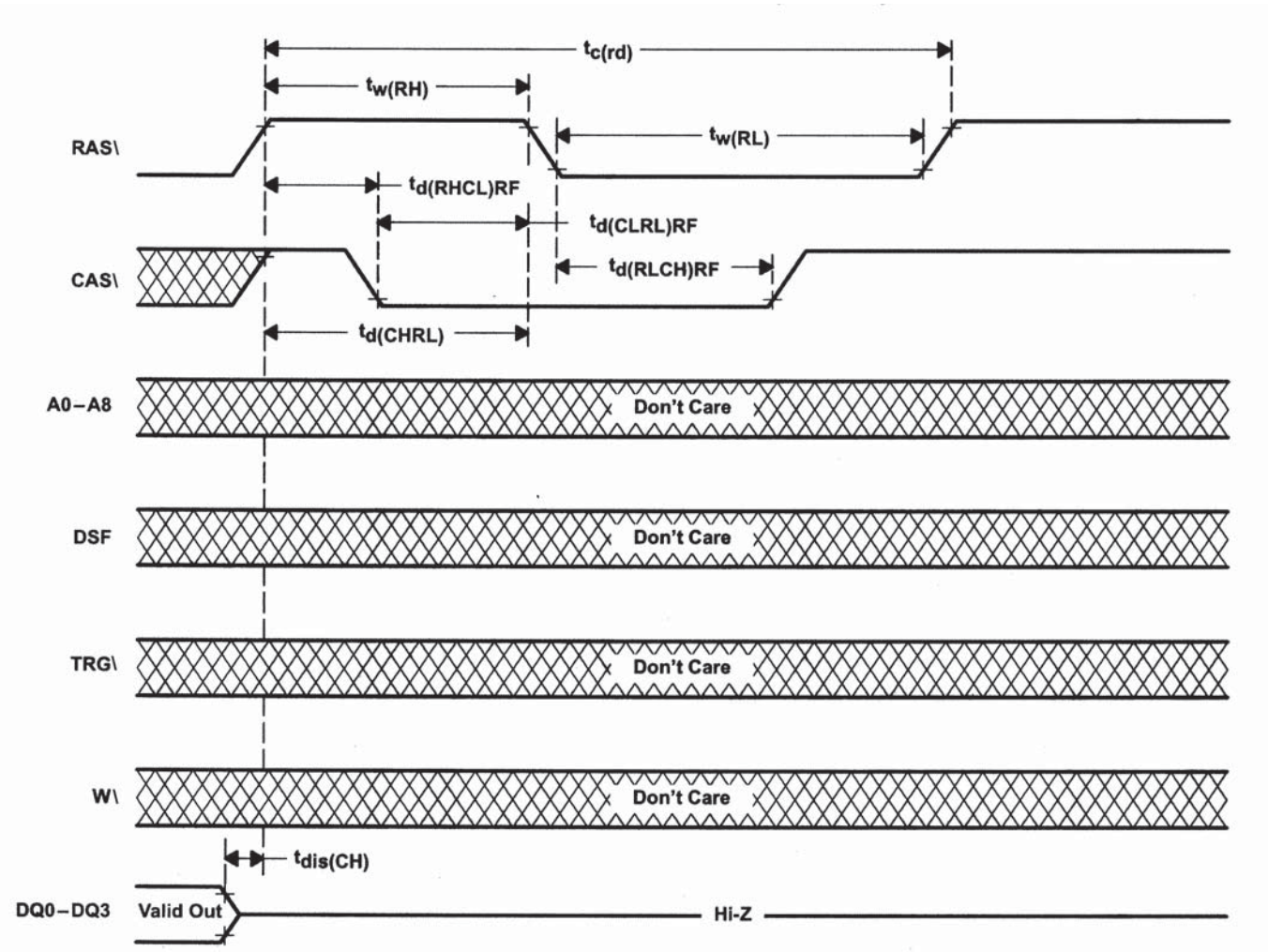
FIGURE 25: RAS\-Only Refresh-Cycle Timing



NOTES:

NOTE E: In persistent write-per-bit function, W\ must be high at the falling edge of RAS\ during the refresh cycle.

FIGURE 26: CBR-Refresh-Cycle Timing



NOTES:

NOTE F: In persistent write-per-bit operation, W\ must be high at the falling edge of RAS\ during the refresh cycle.

FIGURE 27: Hidden-Refresh-Cycle Timing

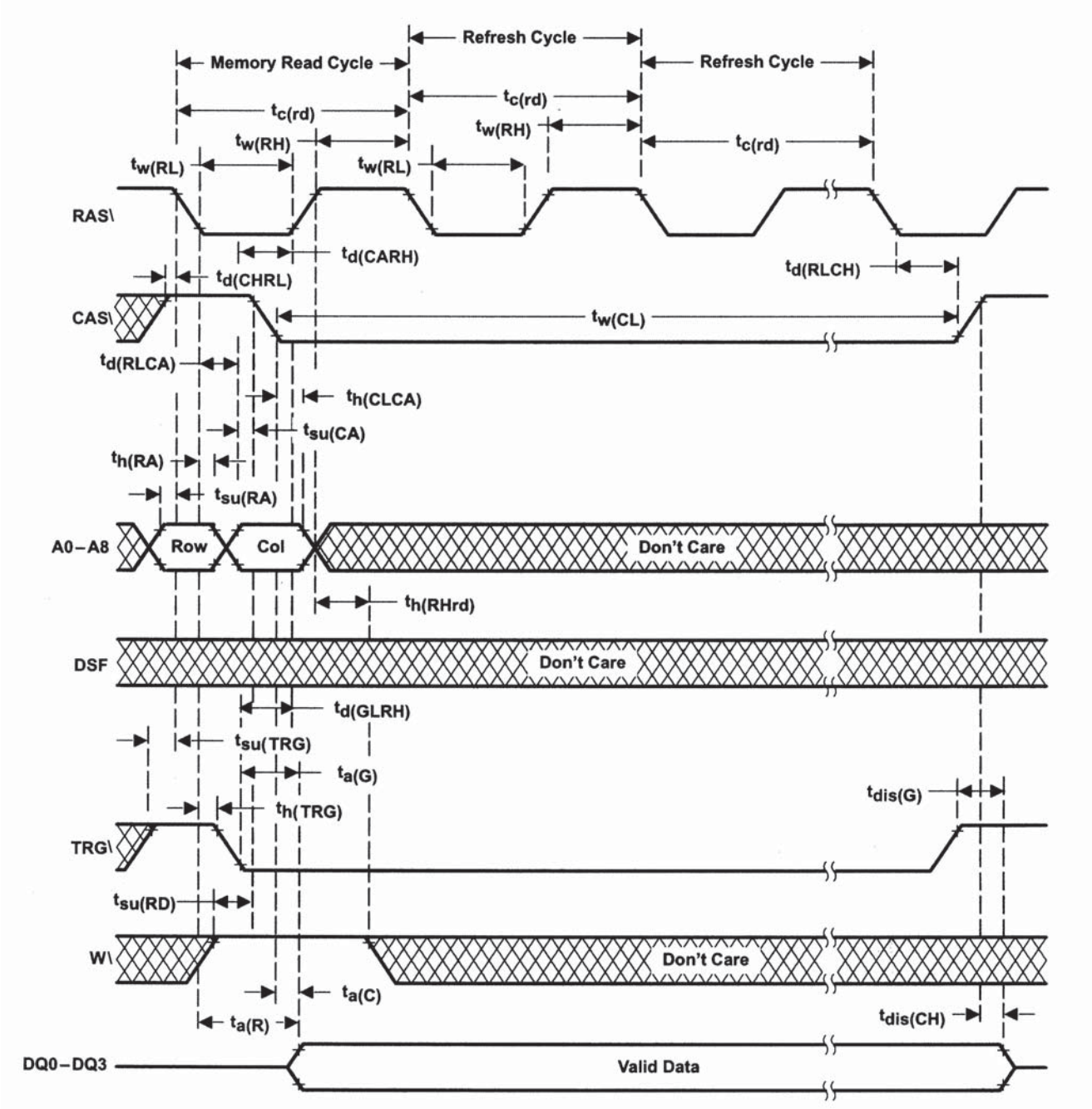
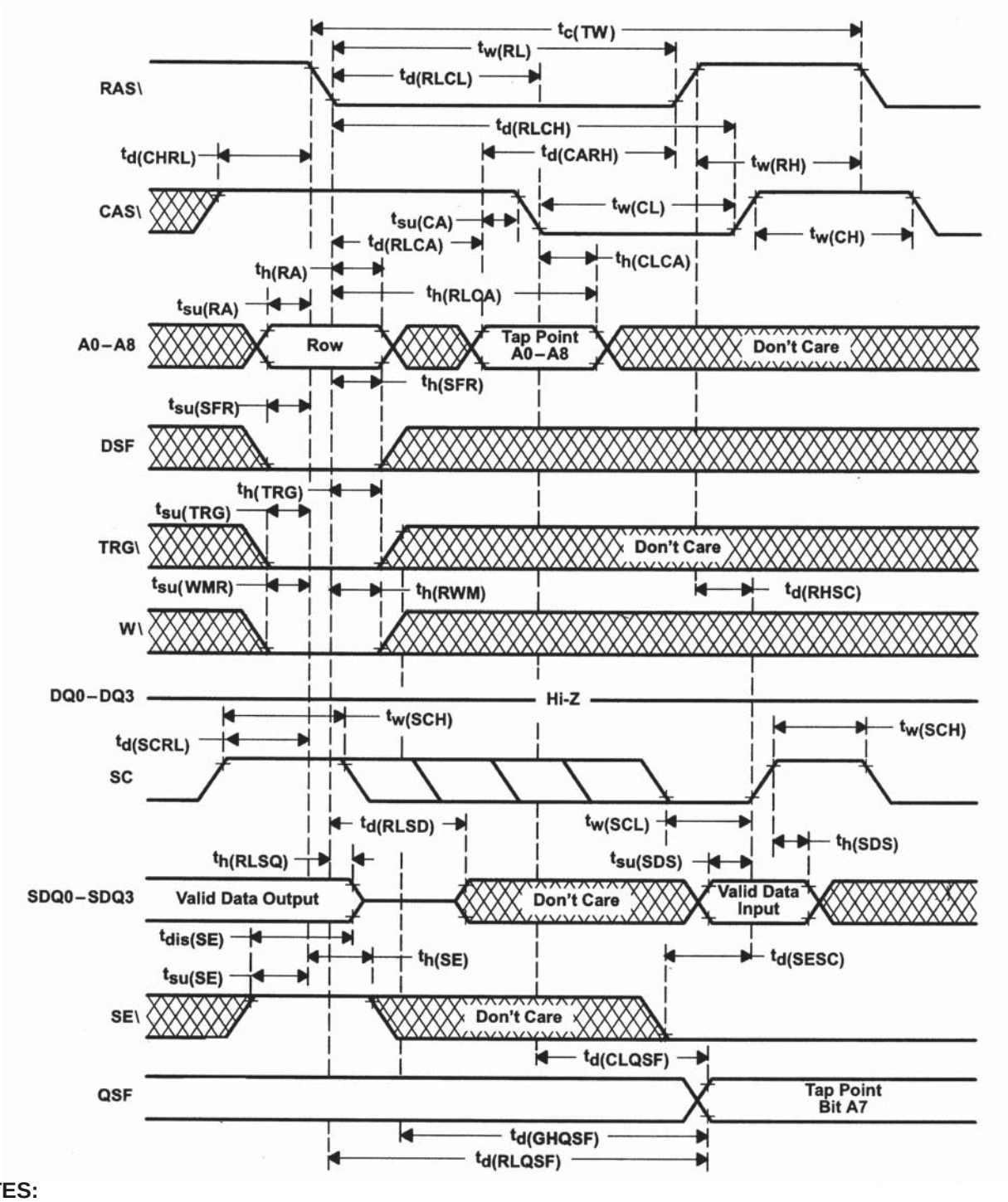


FIGURE 28: Write-Mode-Control Pseudo-Transfer Timing



NOTES:

NOTE G: The write-mode-control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. This figure assumes that the device was originally in the serial-read mode.

FIGURE 29: Data-Register-to-Memory Transfer Timing, Serial Input Enable

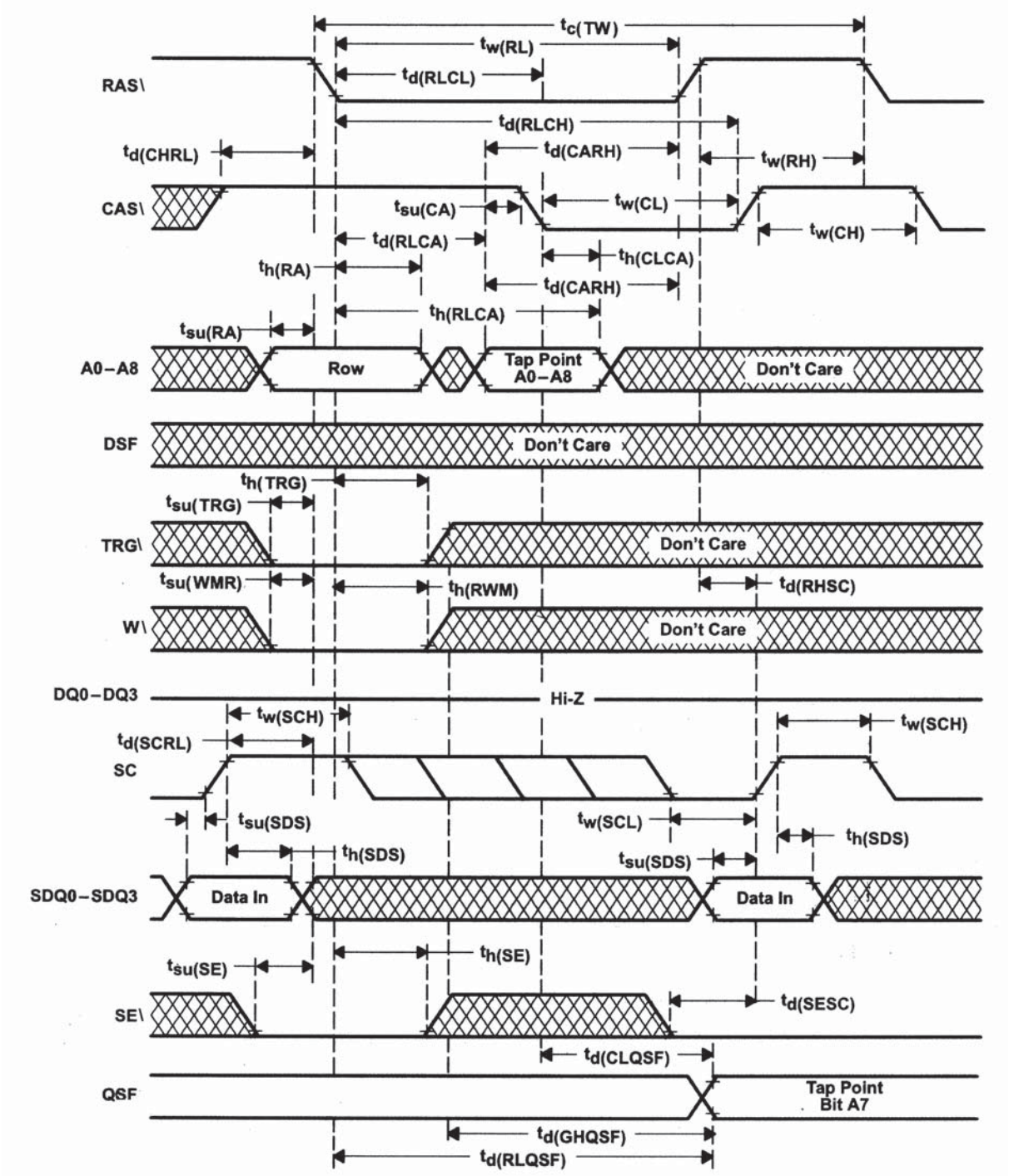


FIGURE 30: Alternate Data-Register-to-Memory Transfer-Cycle Timing

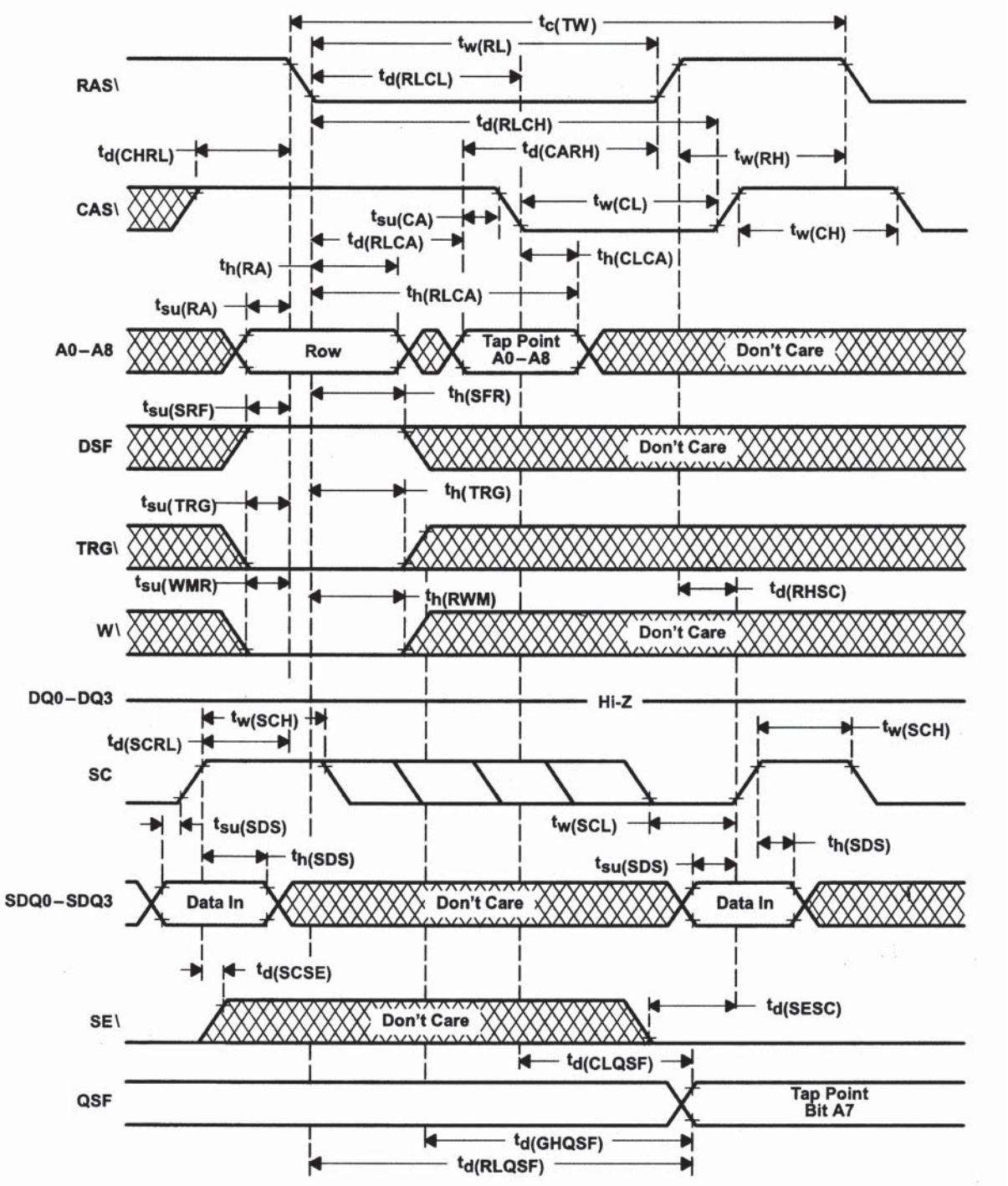
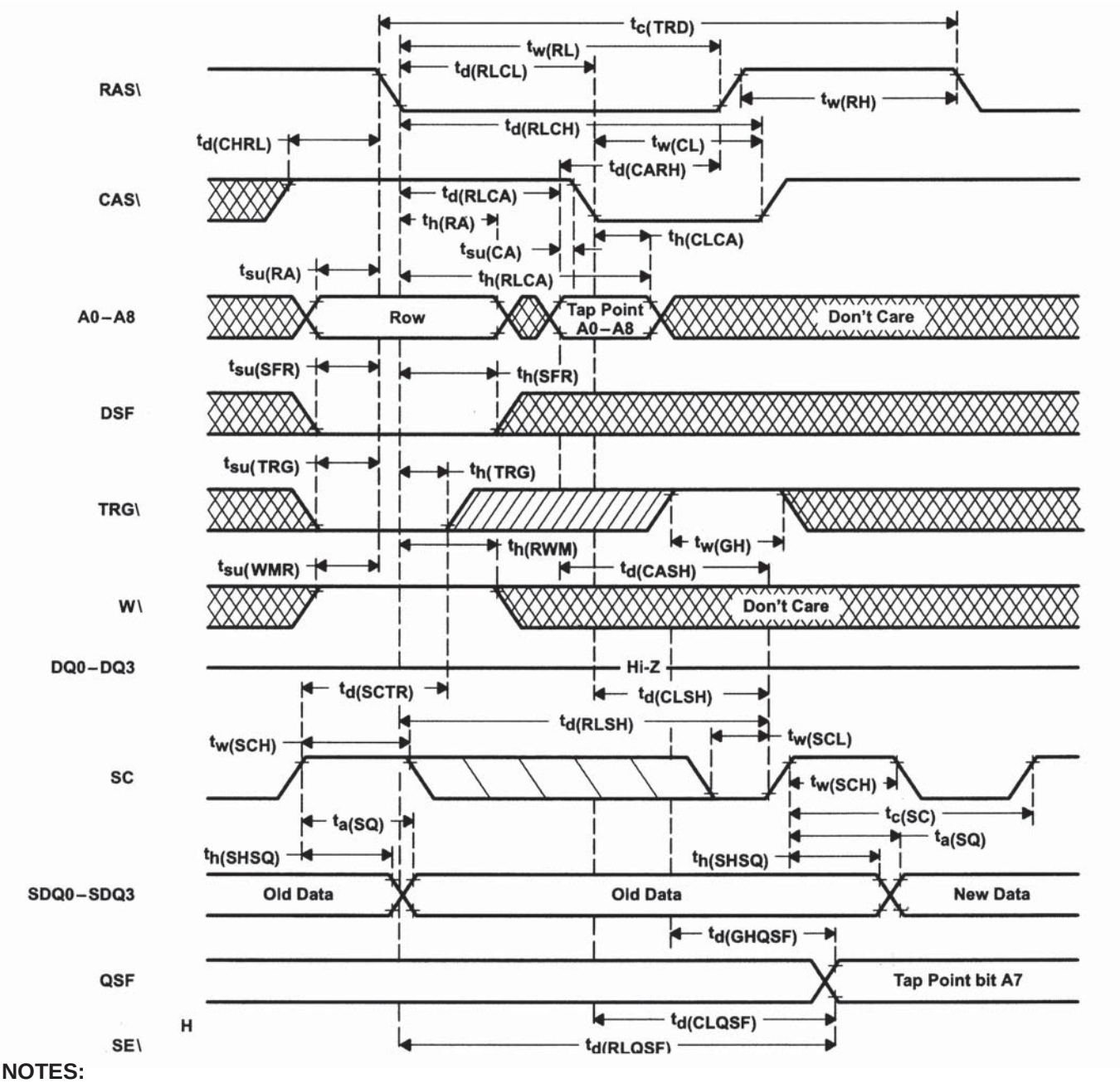


FIGURE 31: Memory-to-Data-Register Transfer-Cycle Timing, Early-Load Operation



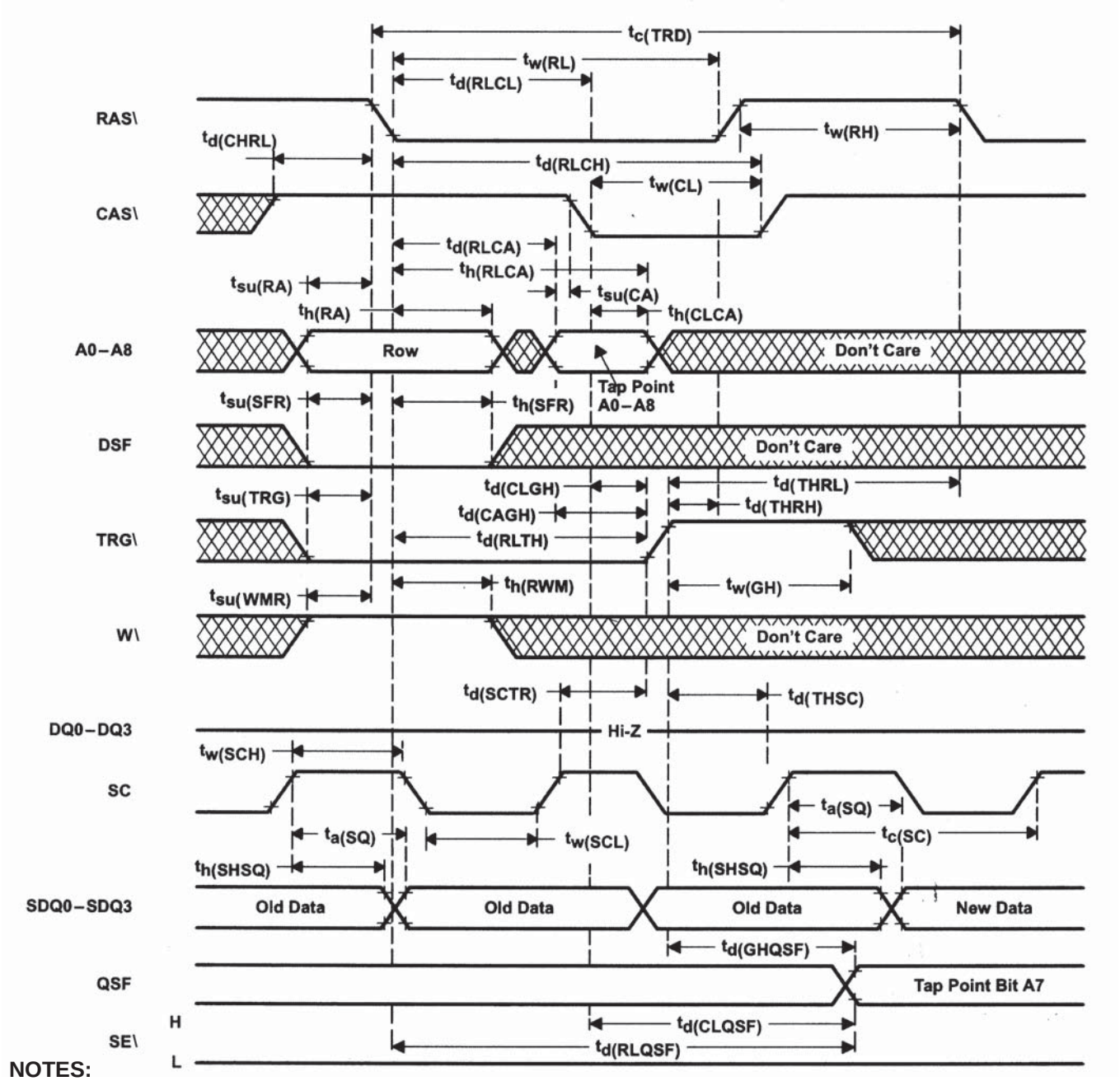
NOTES:

NOTE H: Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH}$) min.

NOTE I: DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written from the 512 corresponding columns of the selected row. The data that is transferred into the data registers can be either shifted out or transferred back into another row.

NOTE J: Once data is transferred into the data registers, the SAM is in the serial-read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after TRG\ has gone high must be activated by a positive transition of SC.

FIGURE 32: Memory-to-Data-Register Transfer-Cycle Timing, Real-Time-Reload Operation/Late-Load Operation



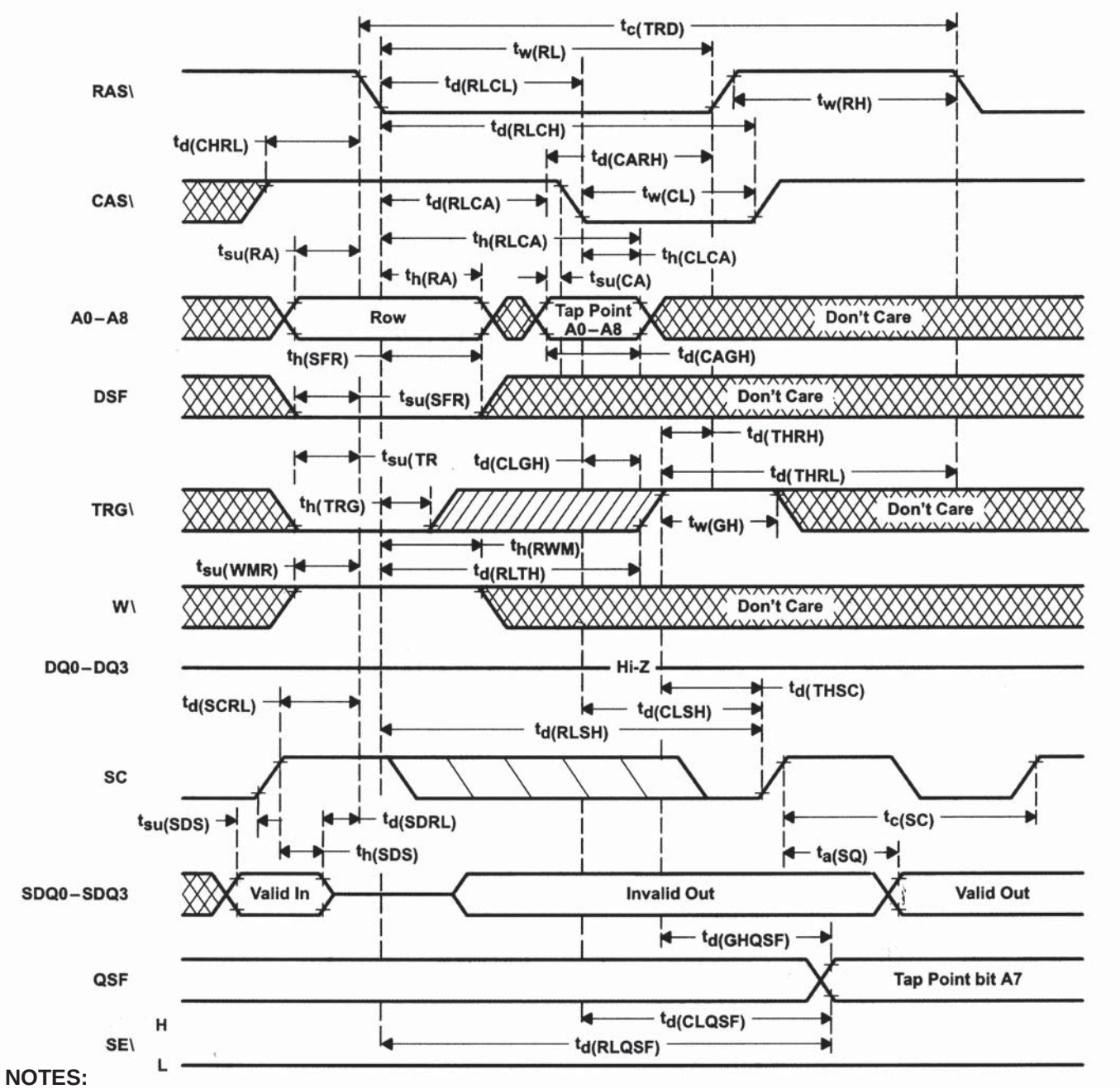
NOTES:

NOTE K: Late-load operation is defined as $t_{d(THRH)} < 0$ ns.

NOTE L: DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written from the 512 corresponding columns of the selected row. The data that is transferred into the data registers can be either shifted out or transferred back into another row.

NOTE M: Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after TRG\ has gone high must be activated by a positive transition of SC.

FIGURE 33: Memory-to-Data-Register Transfer-Cycle Timing, SDQ Ports Previously in Serial-Input Mode



NOTES:

NOTE N: Late-load operation is defined as $t_{d(THRH)} < 0$ ns.

NOTE O: DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

NOTE P: Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after TRG\ has gone high must be activated by a positive transition of SC.

FIGURE 34: Split-Register-Mode Read-Transfer-Cycle Timing

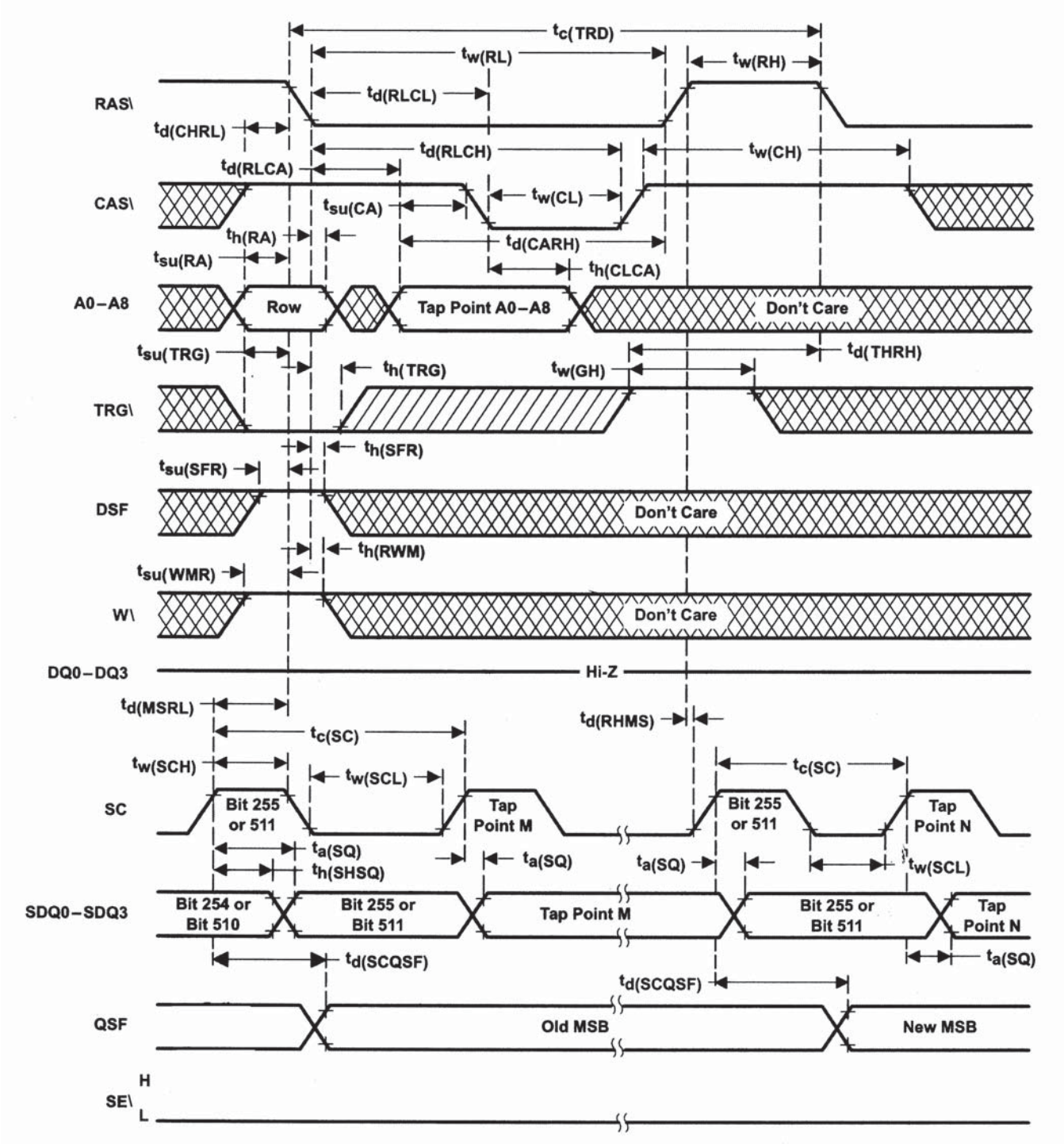
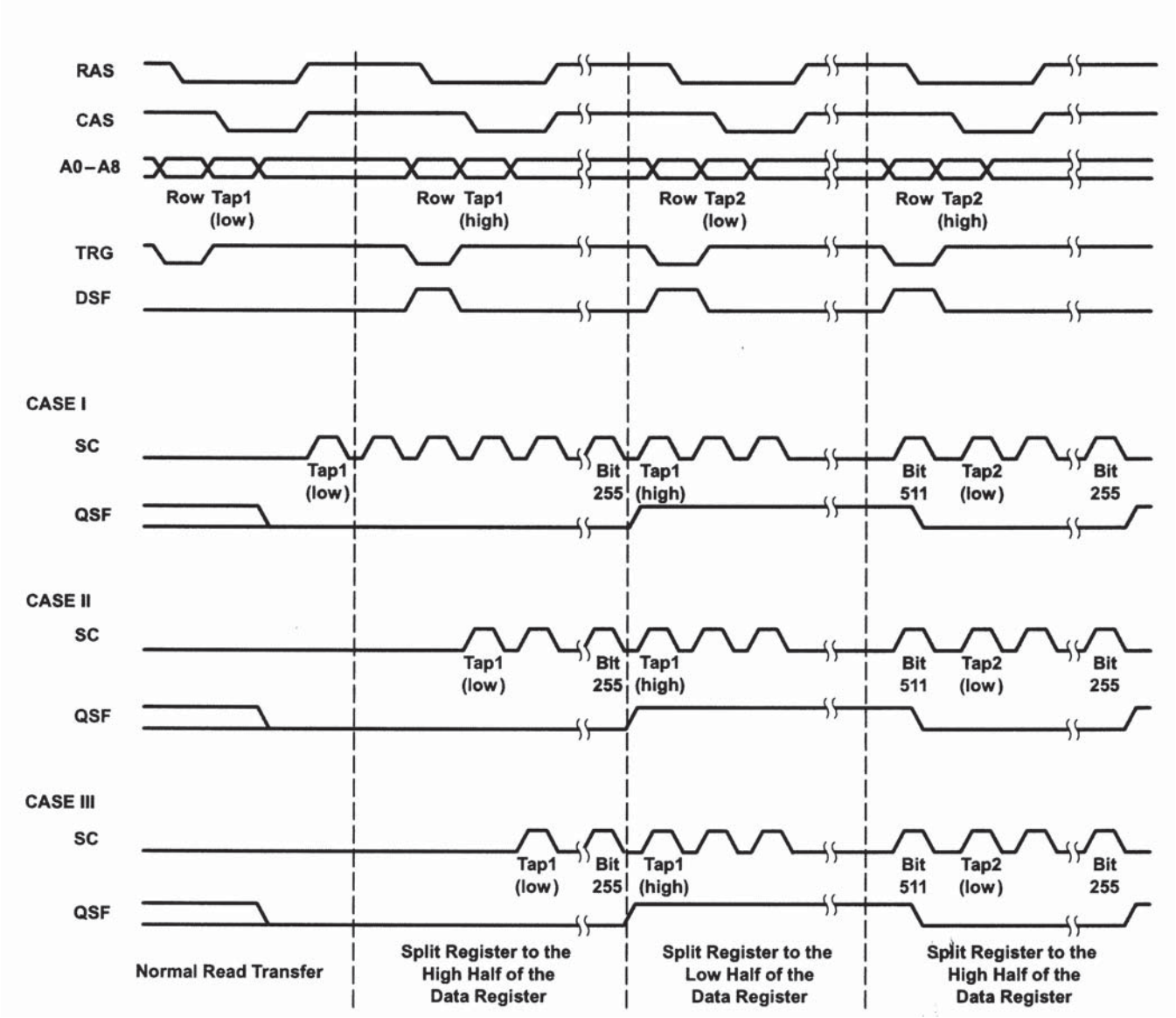


FIGURE 35: Split-Register-Transfer Operating Sequence

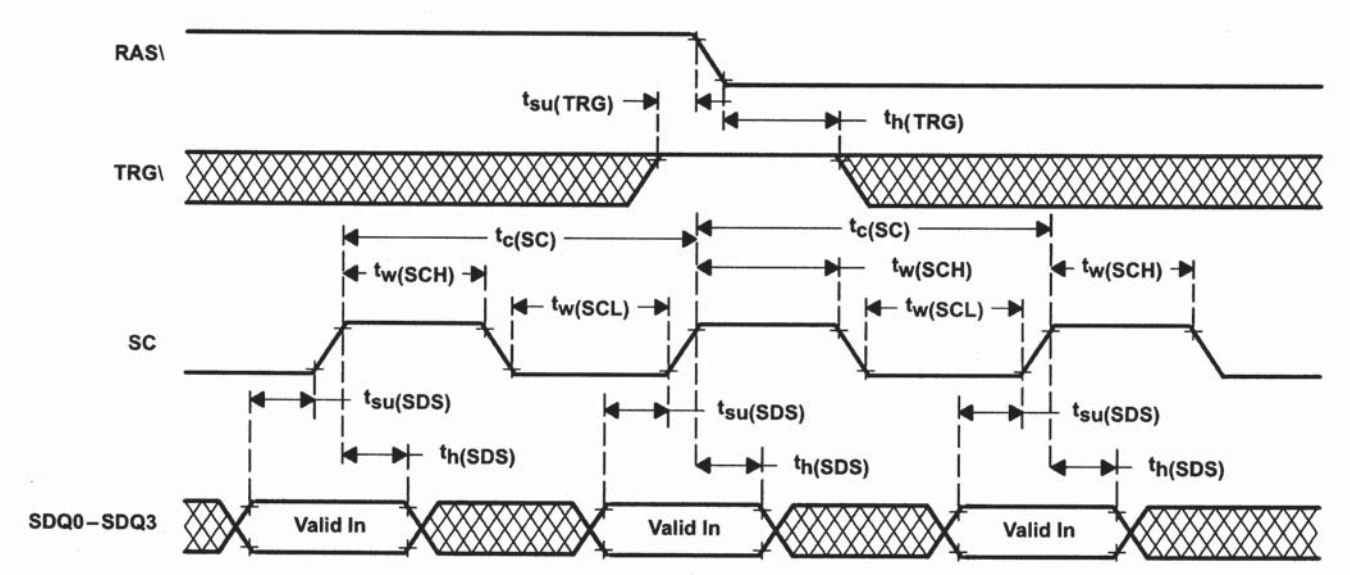


NOTES:

NOTE Q: In order to achieve proper split-register operation, a normal read transfer should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the normal read-transfer cycle (CASE I), during the first split-register cycle (CASE II), or even after the first split-register transfer cycle (CASE III). There is no minimum requirement of SC clock between the normal read-transfer cycle and the first split-register cycle.

NOTE R: A split register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 255 or 511) and the falling edge of RAS\ of the split-register transfer cycle into the inactive half. After $t_{d(MSRL)}$ is met, the split-register transfer into the inactive half must also satisfy the $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of RAS\ of the split-register transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 255 or 511). There is a minimum requirement of one rising edge of SC clock between two split-register transfer cycles.

FIGURE 36: Serial-Write-Cycle Timing (SE\ = V_{IL})

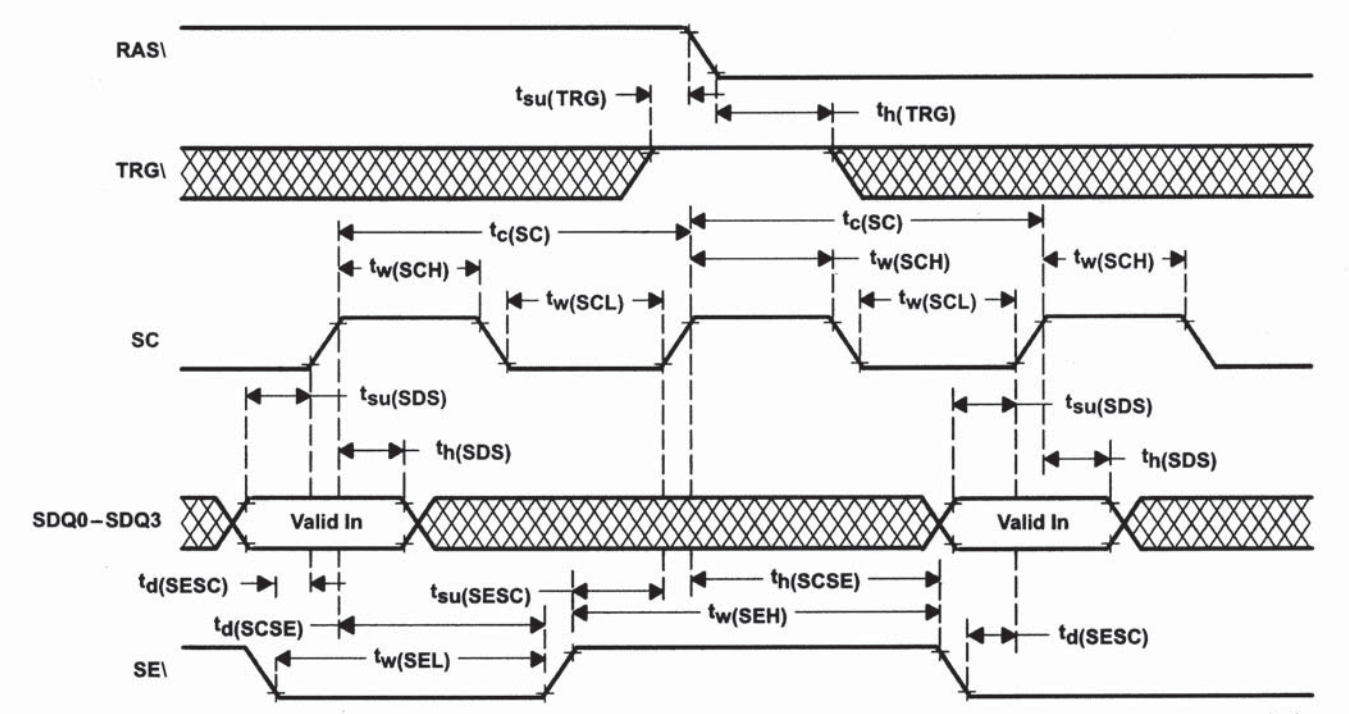


NOTES:

NOTE S: The serial data-in cycle is used to input serial data into the data registers. Before data can be written into the data registers via the SDQ terminals, the device must be put into the write mode by performing a write-mode-control (pseudo-transfer) cycle or any other write-transfer cycle. A read-transfer cycle is the only cycle that takes the serial port (SAM) out of the write mode and puts it into the read mode, disabling the input data. Data is written starting at the location specified by the input address loaded on the previous transfer cycle.

NOTE T: While accessing data in the serial-data registers, the state of TRG\ is a don't care as long as TRG\ is held high when RAS\ goes low to prevent data transfers between memory and data registers.

FIGURE 37: Serial-Write-Cycle Timing (SE\-Controlled Write)

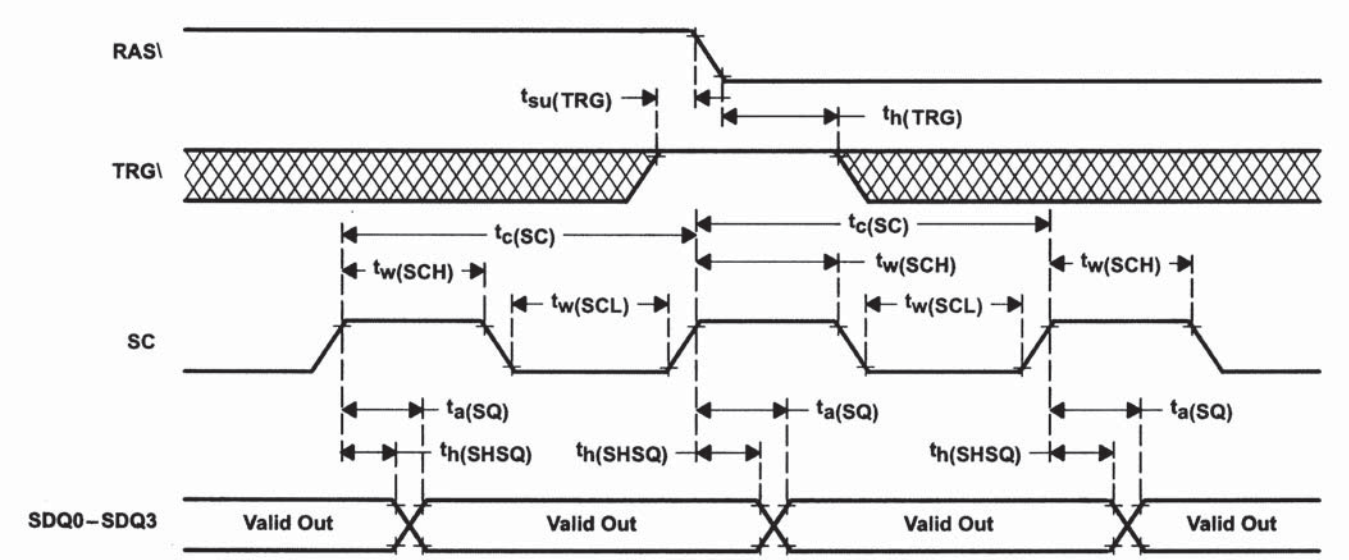


NOTES:

NOTE U: The serial data-in cycle is used to input serial data into the data registers. Before data can be written into the data registers via the SDQ terminals, the device must be put into the write mode by performing a write-mode-control (pseudo-transfer) cycle or any other write-transfer cycle. A read-transfer cycle is the only cycle that takes the serial port (SAM) out of the write mode and puts it into the read mode, disabling the input data. Data is written starting at the location specified by the input address loaded on the previous transfer cycle.

NOTE V: While accessing data in the serial-data registers, the state of TRG\ is a don't care as long as TRG\ is held high when RAS\ goes low to prevent data transfers between memory and data registers.

FIGURE 38: Serial-Read-Cycle Timing (SE\ = V_{IL})

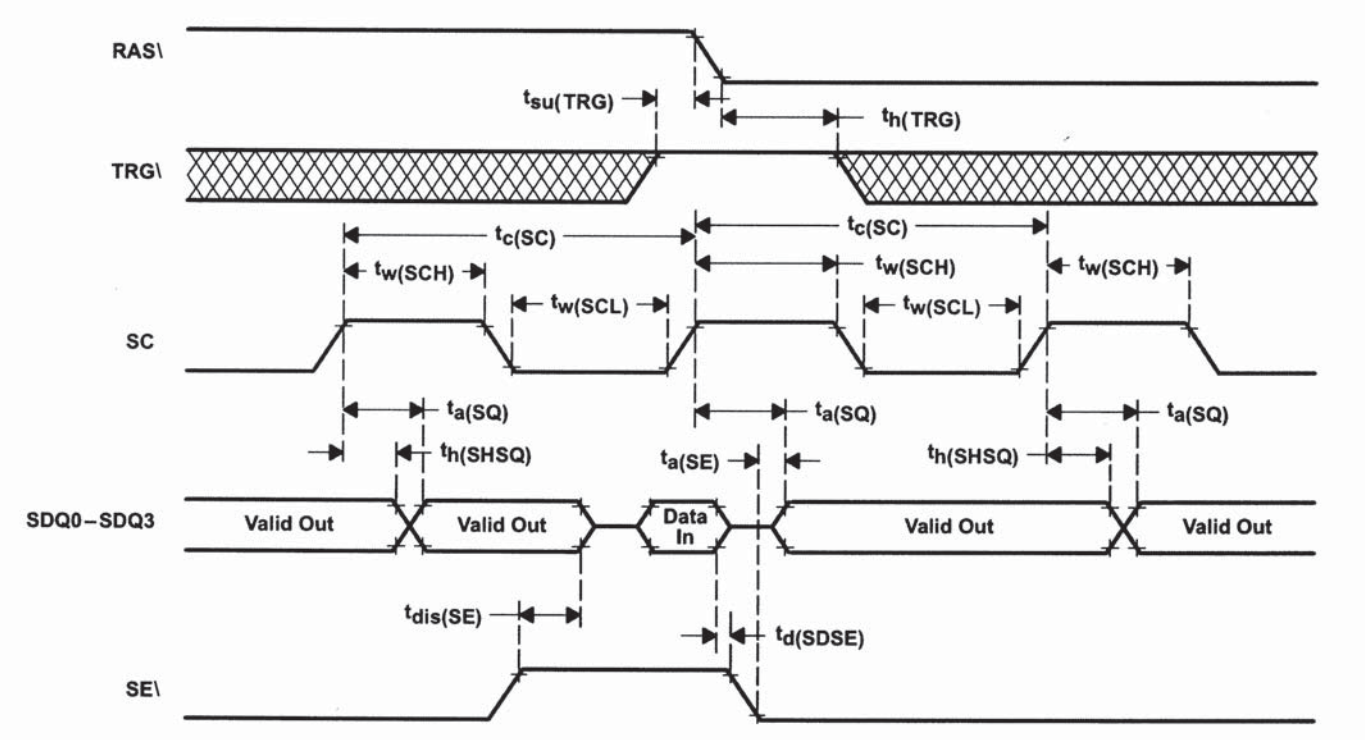


NOTES:

NOTE W: While reading data through the serial-data register, the state of TRG\ is a don't care as long as TRG\ is held high when RAS\ goes low. This is to avoid the initiation of a register-to-memory-to-register data-transfer operation.

NOTE X: The serial data-out cycle is used to read data out of the data registers. Before data can be read via SDQ, the device must be put into the read mode by performing a transfer-read cycle. Any transfer-write cycles occurring between the transfer-read cycle and the subsequent shifting out of data take the device out of the read mode and put it in the write mode, not allowing the reading of data.

FIGURE 39: Serial-Read-Cycle Timing (SE\-Controlled Read)



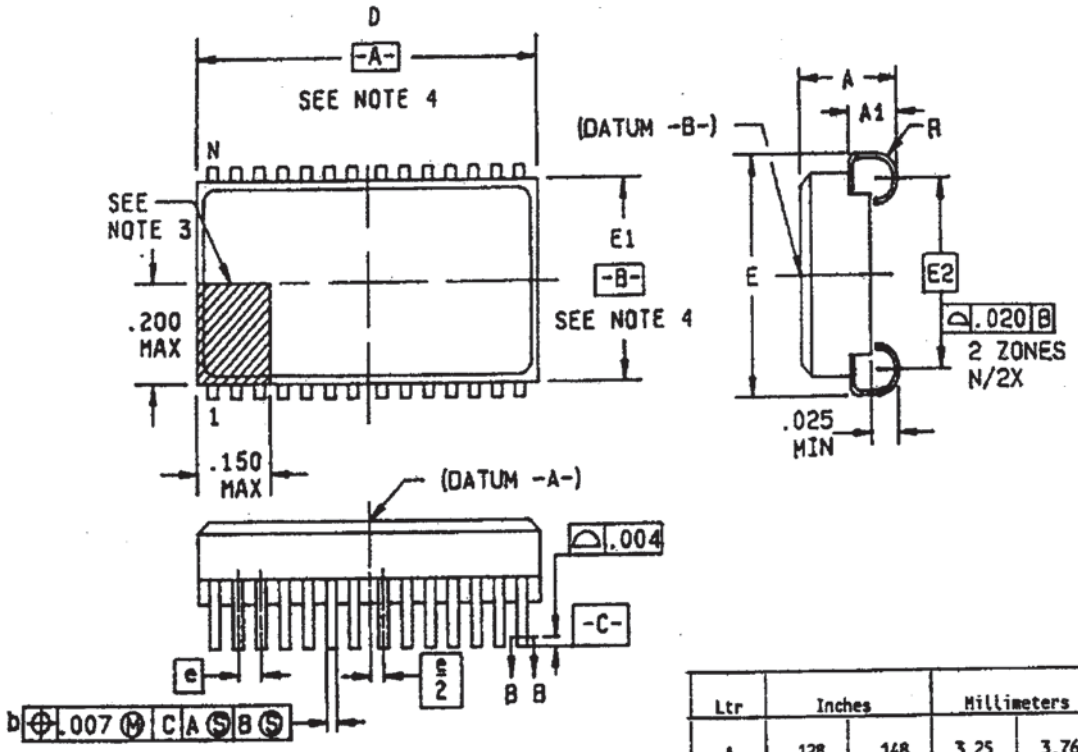
NOTES:

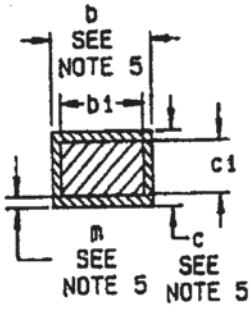
NOTE Y: While reading data through the serial-data register, the state of TRG\ is a don't care as long as TRG\ is held high when RAS\ goes low. This is to avoid the initiation of a register-to-memory-to-register data-transfer operation.

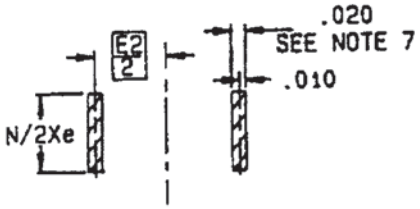
NOTE Z: The serial data-out cycle is used to read data out of the data registers. Before data can be read via SDQ, the device must be put into the read mode by performing a transfer-read cycle. Any transfer-write cycles occurring between the transfer-read cycle and the subsequent shifting out of data take the device out of the read mode and put it in the write mode, not allowing the reading of data.

MECHANICAL DEFINITIONS*

Micross Case #500 (Package Designator DCJ)
SMD 5962-89497, Case Outline T







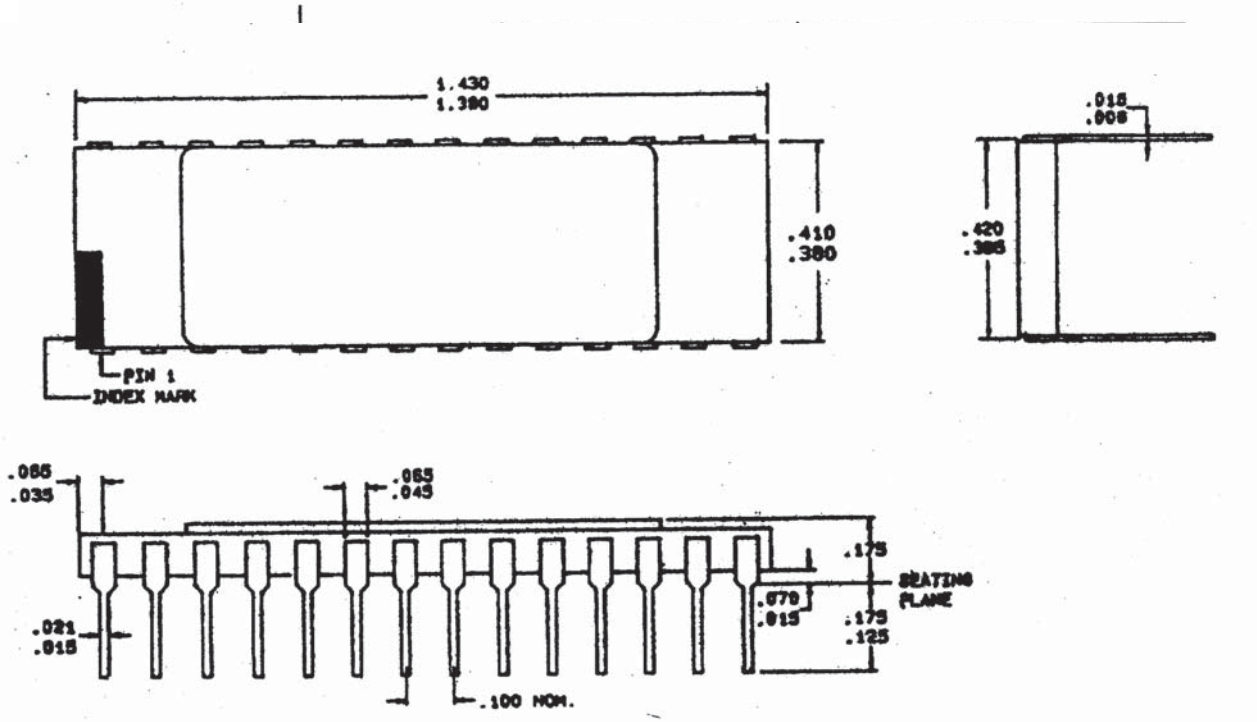
Inches	mm
.004	0.10
.007	0.18
.010	0.25
.020	0.51
.025	0.64
.150	3.81
.200	5.08

Ltr	Inches		Millimeters	
A	.128	.148	3.25	3.76
A1	.055	.075	1.40	1.91
b	.015	.022	0.38	0.56
b1	.015	.019	0.38	0.48
c	.004	.009	0.10	0.23
c1	.004	.006	0.10	0.15
D	.710	.730	18.03	18.54
e	.050 BSC		1.27	1.27
E	.435	.445	11.05	11.30
E1	.405	.415	10.29	10.54
E2	.370 BSC		9.40	9.40
m	.0002	.0015	0.005	0.038
N	28			
R	.030	.040	0.76	1.01

All measurements are in inches.

MECHANICAL DEFINITIONS*

Micross Case #109 (Package Designator C or JDM)
SMD 5962-89497, Case Outline X

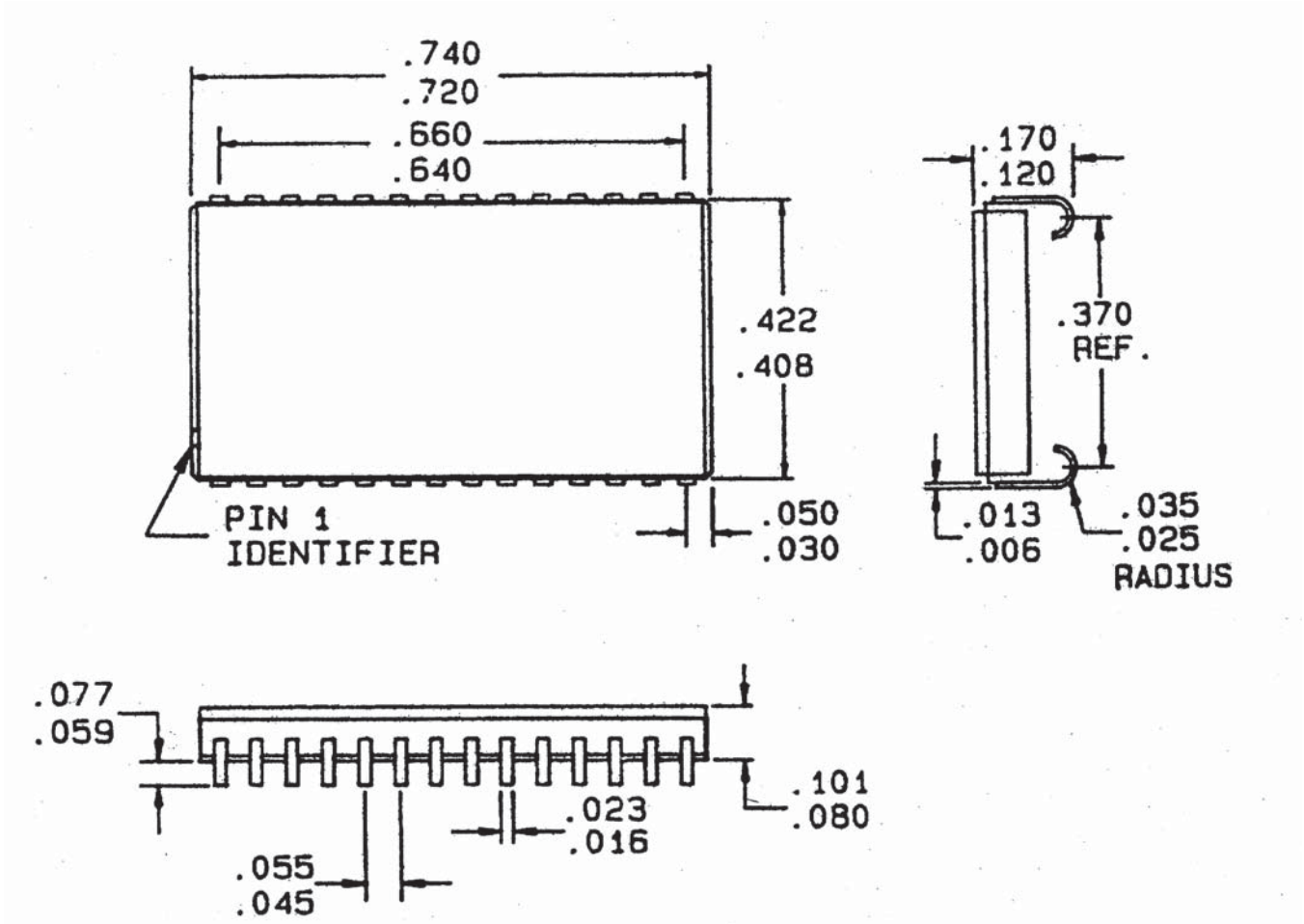


Inches	mm	Inches	mm
.008	0.20	.125	3.18
.015	0.38	.175	4.45
.021	0.53	.380	9.65
.035	0.89	.385	9.79
.045	1.14	.410	10.41
.065	1.65	.420	10.67
.070	1.78	1.380	35.05
.100	2.54	1.430	36.32

All measurements are in inches.

MECHANICAL DEFINITIONS*

Package Designator HJM
SMD 5962-89497, Case Outline Y

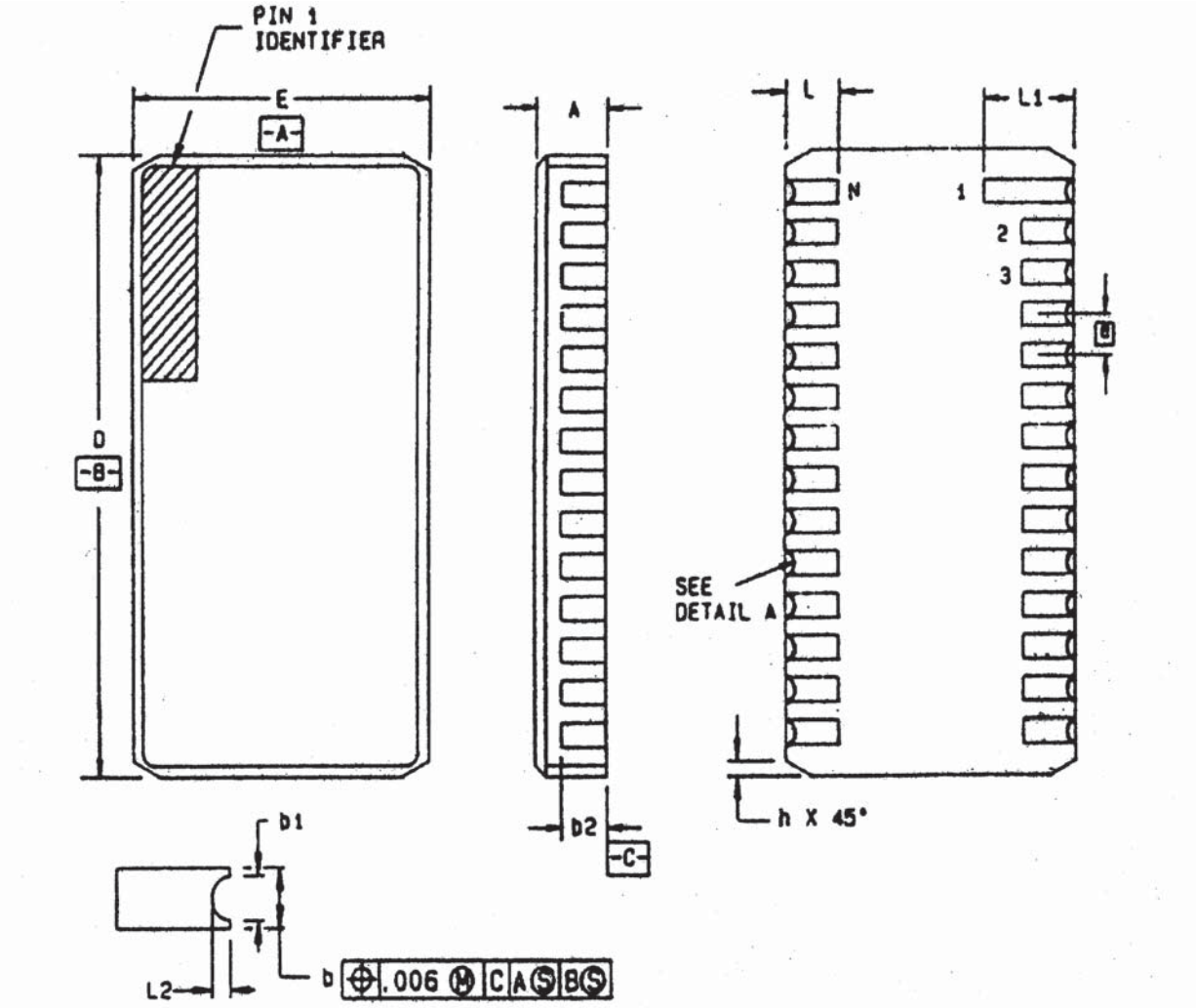


Inches	mm	Inches	mm
.006	0.152	.077	1.778
.013	0.330	.080	2.032
.016	0.406	.101	2.565
.023	0.584	.139	3.513
.025	0.635	.170	4.318
.030	0.762	.370	9.398
.035	0.889	.408	10.636
.045	1.143	.422	10.719
.050	1.270	.640	16.256
.055	1.397	.660	16.764
.059	1.498	.720	18.288
		.740	18.796

All measurements are in inches.

MECHANICAL DEFINITIONS*

Micross Case #203 (Package Designator EC or HMM)
SMD 5962-89497, Case Outline Z

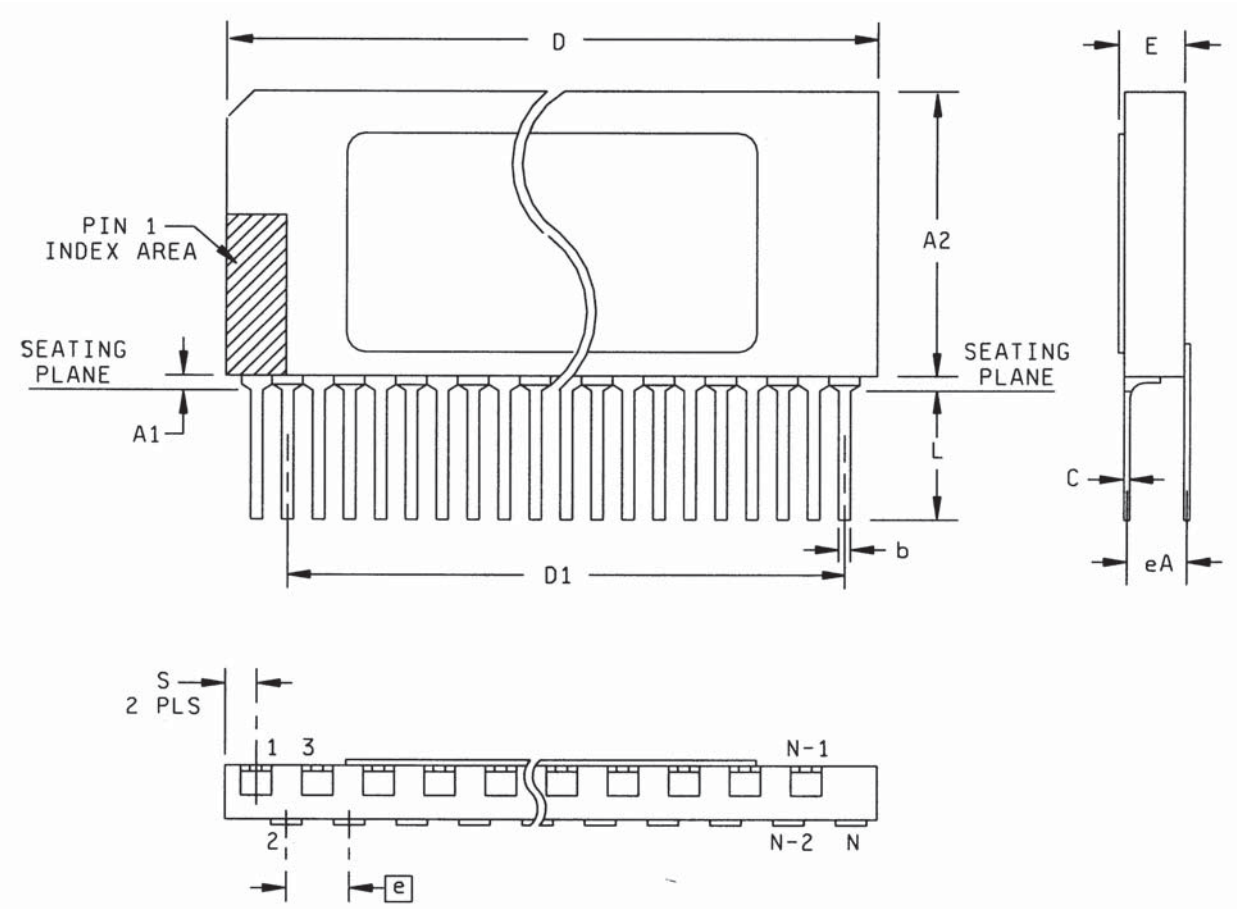


Ltr	Dimensions				Ltr	Dimensions			
	Inches		Millimeters			Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.080	.100	2.03	2.54	e	.050 BSC		1.27	
b	.022	.028	0.56	0.71	h	.012 REF		0.30	
b1	.006	.022	0.15	0.56	L	.070	.080	1.78	2.03
b2	.040		1.02		L1	.090	.110	2.29	2.79
D	.700	.740	17.78	18.80	L2	.003	.015	0.08	0.38
E	.392	.408	9.96	10.36	N	28 terminals			

All measurements are in inches.

MECHANICAL DEFINITIONS*

Package Designator CZ or SVM
SMD 5962-89497, Case Outline M

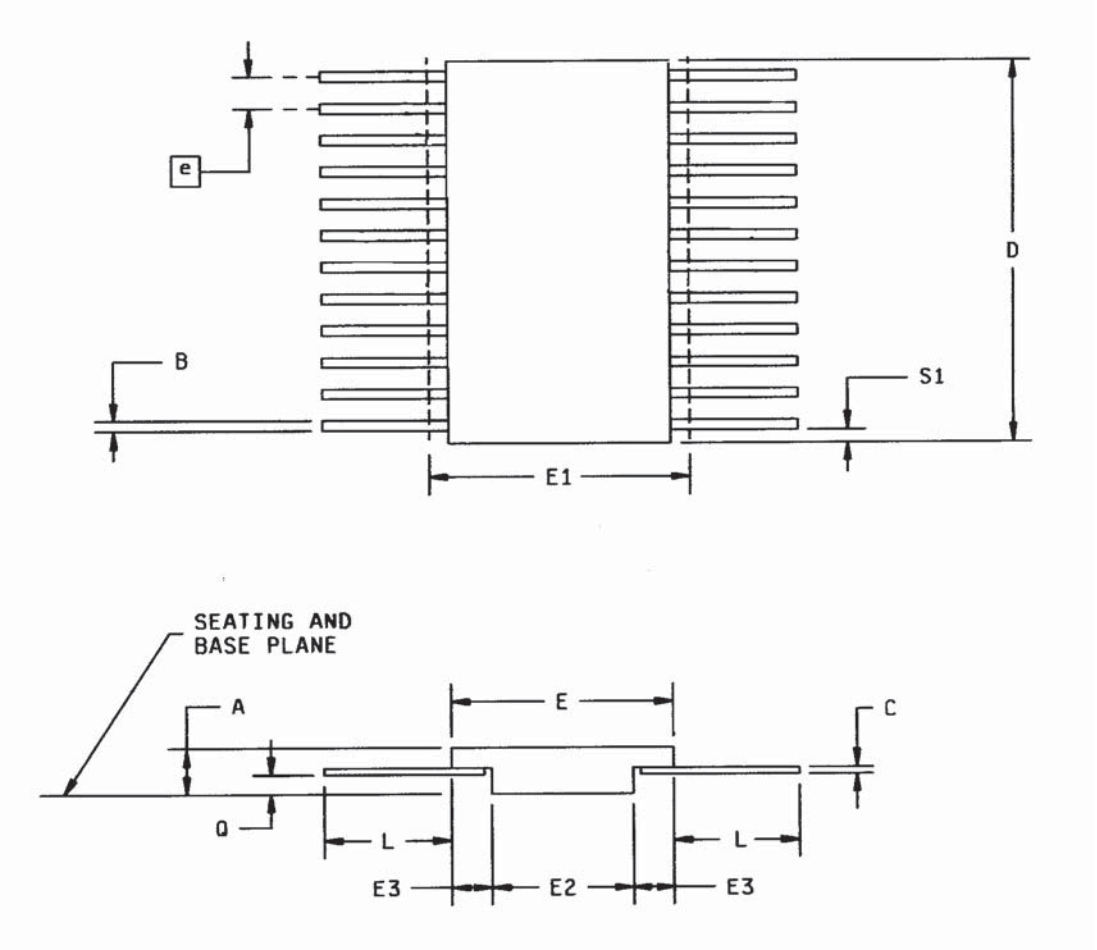


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A1	0.38	1.27	.015	.050
A2	11.18	11.81	.440	.465
b	0.41	0.58	.016	.023
c	0.20	0.39	.008	.015
D	36.45	37.21	1.435	1.465
D1	32.77	33.27	1.290	1.310
e	2.54 BSC		.100 BSC	
eA	2.16	2.92	.085	.115
E	2.54	3.30	.100	.130
L	3.18	5.08	.125	.200
S	0.88	1.65	.035	.065

All measurements are in inches.

MECHANICAL DEFINITIONS*

Micross Case #302 (Package Designator F)
SMD 5962-89497, Case Outline U



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.090	0.130
b	0.015	0.022
c	0.004	0.009
D	---	0.740
E	0.380	0.420
E1	---	0.440
E2	0.180	---
E3	0.030	---
e	0.050 BSC	
L	0.250	0.370
Q	0.026	0.045
S1	0.000	---

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: MT42C4256DCJ-12/883C

Device Number	Package Type	Speed ns	Process
MT42C4256	DCJ	-10	/*
MT42C4256	DCJ	-12	/*

EXAMPLE: MT42C4256C-12/IT

Device Number	Package Type	Speed ns	Process
MT42C4256	C	-10	/*
MT42C4256	C	-12	/*

EXAMPLE: MT42C4256CZ-12/883C

Device Number	Package Type	Speed ns	Process
MT42C4256	CZ	-10	/*
MT42C4256	CZ	-12	/*

EXAMPLE: MT42C4256F-12/IT

Device Number	Package Type	Speed ns	Process
MT42C4256	F	-10	/*
MT42C4256	F	-12	/*

EXAMPLE: MT42C4256EC-10/883C

Device Number	Package Type	Speed ns	Process
MT42C4256	EC	-10	/*
MT42C4256	EC	-12	/*

EXAMPLE: SMJ44C251B 10HJM

Device Number	Speed ns	Package Type	Process
SMJ44C251B	10	HJM	See Note
SMJ44C251B	12	HJM	See Note

EXAMPLE: SMJ44C251B 12JDM

Device Number	Speed ns	Package Type	Process
SMJ44C251B	10	JDM	See Note
SMJ44C251B	12	JDM	See Note

EXAMPLE: SMJ44C251B 12HMM

Device Number	Speed ns	Package Type	Process
SMJ44C251B	10	HMM	See Note
SMJ44C251B	12	HMM	See Note

EXAMPLE: SMJ44C251B 10SVM

Device Number	Speed ns	Package Type	Process
SMJ44C251B	10	SVM	See Note
SMJ44C251B	12	SVM	See Note

***OPERATING TEMPERATURE**

XT = Military Temperature Range -55°C to +125°C
IT = Industrial Temperature Range -40°C to +85°C
883C = MIL-STD-883C process -55°C to +125°C

NOTE: SMJ prefix denotes MIL-STD-883C process, temperature range -55°C to +125°C.

MICROSS TO DSCC PART NUMBER CROSS REFERENCE*

Package Designator C or JDM

Micross Part Number	SMD Part Number
MT42C4256C-10/883C	5962-8949704MXA
MT42C4256C-12/883C	5962-8949703MXA
SMJ44C251B-10JDM**	5962-8949704MXA
SMJ44C251B-12JDM**	5962-8949703MXA

Package Designator CZ or SVM

Micross Part Number	SMD Part Number
MT42C4256CZ-10/883C	5962-8949704MMA
MT42C4256CZ-12/883C	5962-8949703MMA
SMJ44C251B-10SVM**	5962-8949704MMA
SMJ44C251B-12SVM**	5962-8949703MMA

Package Designator EC or HMM

Micross Part Number	SMD Part Number
MT42C4256EC-10/883C	5962-8949704MZA
MT42C4256EC-12/883C	5962-8949703MZA
SMJ44C251B-10HMM**	5962-8949704MZA
SMJ44C251B-12HMM**	5962-8949703MZA

Package Designator DCJ

Micross Part Number	SMD Part Number
MT42C4256DCJ-10/883C	5962-8949704MYA
MT42C4256DCJ-12/883C	5962-8949703MYA

Package Designator F

Micross Part Number	SMD Part Number
MT42C4256F-10/883C	5962-8949704MYA
MT42C4256F-12/883C	5962-8949703MYA

Package Designator HJM

Micross Part Number	SMD Part Number
SMJ44C251B-10HJM**	5962-8949704MYA
SMJ44C251B-12HJM**	5962-8949703MYA

** Micross part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*
*** Parts are listed on SMD under the old Texas Instruments part number. Micross purchased this product line in November of 1999.*

DOCUMENT TITLE

128 Mb: 8 Meg x 16 SDRAM Synchronous DRAM Memory

Rev #	History	Release Date	Status
0.5	Removed F & DCJ package- pg 1, 56, 57 Deleted package diagrams (old page 50 & 55)	April 2010	Release
0.6	Added F & DCJ package information back into datasheet	June 2010	Release