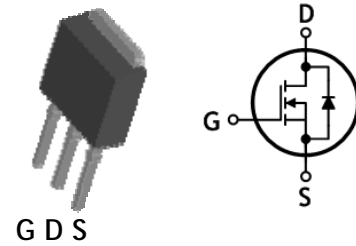


## 200V LOGIC N-Channel MOSFET

### Features

- Drain-Source breakdown voltage:  $BV_{DSS}=200V$  (Min.)
- Low gate charge:  $Q_g=4nC$  (Typ.)
- Low drain-source On-Resistance:  $R_{DS(on)}=1.35\Omega$  (Max.)
- 100% avalanche tested
- RoHS compliant device

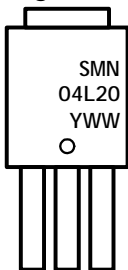


### Ordering Information

Part Number	Marking	Package
SMN04L20IS	SMN04L20	I-PAK (Short Lead)

I-PAK

### Marking Information



Column 1, 2: Device Code  
 Column 3: Production Information  
 e.g.) YWW  
 -. Y: Year Code  
 -. WW: Week Code

### Absolute maximum ratings ( $T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	200	V	
Gate-source voltage	$V_{GSS}$	$\pm 20$	V	
Drain current (DC) *	$I_D$	$T_c=25^\circ C$	3.2	A
		$T_c=100^\circ C$	2.02	A
Drain current (Pulsed) *	$I_{DM}$	12.8	A	
Avalanche current <sup>(Note 2)</sup>	$I_{AS}$	2.5	A	
Single pulsed avalanche energy <sup>(Note 2)</sup>	$E_{AS}$	52	mJ	
Repetitive avalanche current <sup>(Note 1)</sup>	$I_{AR}$	2.5	A	
Repetitive avalanche energy <sup>(Note 1)</sup>	$E_{AR}$	3.3	mJ	
Power dissipation	$P_D$	33	W	
Junction temperature	$T_J$	150	$^\circ C$	
Storage temperature range	$T_{stg}$	-55-150	$^\circ C$	

\* Limited only maximum junction temperature

## Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 3.78	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 50	

Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0$	200	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$ , $V_{DS}=V_{GS}$	1	1.75	2.25	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=200\text{V}$ , $V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=1.6\text{A}$	-	1.1	1.35	$\Omega$
		$V_{GS}=5\text{V}$ , $I_D=1.6\text{A}$	-	1.13	1.4	$\Omega$
Forward transfer conductance (Note 3)	$g_{fs}$	$V_{DS}=10\text{V}$ , $I_D=1.6\text{A}$	-	3	-	S
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$	-	224	302	pF
Output capacitance	$C_{oss}$		-	38	51	
Reverse transfer capacitance	$C_{rss}$		-	6.2	10	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=100\text{V}$ , $I_D=3.2\text{A}$ $R_G=25\Omega$	-	23	51	ns
Rise time (Note 3,4)	$t_r$		-	85	177	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	80	169	
Fall time (Note 3,4)	$t_f$		-	32	68	
Total gate charge (Note 3,4)	$Q_g$	$V_{DS}=160\text{V}$ , $V_{GS}=10\text{V}$ $I_D=3.2\text{A}$	-	4	5	nC
Gate-source charge (Note 3,4)	$Q_{gs}$		-	1.4	-	
Gate-drain charge (Note 3,4)	$Q_{gd}$		-	0.6	-	

Source-Drain Diode Ratings and Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	3.2	A
Source current (Pulsed)	$I_{SM}$		-	-	12.8	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}$ , $I_S=3.2\text{A}$	-	-	1.5	V
Reverse recovery time (Note 3,4)	$t_{rr}$	$I_S=3.2\text{A}$ , $V_{GS}=0\text{V}$ $di_f/dt=100\text{A}/\mu\text{s}$	-	90	-	ns
Reverse recovery charge (Note 3,4)	$Q_{rr}$		-	0.29	-	$\mu\text{C}$

## Note:

1. Repeated rating: Pulse width limited by safe operating area
2.  $L=7.6\text{mH}$ ,  $I_{AS}=3.2\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycles  $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Typical Electrical Characteristics Curves

Fig. 1  $I_D - V_{DS}$

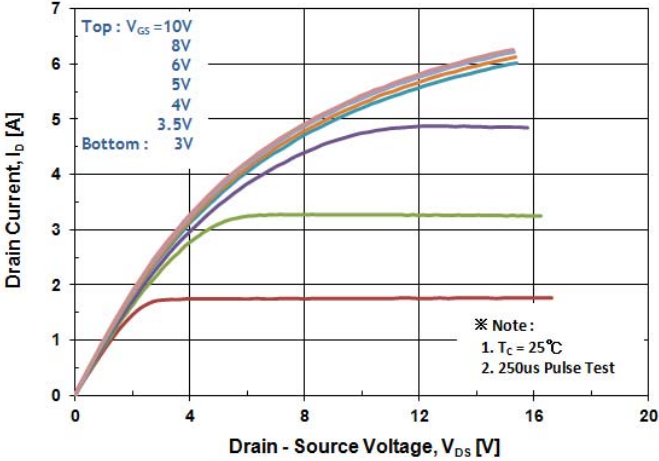


Fig. 2  $I_D - V_{GS}$

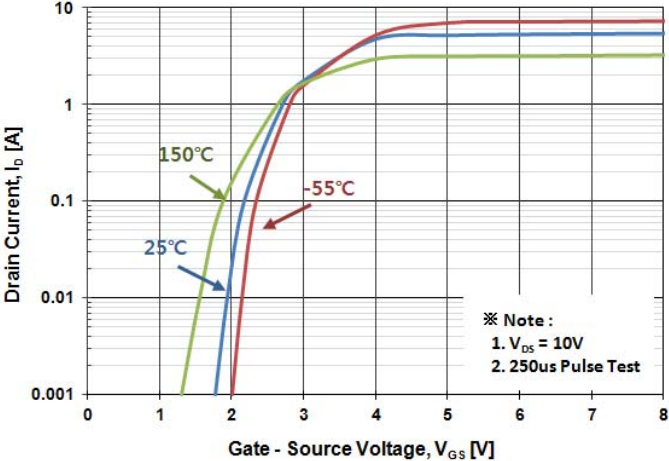


Fig. 3  $R_{DS(ON)} - I_D$

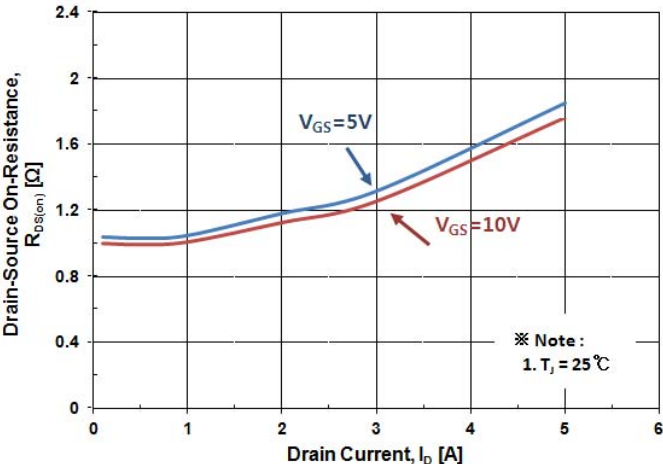


Fig. 4  $I_S - V_{SD}$

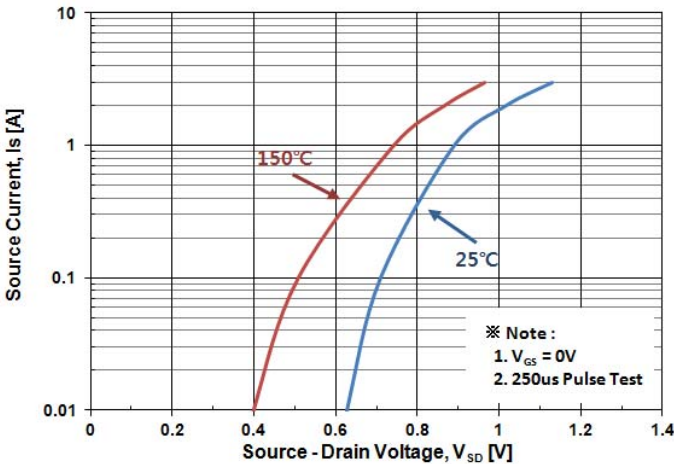


Fig. 5 Capacitance -  $V_{DS}$

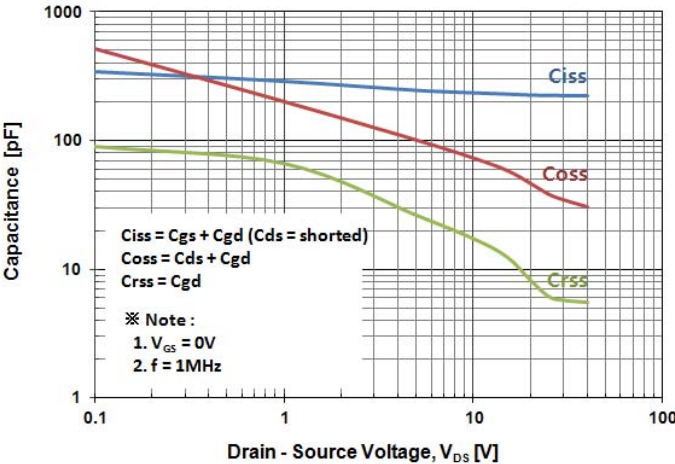


Fig. 6  $V_{GS} - Q_G$

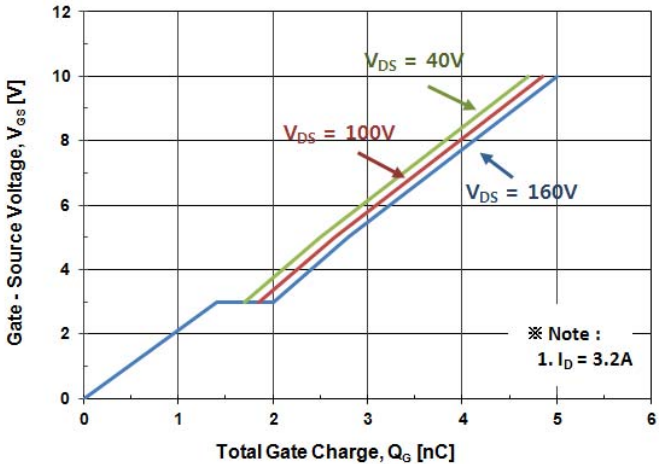


Fig. 7  $BV_{DSS} - T_J$

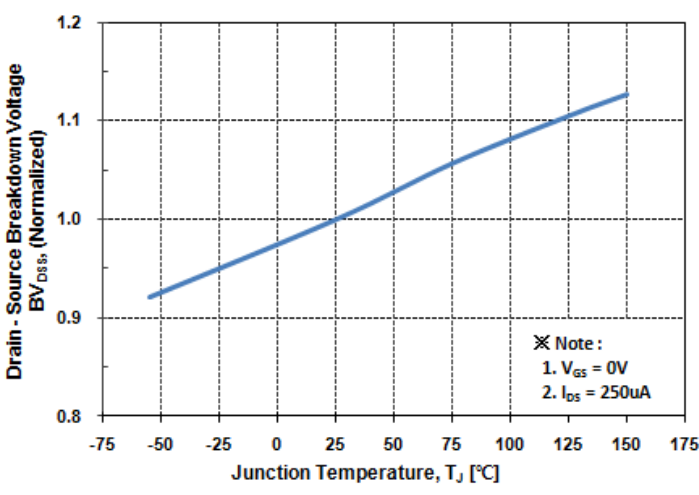


Fig. 8  $R_{DS(on)} - T_J$

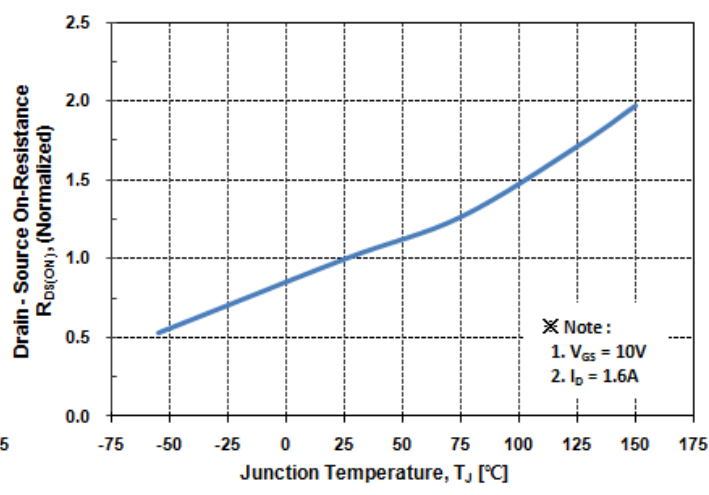


Fig. 9  $I_D - T_C$

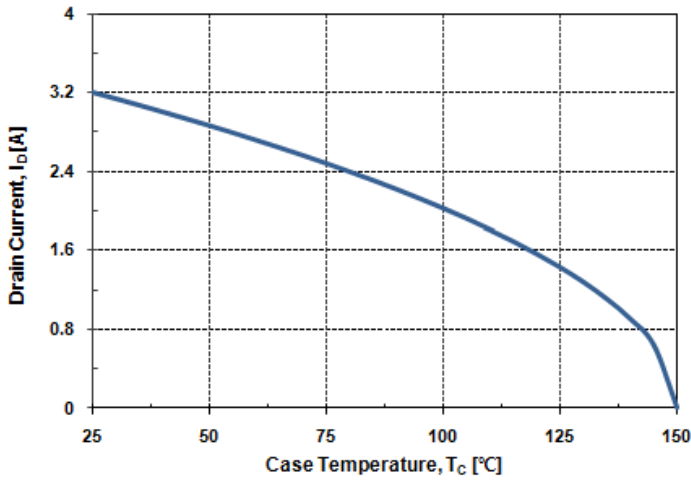


Fig. 10 Safe Operating Area

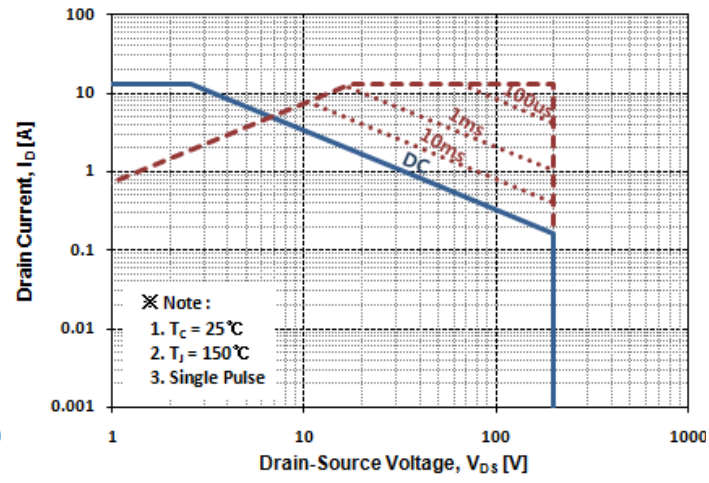


Fig. 11 Transient Thermal Impedance

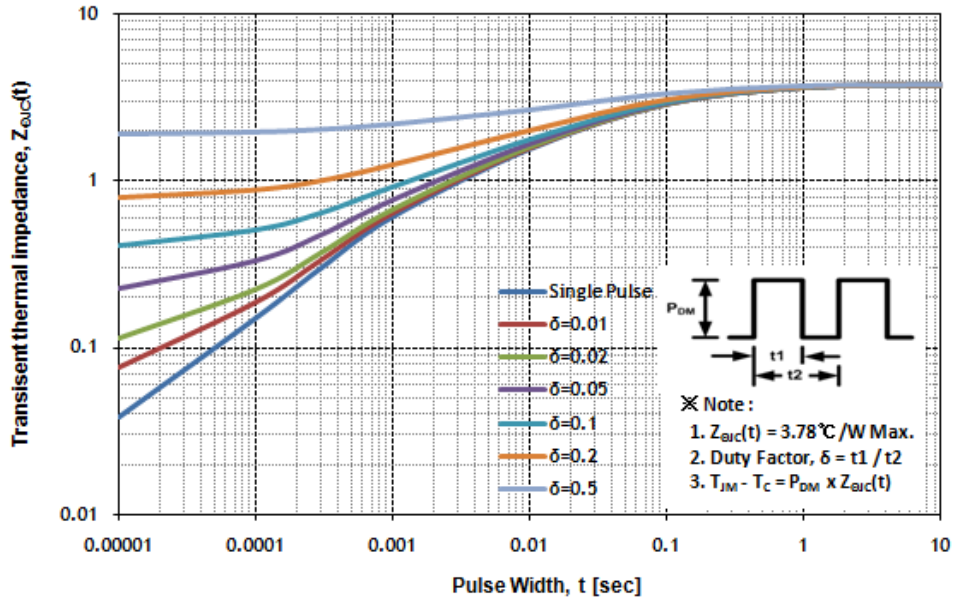


Fig. 12 Gate Charge Test Circuit & Waveform

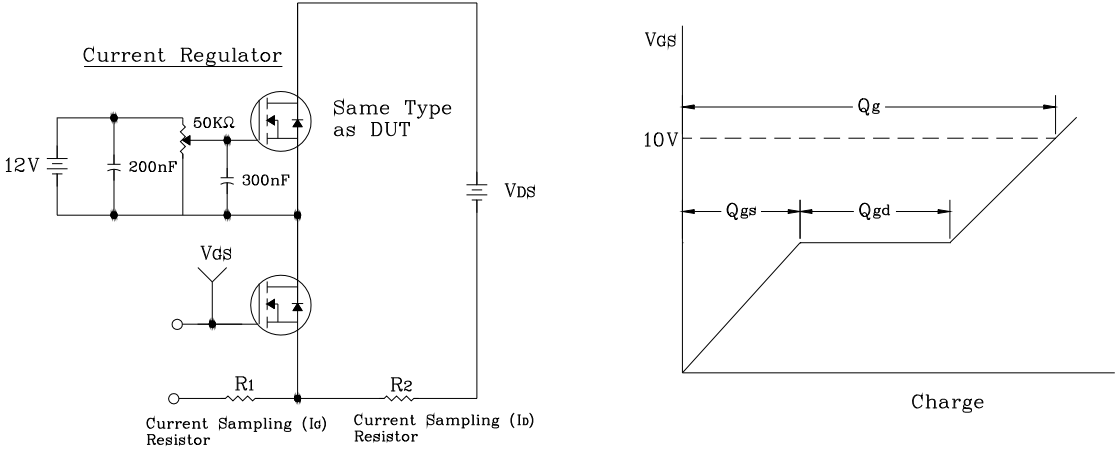


Fig. 13 Resistive Switching Test Circuit & Waveform

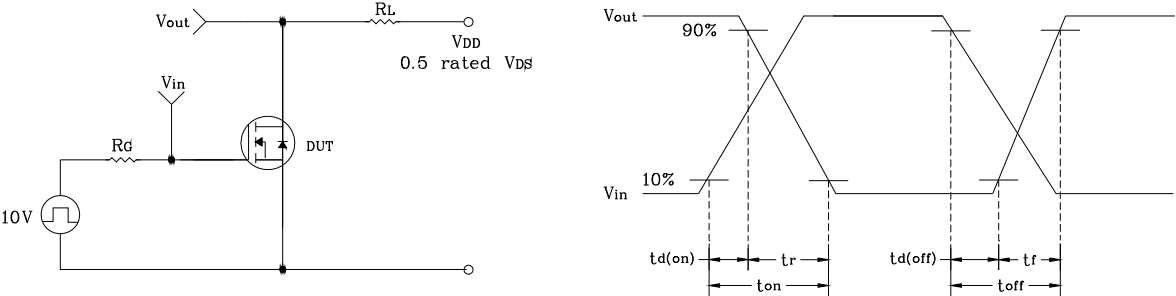


Fig. 14 E<sub>AS</sub> Test Circuit & Waveform

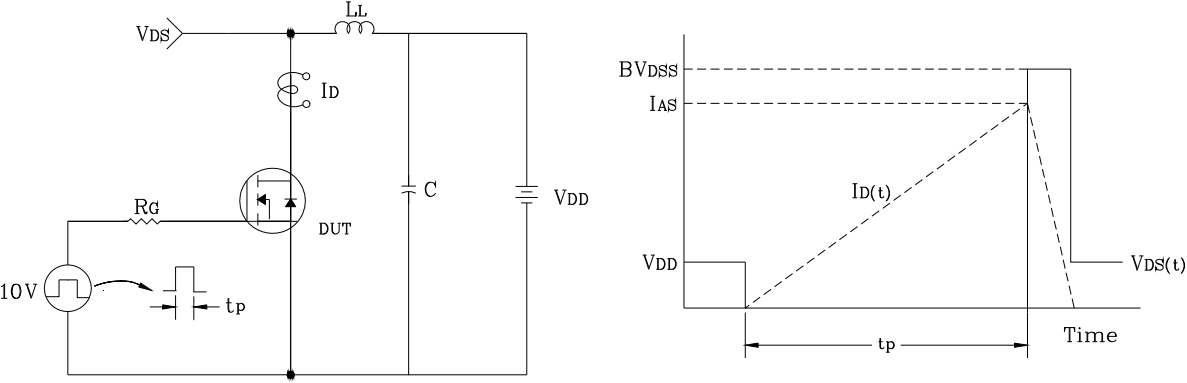
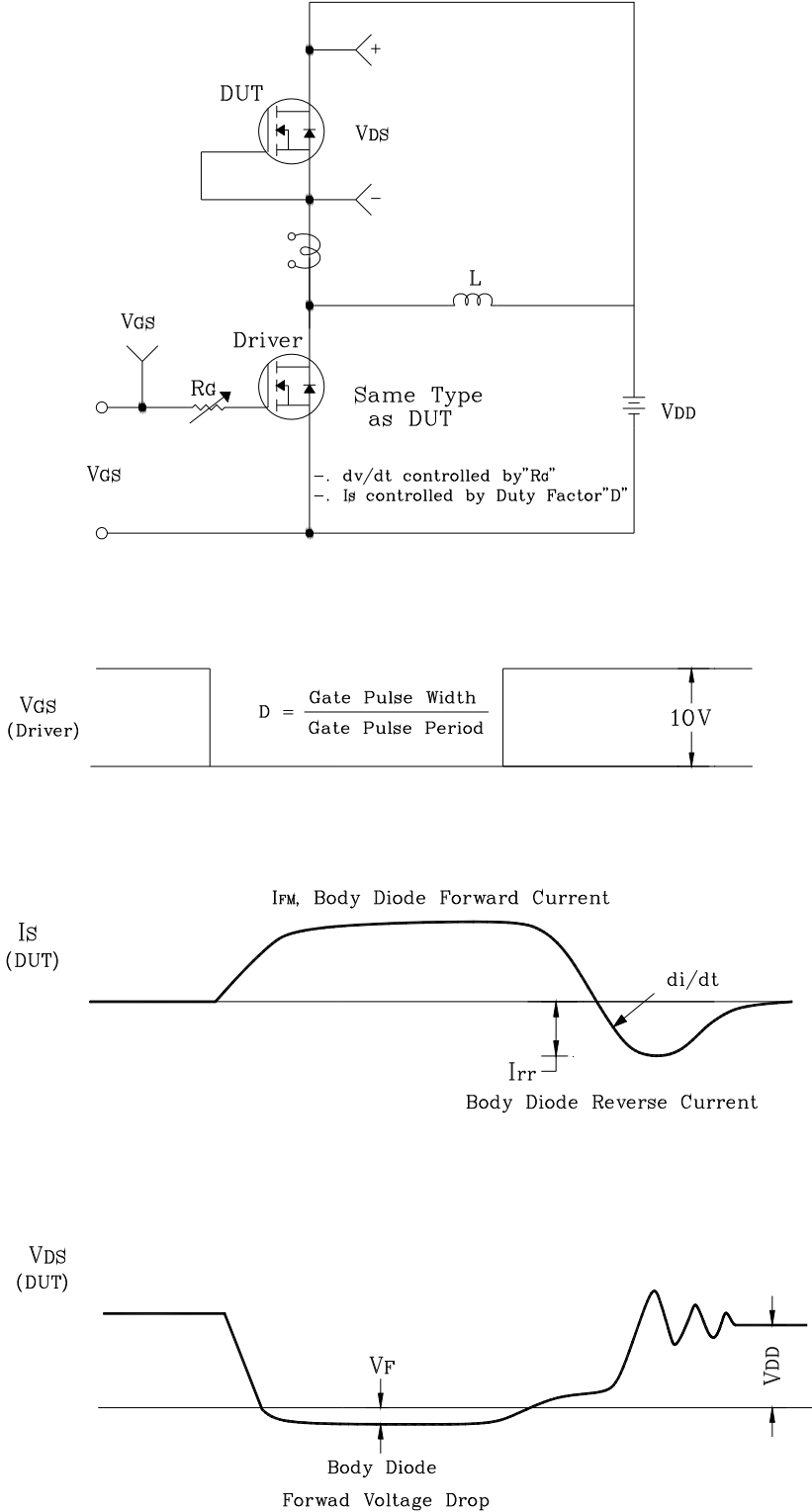
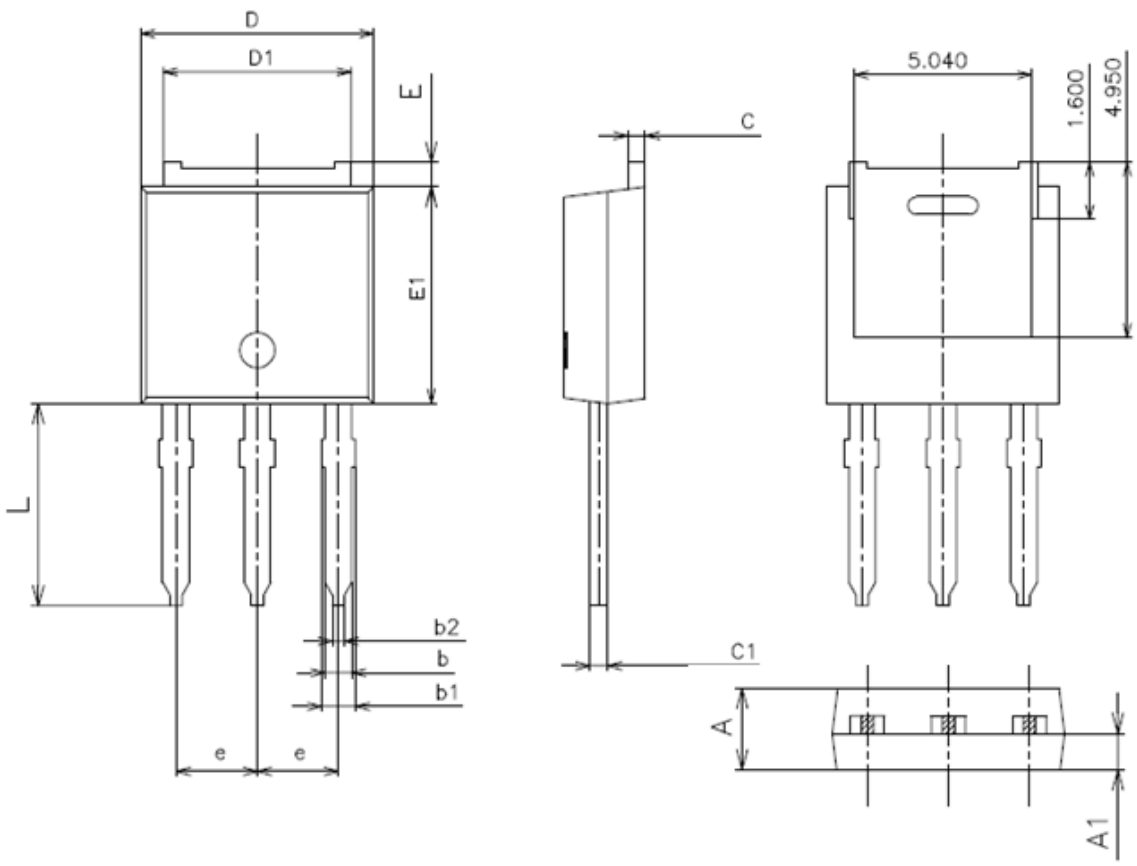


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
D	6.40	6.60	6.80	
D1	5.14	5.34	5.54	
E	0.50	0.70	0.90	
E1	5.90	6.10	6.30	
A	2.20	2.30	2.40	
A1	0.87	1.07	1.27	
C	0.40	0.50	0.60	
C1	0.40	0.50	0.60	
L	5.50	5.70	5.90	
b	0.66	0.76	0.86	
b1	0.82	1.02	1.22	
b2	0.25	0.35	0.45	
e	2.10	2.30	2.50	

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