DATA SHEET

SMP1331-085LF: 50 W Surface Mount Shunt Connected PIN Diode

Applications

- Low-loss, high-power switches
- Low distortion attenuators

Features

- Low-thermal resistance: 28 °C/W
- Suitable for 50 W Continuous Wave T/R switches
- Low capacitance: 0.35 pF
- Low distortion performance
- QFN (3-pin, 2 × 2 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

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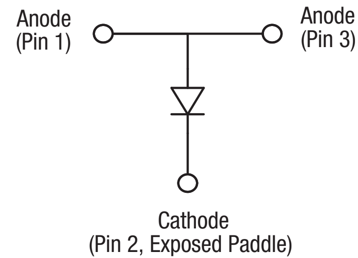

Figure 1. SMP1331-085LF Block Diagram

Description

The SMP1331-085LF is a surface mountable, low capacitance silicon PIN diode designed as a shunt connected PIN diode for high power, high volume switch and attenuator applications from 10 MHz to beyond 6 GHz.

Maximum resistance at 100 mA is 0.5 Ω and typical capacitance at 30 V is 0.35 pF. The combination of low junction capacitance, low parasitic inductance, low thermal resistance, and nominal 30 μm I-region width, makes the SMP1331-085LF useful in large signal switches and attenuator applications.

The device has a 2.5 W dissipation power rating, making it capable of handling more than 50 W @ 85 °C Continuous Wave (CW) in a shunt-connected transmit/receive (T/R) switch.

Design information for high power switches may be found in the Skyworks Application Note, *Design With PIN Diodes* (document number 200312).

A block diagram of the SMP1331-085LF is shown in Figure 1.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SMP1331-085LF are provided in Table 1. Electrical specifications are provided in Table 2.

Typical DC performance characteristics of the SMP1331-085LF are illustrated in Figures 2 and 3.

Table 1. SMP1331-085LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Reverse voltage	V_R		200	V
Forward current @ 25 °C	I_F		200	mA
CW power dissipation @ 85 °C	P_D		2.5	W
Peak pulse power dissipation @ 85 °C (10% duty cycle)			25	W
Storage temperature	T_{STG}	–65	+200	°C
Operating temperature	T_A	–40	+150	°C
Electrostatic discharge:	ESD			
Charged Device Model (CDM), Class 4			1100	V
Human Body Model (HBM), Class 1C			1000	V
Machine Model (MM), Class C			400	V

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION*: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 2. SMP1331-085LF Electrical Specifications (Note 1)
(T_A = +25 °C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Reverse current	I_R	V_R = 200 V			10	µA
Capacitance	C_T	f = 1 MHz, V_R = –30 V			0.35	pF
Resistance	R_S	f = 100 MHz:				
		I_F = 1.0 mA			14.5	Ω
		I_F = 10.0 mA		1.7		Ω
		I_F = 100 mA		0.5		Ω
Forward voltage	V_F	I_F = 10 mA		0.8		V
Carrier lifetime	T_L	I_F = 10 mA		600		ns
I region width	W			30		µm
CW thermal resistance	θ_{JC}	Junction-to-case		28		°C/W
Peak thermal resistance	θ_P	Single 1 µs pulse width, junction-to-case (10% duty cycle)		2.8		°C/W

Note 1: Performance is guaranteed only under the conditions listed in this table.

Typical DC Performance Characteristics
(T_A = 25 °C, Unless Otherwise Noted)

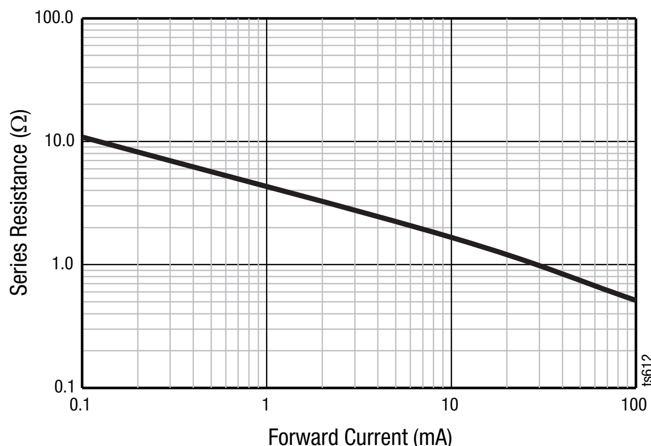

Figure 2. Series Resistance vs Current @ 100 MHz

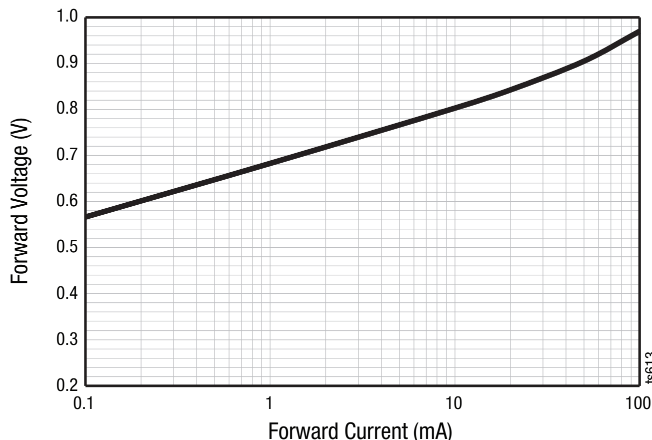

Figure 3. Forward Voltage vs Forward Current

High-Power Switch Design Application

The SMP1331-085LF PIN diode is designed for shunt applications such as reflective switches or shunt-diode attenuator circuits. Compared to other surface mount packages, the design of the QFN package produces lower thermal resistance and also reduces the effects of the parasitic inductance of the anode bond wires.

A cross-sectional view of the SMP1331-085LF PIN diode is shown in Figure 4. The cathode of the die is soldered directly to the top of the exposed paddle. This paddle is composed of copper, so its thermal resistance is very low.

The copper ground paddle minimizes the total thermal resistance between the I layer, which is the location where most heat is generated under normal operation, and the surface to which the package is mounted. Minimal thermal resistance between the I layer and the external environment minimizes junction temperature.

The electrically equivalent circuit of the SMP1331-085LF PIN diode is shown in Figure 5. The inductances of pins 1 and 2, as well as the inductances of the bond wires are in series with the input and output transmission lines of the external circuit rather than the portion of the circuit that contains the shunt PIN diode.

The effects of these parasitic series inductances are negligible, since they add a very small insertion loss to the shunt PIN but have no effect on the isolation that the diode produces when it is forward biased.

A cross section of the suggested printed circuit board design is shown in Figure 6. The via shown in this view is critical, both for electrical performance and for thermal performance. It is recommended that several vias should be placed under the entire footprint of the exposed paddle (pin 2) to minimize both electrical inductance to the system ground and thermal resistance to the system heat sink.

A high-power switch has been designed and tested. This circuit is shown in Figure 7, and Table 3 lists the Evaluation Board Bill of Materials for the circuit.

Typical RF performance of the SMP1331-087LF using the circuit shown in Figure 7 is summarized in Table 3 and illustrated in Figures 8 through 10.

An assembly drawing for the Evaluation Board is shown in Figure 11. The layer detail physical characteristics are provided in Figure 12.

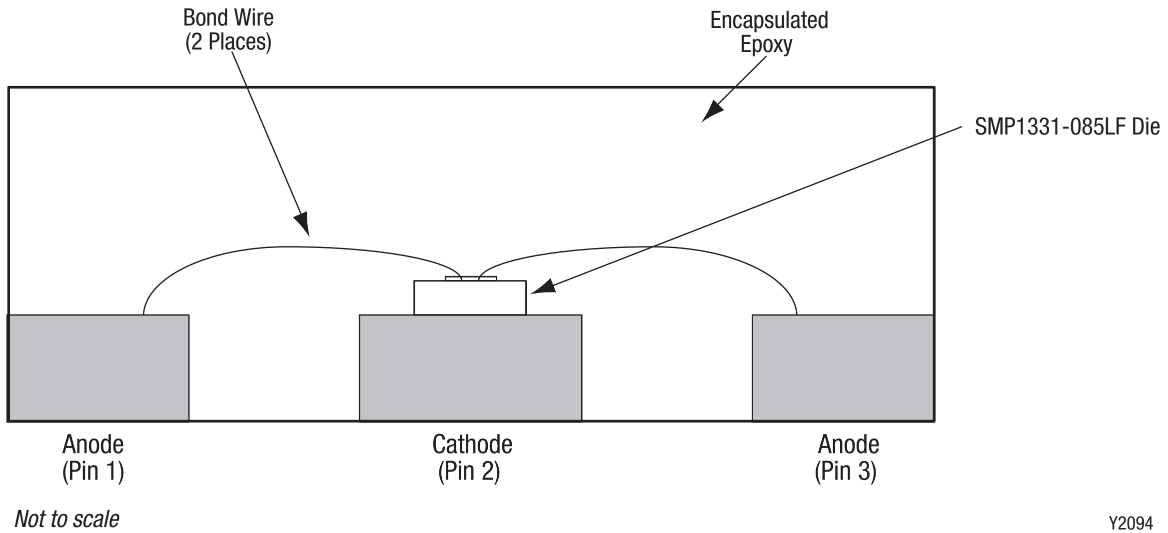

Figure 4. Cross-Sectional View of the SMP1331-085LF

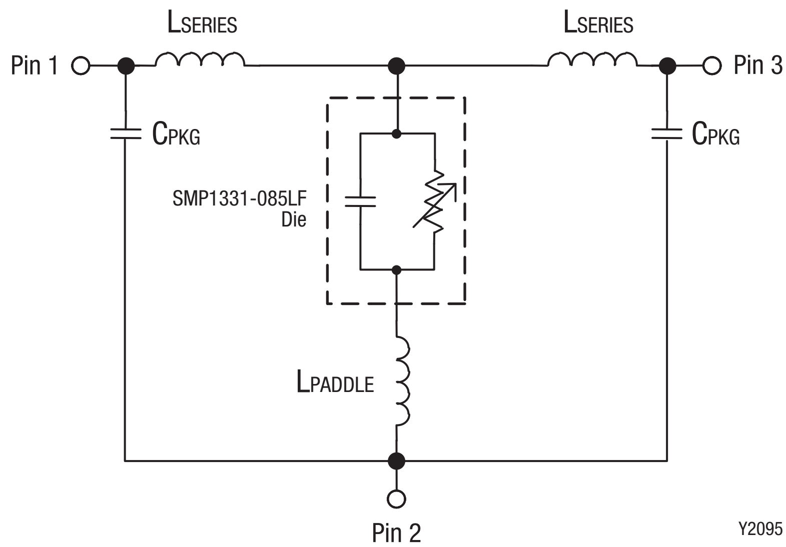

Figure 5. SMP1331-085LF Electrically Equivalent Circuit

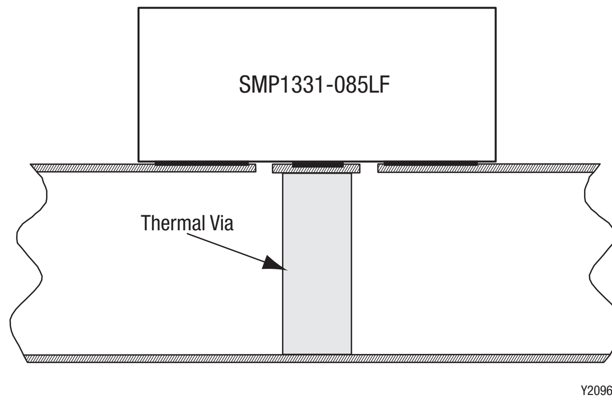

Figure 6. Cross-Sectional View of Suggested Printed Circuit Board

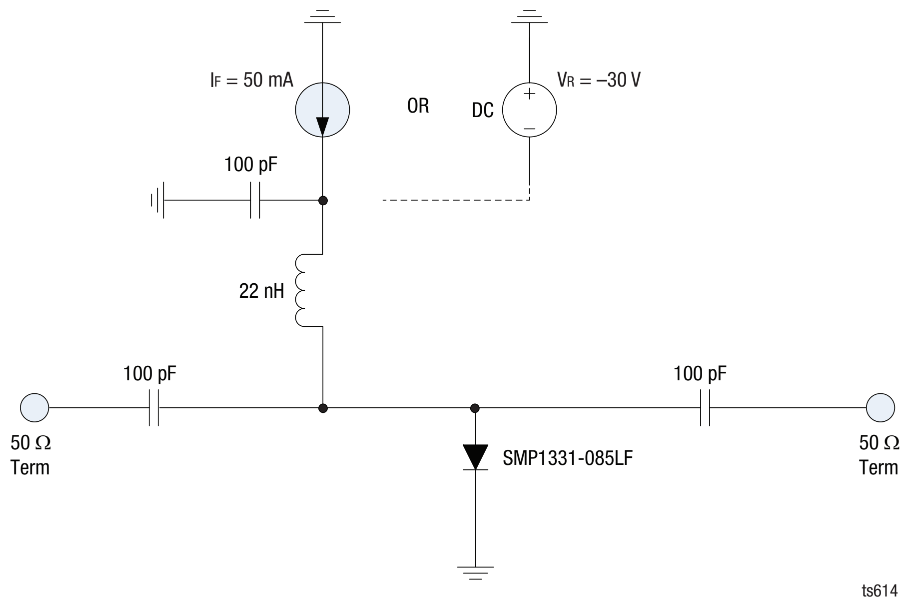

Figure 7. High-Power Switch Design

Table 3. Evaluation Board Bill of Materials for EN33-D515-001_V4

Component	Value	Size	QTY	Manufacturer	Mfg. Part Number	Characteristics
C	100 pF	0402	3	Murata	GRM1555C1H101JZ01	5% C0G 50 V
L	22 nH	0402	1	Taiyo Yuden	HK100522NJ-T	5% 300 mA SRF 1.9 GHz

Table 4. Typical RF Performance Characteristics @ 25 °C, f = 2.6 GHz
(T_A = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, EVB Optimized with Bias Circuit, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typical	Units
Insertion loss	IL	V_R = –30 V	–0.18	dB
Return loss	RL	V_R = –30 V	–18.7	dB
Isolation	ISO	I_F = 50 mA	29.8	dB
Max power	P_{MAX}	V_R = –30 V	47	dBm

Typical RF Performance Characteristics
(T_{OP} = +25 °C, Characteristic Impedance [Z0] = 50 Ω, EVB Optimized with Bias Circuit, Unless Otherwise Noted)

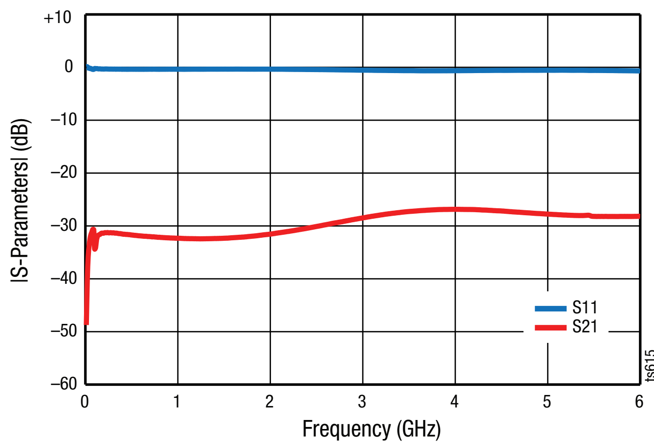

Figure 8. S-Parameter Magnitude vs Frequency, I_F = 50 mA

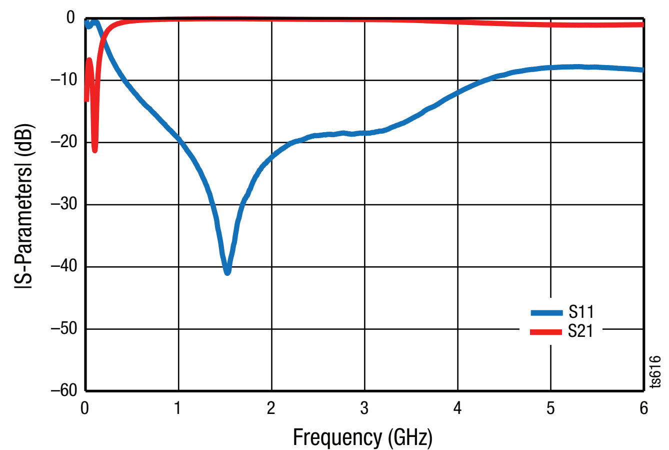

Figure 9. S-Parameter Magnitude vs Frequency, V_R = –30 V

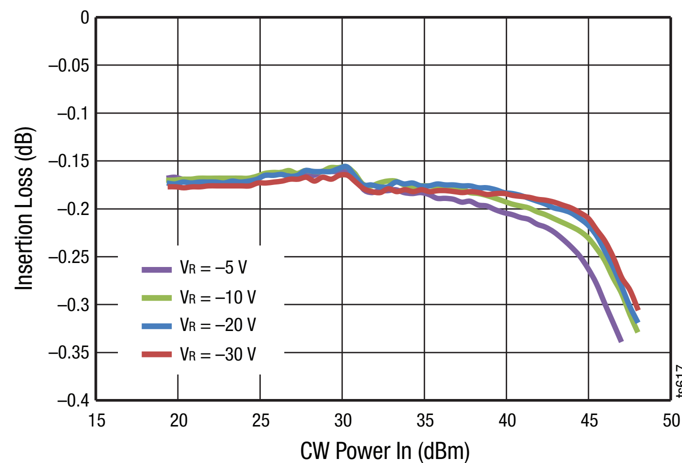

Figure 10. Insertion Loss vs CW Power In at Different V_R, f = 2.6 GHz

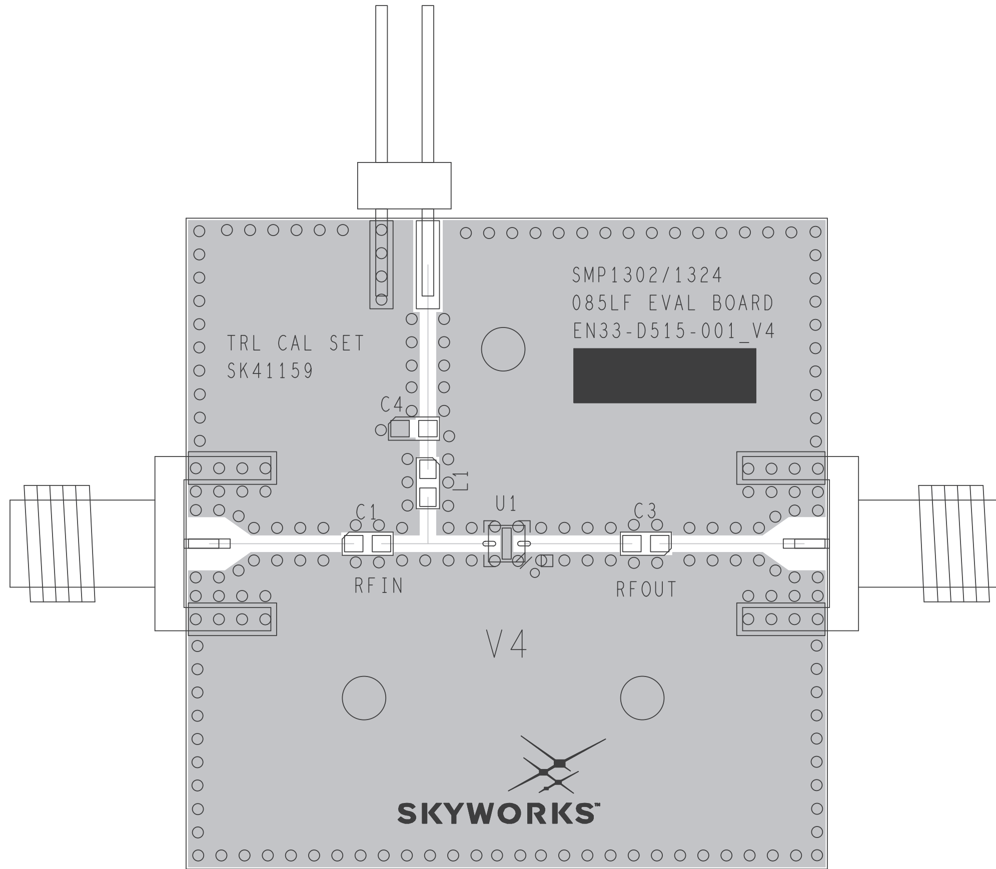

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Figure 11. Evaluation Board Assembly Diagram

Cross Section

Name	Thickness (in)	Material
Top Soldermask		
L1	(0.0028)	Cu foil
Laminate	0.012 ± 0.0006	Rogers RO4003C Core
L2	(0.0014)	Cu foil
Laminate	(Note 1)	FR4 Prepreg
L3	(0.0014)	Cu foil
Laminate	0.010 ± 0.0006	FR4 Core
L4	(0.0028)	Cu foil
Bottom Soldermask		

Note 1: Adjust this thickness to meet total thickness goal of 0.062 ± 0.005 inches.

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Figure 12. Evaluation Board Layer Detail Physical Characteristics

Package Dimensions

The PCB layout footprint for the SMP1331-085LF is shown in Figure 13. Typical part markings are shown in Figure 14. Package dimensions for the 3-pin QFN are provided in Figure 15, and Figure 16 provides the tape and reel dimensions.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SMP1331-085LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

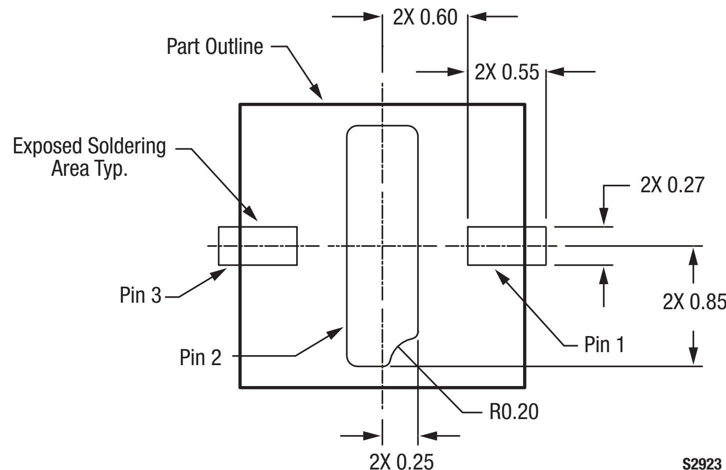

Figure 13. SMP1331-085LF PCB Layout Footprint

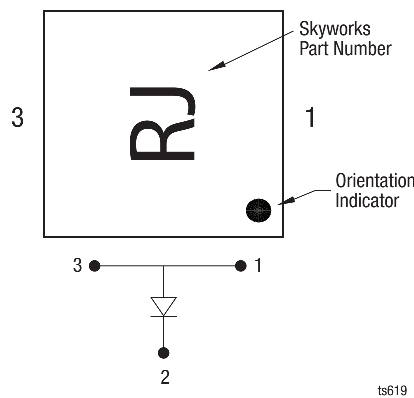

Figure 14. Typical Part Markings (Top View)

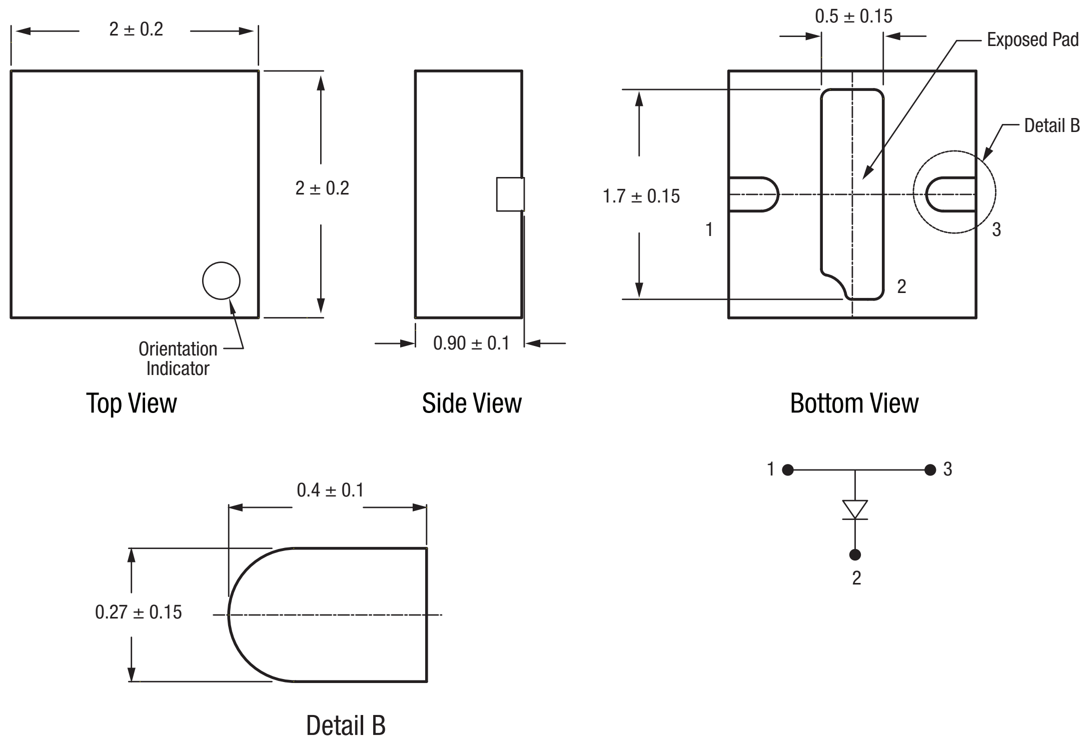

Figure 15. SMP1331-085LF QFN Package Dimension Drawing

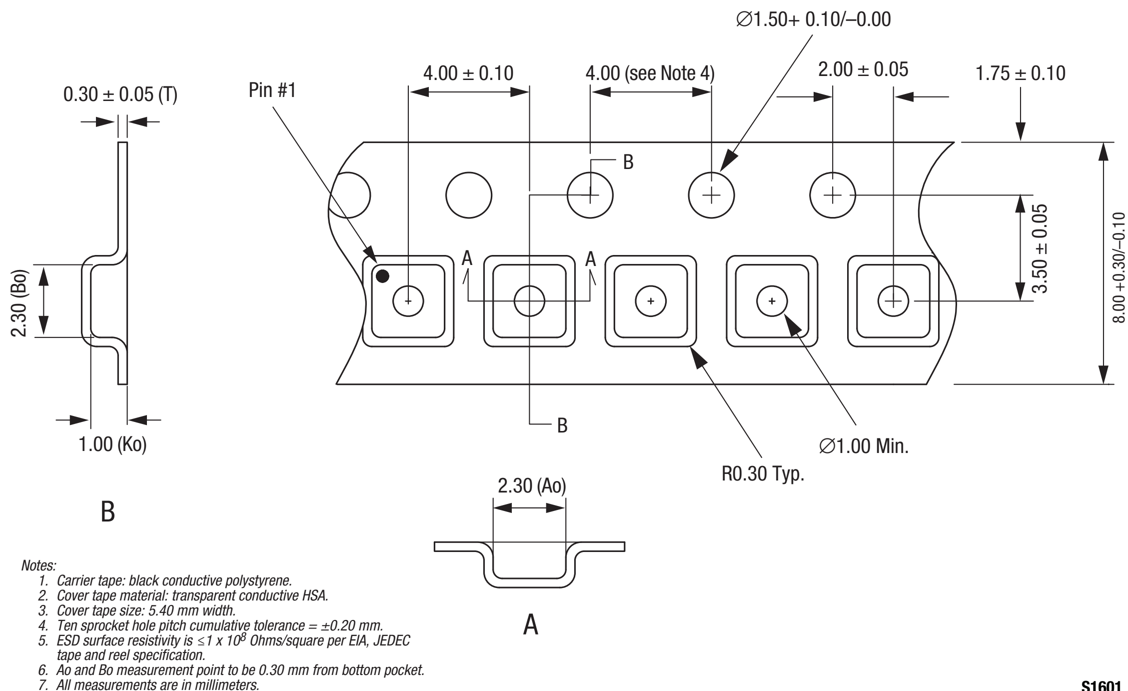

Figure 16. SMP1331-085LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number
SMP1331-085LF: Surface Mount PIN Diode	SMP1331-085LF

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