SIEMENS

Technical Description
Order No: 6AR1930-4AA05-2CA0 **June 1999**

# SMP16-SFT260

Order Number: 6AR1304-0AA01-0AA0

**4-Channel Positioning Board for SMP16 Systems**

## SICOMP Industrial Microcomputer

(4)J31069-D2078-U001-A0-7618

## Product History of the Technical Description

| Revision [1)] | Record of Changes | Date |
|---|---|---|
| A0 | First edition | 06/99 |

*1) Corresponds to the 4th block of digits of the drawing number in the footer*

## Explanation of Notation

* An asterisk behind the signal name indicates a low-active signal (e.g., IOR*).

/ A slash between two signal names separates two level-dependent functions of one signal. Example: C/D* means Command for high level and Data for low level.

– Connections indicated with a dash in a connector assignment table are reserved (i.e., bus or I/O interface).

**Signal** Special signals not included in these specifications are indicated in bold print in the signal assignment tables and then explained (e.g., **AMSEOP**).

 TD1/Ka/WW8.0/VS5.0/A4

# Safety Notes for SICOMP Boards

## ESD protection measures

### Caution

When handling boards and other components carrying this symbol, always adhere to ESD protection guidelines (**E**lectrostatic **S**ensitive **D**evices).

- Never touch the boards unless required work makes this absolutely necessary.
- When working with the boards, use a conductive and grounded work surface.
- Wear a grounding bracelet.
- Never touch the pins, connections or printed circuits of the boards.
- Never permit the boards or components to be touched by chargeable objects (e.g., synthetic materials).
- Keep the boards or components at least 10 cm away from CRT units and television sets.
- Leave the boards in their special packaging until they are needed. When registering boards, etc. do not remove the boards from their packaging or touch them.
- Boards may only be installed or removed when the voltage is off.

## Wiring of Bus Backplanes

System-related signal wiring on SICOMP board systems is performed with wrap connections. The power supply cables are bundled together with cable binders. These cables are equipped with plug-in or screw connections.

**Caution:**
All signal wiring (the interrupt signal lines in particular) must be of the appropriate design and kept as short as possible. When longer interrupt signal lines cannot be avoided, twisted pair wiring must be used.

## Related SICOMP SMP16 Literature

For more information on installing and handling SICOMP boards, see "SICOMP IMC system manual".

# Table of Contents

# 1 Initial Startup

The primary steps involved in the initial startup of the board are listed below.

1. Software configuration. See chapters 1.1 and 4 for more information.

   **Attention:**
   Only chip select channel 0 may be **enabled** for the board. The other chip select channels and the ASBIC channel must be **disabled**.

2. Wiring the interrupts on the bus backplane. See chapter 1.2 for more information.
3. Connecting accessory modules for additional interfaces. See chapter 1.3 for more information.
4. Wiring the I/O devices. See chapter 1.4 for more information.

**Caution**

Do not plug or unplug the board or the encoder connections while the power is on. To do so may damage the board permanently.

## 1.1 Preparing for Software Configuration

The configuration of the board with the SMP16-AKO auto configuration software (see chapter 2.12) can be performed directly in the target system or in a separate generation system. In addition, the configuration can be performed in a separate system, but the board can still be configured in the target system. In all cases, the board must be installed in an SMP16 bus system with daisy chain connection at the time of programming.

### Configuration in the target system

| | **Requirements on the Target System** |
|---|---|
| Required hardware | • SICOMP IMC AT CPU<br>• SMP16 bus backplane with daisy chain |
| Required software | • Windows 95<br>• SMP16-AKO V2.0 |

### Configuration in the target system, generation of the configuration in separate system

| | **Requirements on the Target System** | **Requirements on the Generation System** |
|---|---|---|
| Required hardware [1)] | • SICOMP IMC AT CPU<br>• SMP16 bus backplane with daisy chain | • PC-AT (e.g., workplace computer or laptop) |
| Required software | • RMOS or MS-DOS<br>• AKO start program | • Windows 95 or Windows NT<br>• SMP16-AKO V2.0 |

*1) In addition, there must be a way to transfer the generated configuration file (i.e., STARTUP.SKD) to the target system. Some examples are listed below.*
*- Serial connection via zero modem cable (is supported by AKO start program)*
*- Floppy disk drives on both systems*
*- LAN connection*

## Configuration in a separate generation system

The board is installed in the generation system for configuration and then returned to the target system afterwards.

| | **Requirements on the Generation System** |
|---|---|
| Required hardware | • SICOMP IMC AT CPU<br>• SMP16 bus backplane with daisy chain |
| Required software | • Windows 95<br>• SMP16-AKO V2.0 |

## Daisy chaining for configuration via software

With SMP16-SYS403 bus backplanes with 5 or more slots, the daisy change connection is already implemented electronically.

With the other bus backplanes, the slots of the software-configurable boards must be wired as shown below.

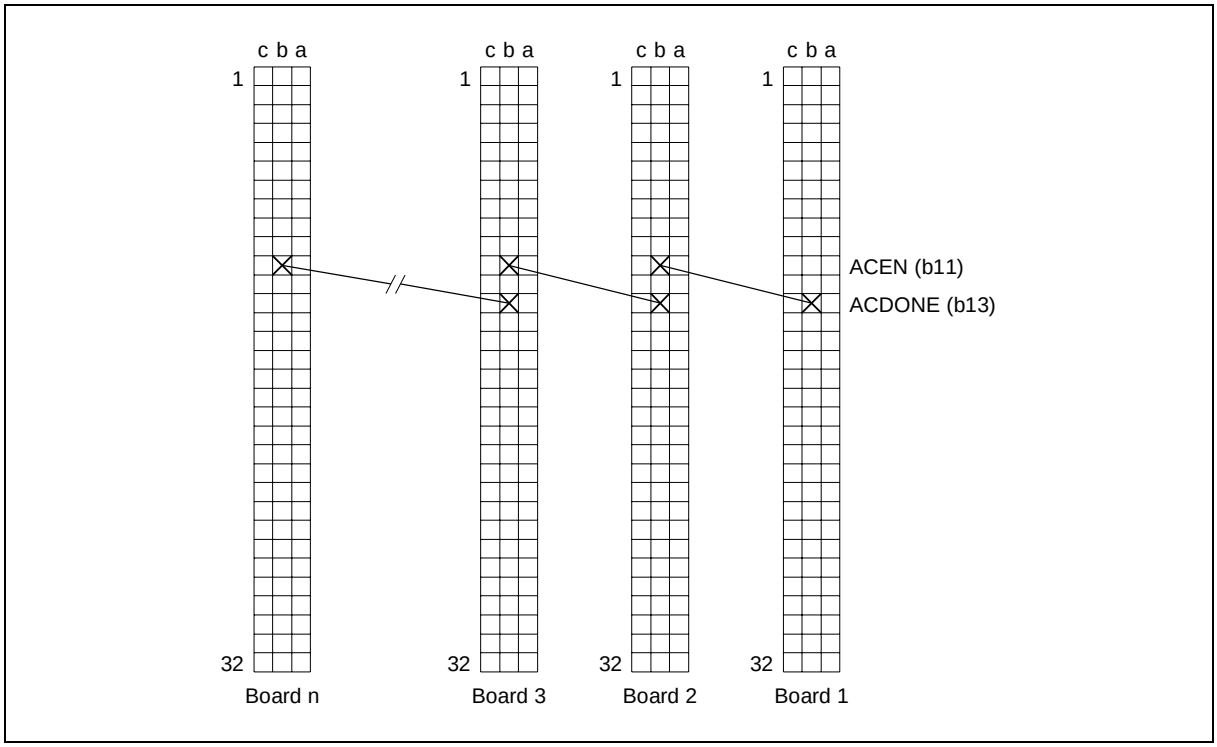



Figure 1.1 Daisy chaining on the SMP16 bus backplane for configuration via software

The ACEN input of the first software configurable board in the chain of configuration remains open as does the ACDONE output of the last board. All other ACDONE outputs must be connected with the ACEN input of the next board. See chapter 3.1.2.

## 1.2 Interrupt Wiring

The outputs of the interrupts used must be wired on the bus backplane from the slot of the board to free interrupt inputs on the CPU or other interrupt-processing boards.

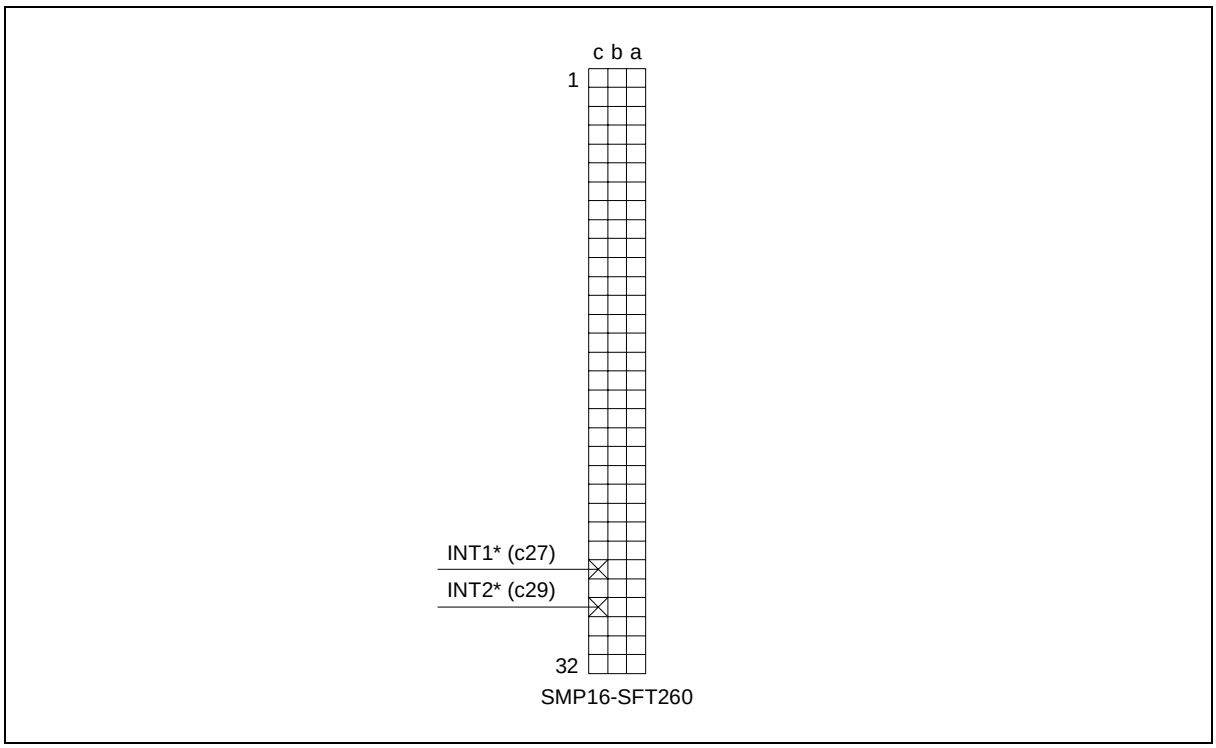



Figure 1.2 Interrupt sources of the SMP16-SFT260

## 1.3 Connection of Accessory Modules

If necessary, accessory modules must be connected to the SMP16-SFT260 to provide additional interfaces. See chapter 2.12.

- SMP16-ZUB260: Two ribbon cables on X3 and X4 of the board
- SMP16-ZUB261: One ribbon cable on X5 of the board

# 1.4 Wiring the I/O

## 1.4.1 Connecting Incremental Encoders

### 5 V incremental encoders

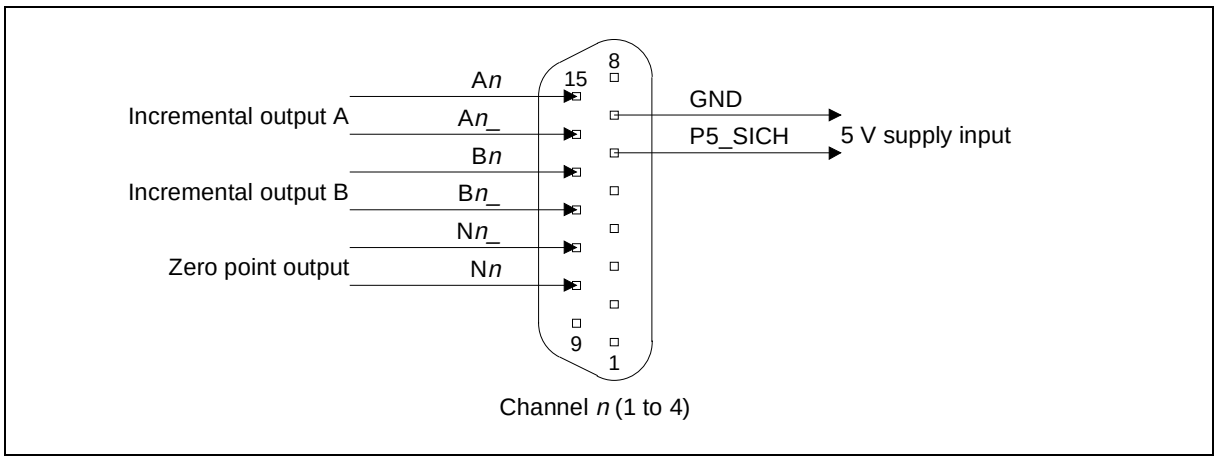



Figure 1.3 Connection of a 5 V incremental encoder on X6 or X7 of the board SMP16-SFT260, or X1 or X2 of the SMP16-ZUB260 accessory module

### 24 V incremental encoders

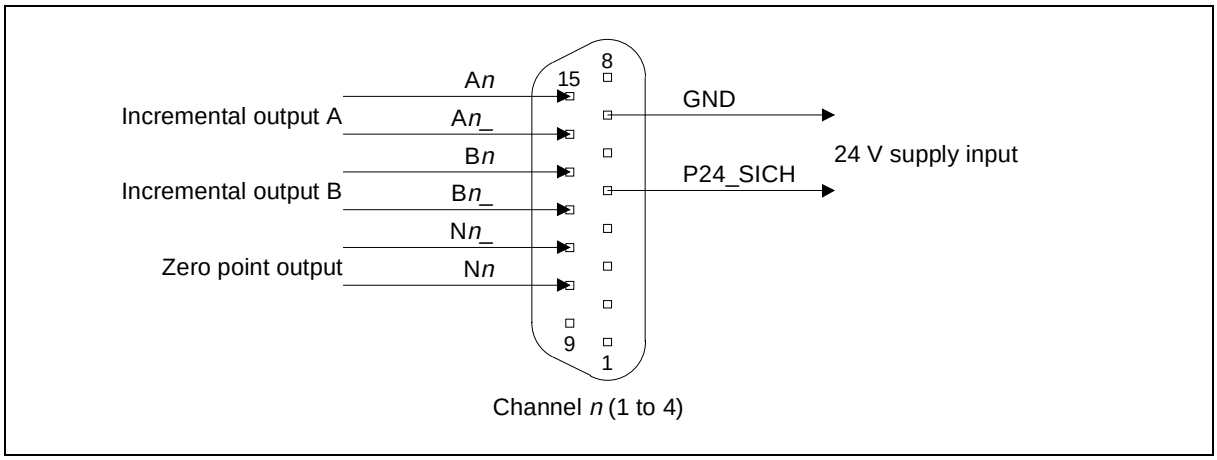



Figure 1.4 Connection of a 24 V incremental encoder on X6 or X7 of the board SMP16-SFT260, or X1 or X2 of the SMP16-ZUB260 accessory module

**Note:**
With one-track encoders or encoders without a zero mark, the open inputs must be terminated (i.e., B*n*, N*n* against GND, B*n*_, N*n*_ against P5_SICH) since otherwise a permanent wire break message would be generated.

### 1.4.2 Connecting SSI Encoders

## 5 V SSI encoders

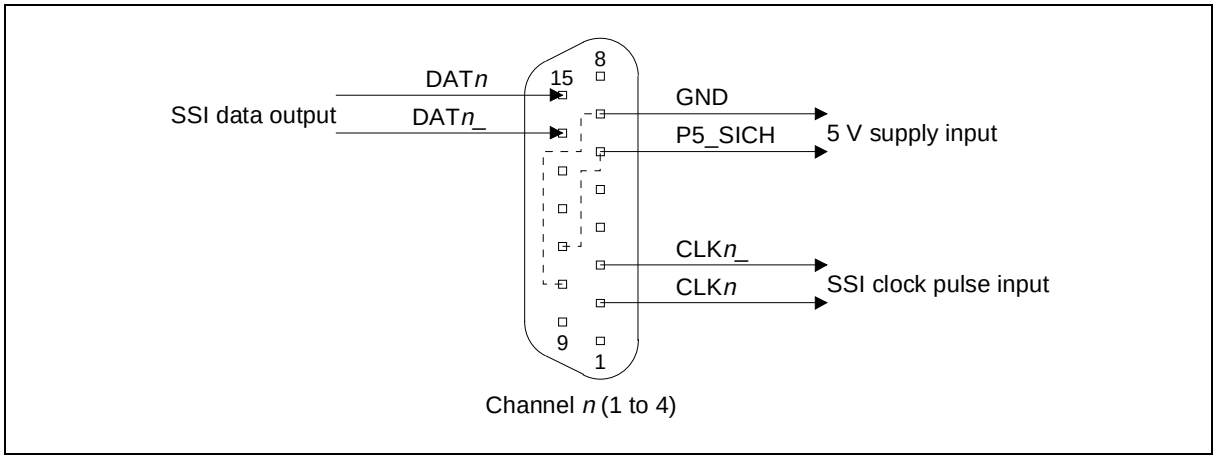



Figure 1.5 Connection of a 5 V SSI encoder on X6 or X7 of the board SMP16-SFT260, or X1 or X2 of the SMP16-ZUB260 accessory module

## 24 V SSI encoders

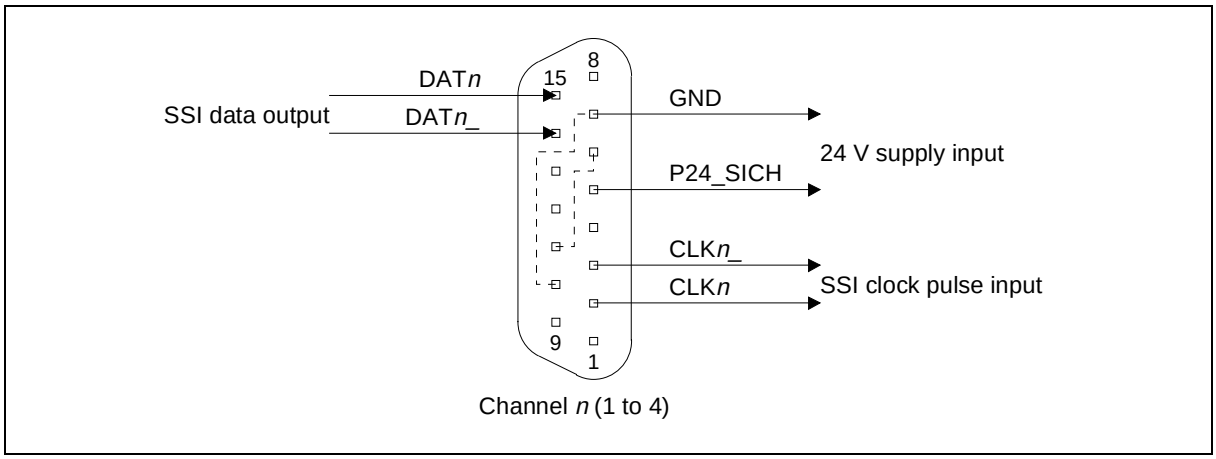



Figure 1.6 Connection of a 24 V SSI encoder on X6 or X7 of the board SMP16-SFT260, or X1 or X2 of the SMP16-ZUB260 accessory module

**Note:**
In observer mode, the zero marking signals must be terminated (i.e., pin 10 against GND and pin 11 against P5_SICH) since otherwise a permanent wire break message would be generated. These connections are shown above with broken lines.

## 1.4.3 Connection of the Gate Signals and the 24 V Power

**Notes:**
When a 24 V voltage is fed in, this is available on all plug connectors of the board and the accessory modules.

Do not install the cables for the 24 V power and the signals of the gate inputs in the encoder cable.

### On the plug connectors of the encoder channels

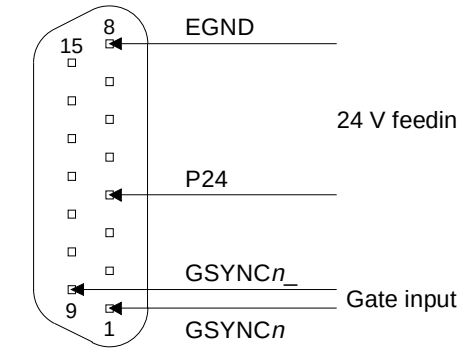



Figure 1.7 Connection to X6 or X7 of the SMP16-SFT260 board, or X1 or X2 of the SMP16-ZUB260 accessory module

### Via accessory module SMP16-ZUB261

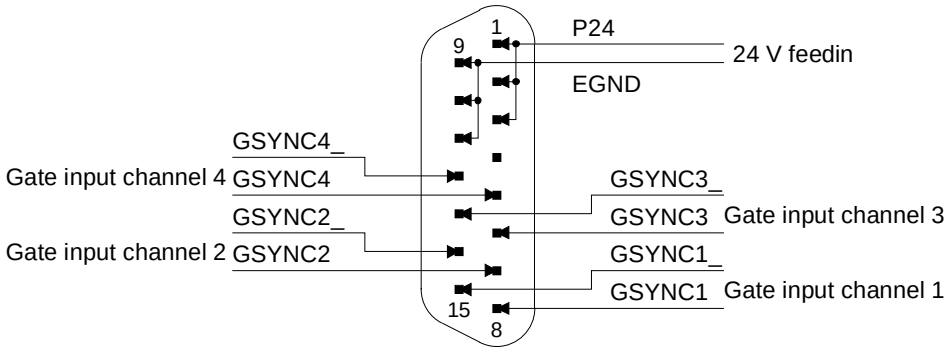



Figure 1.8 Connection to X1 of the SMP16-ZUB261 accessory module

**Note:**
The signals of the gate inputs are available in parallel on the plug connectors of the respective encoder channels.

# 2 Features

## 2.1 Overview of the Functions

### General

- 1-slot-wide positioning board for SMP16 systems
- Four channels for connection of SSI or incremental encoders
- Connections for channels 1 and 2 via sub D sockets directly on the front plate of the board
- Connections for channels 3 and 4 via sub D sockets on the accessory module SMP16-ZUB260
- 5 V encoder power supply directly on the SMP16 bus
- External feedin for 24 V encoder power supply
- Two time measuring channels
- Gate functions for track signals and zero marking signal
- SMP16 bus interface via ASBIC block
- Auto configuration with data storage in EEPROM
- Individual labeling of the front plate via included adhesive labels

### Encoder inputs

- SSI encoder with 13, 21 or 25 bits. Clock pulse adjustable from 78 kHz to 1.25 MHz.
- One or two-track incremental encoder, maximum of 1.25 MHz
- Wire break monitoring
- 5 V and 24 V encoder power supply
- Two encoder ASICs (type GE2003N)
- EPLDs for gate functions and wire break monitoring

For a detailed description of the encoder ASICs, see chapter 6.

### Interrupts

The board can generate two interrupts on the SMP16 bus which come directly from the encoder ASICs. See chapter 6.2.

## 2.2 Block Circuit Diagram

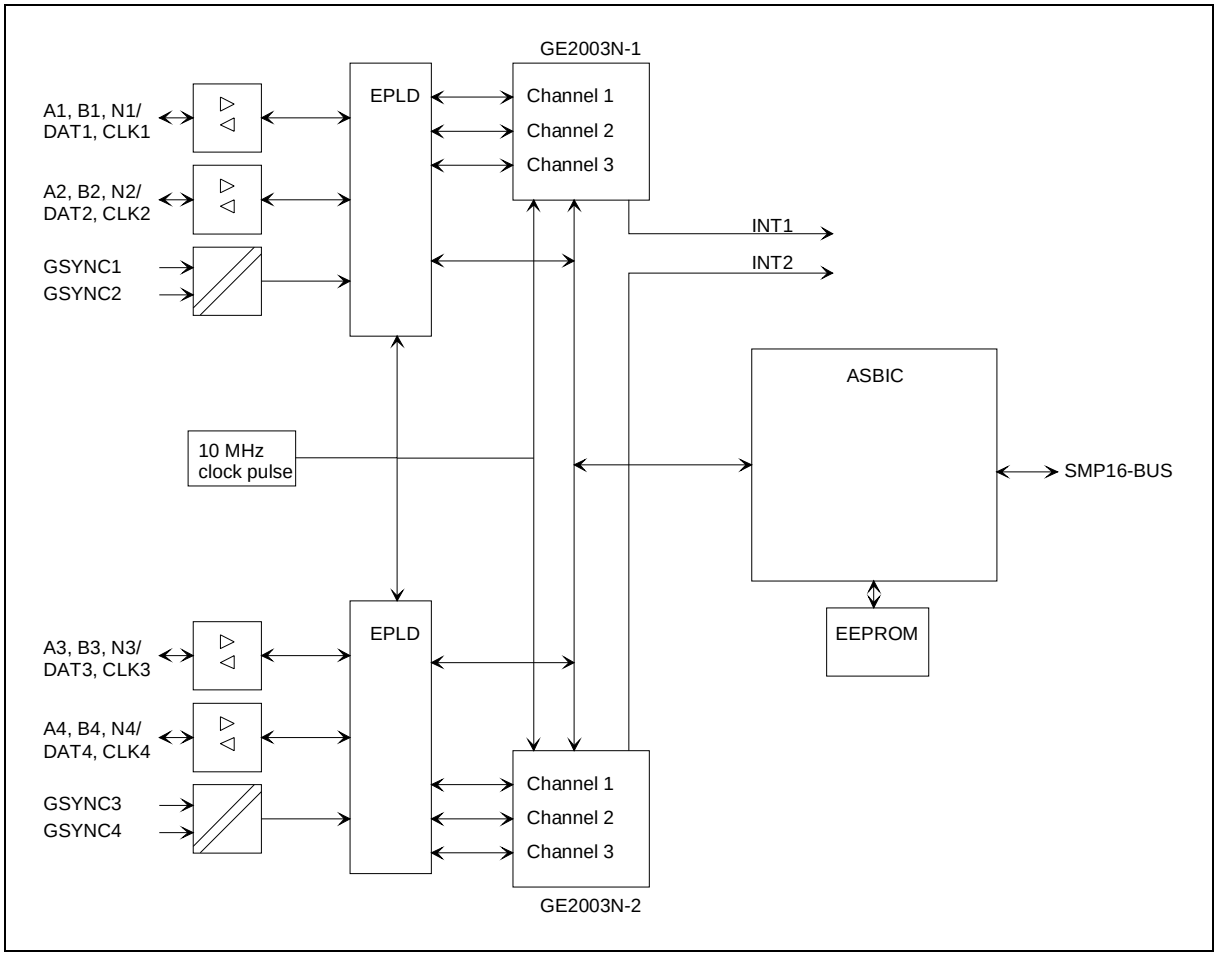



Figure 2.1 Block circuit diagram of the SMP16-SFT260

## 2.3 Encoder Inputs

Each of the encoder ASICs contains three identical position acquisition channels, two of which are used for encoders. The third channel of each ASIC can be used as a time-measuring channel. See chapter 2.5.

- Encoder channels 1 and 2 of the board are acquired by the first ASIC (GE2003N-1).
- Encoder channels 3 and 4 of the board are acquired by the second ASIC (GE2003N-2).

Each encoder channel can be operated with an absolute value encoder (SSI) or an incremental encoder. All encoder signals are designed as differential signals in accordance with RS 485/RS 422.

### Wire break monitoring

The input signals of the encoder connections are monitored for the following errors.

- Wire break of one or both cables of one track
- Short circuiting of the cables of one track
- Short circuit against GND
- Short circuit against +5 V

All error messages of one encoder channel are combined in a group message. See chapter 5.1.

Reliable wire break monitoring is only ensured for input frequencies up to a maximum of 200 kHz. The counting signals can always be acquired up to the maximum counting frequency.

In contrast to incremental encoders where all encoders signals are monitored, only the DAT data input is monitored with SSI encoders. The CLK clock pulse signal and the unused zero marking signal are circuited as outputs.

In observer mode, all signals are inputs and are monitored. The zero marking signal must be terminated to prevent a permanent wire break message for this signal. See chapter 1.4.2.

## 2.4 Gate Function and Gate Inputs

The board has three gate functions.

- Gate function for track signals A and B
- Gate function for the zero marking signal
- Gate function for the time-measuring function. See chapter 2.5.

**Caution**

The gate functions may only be activated with incremental encoders.

### 2.4.1 Gate Function for Track Signals A and B

When the gate function is activated, the track signals are not forwarded to the encoder ASIC unless the related gate input is also active. The enable for the gate function for the track signals and the active level of the gate input can be specified separately for each encoder channel. See chapter 5.2.

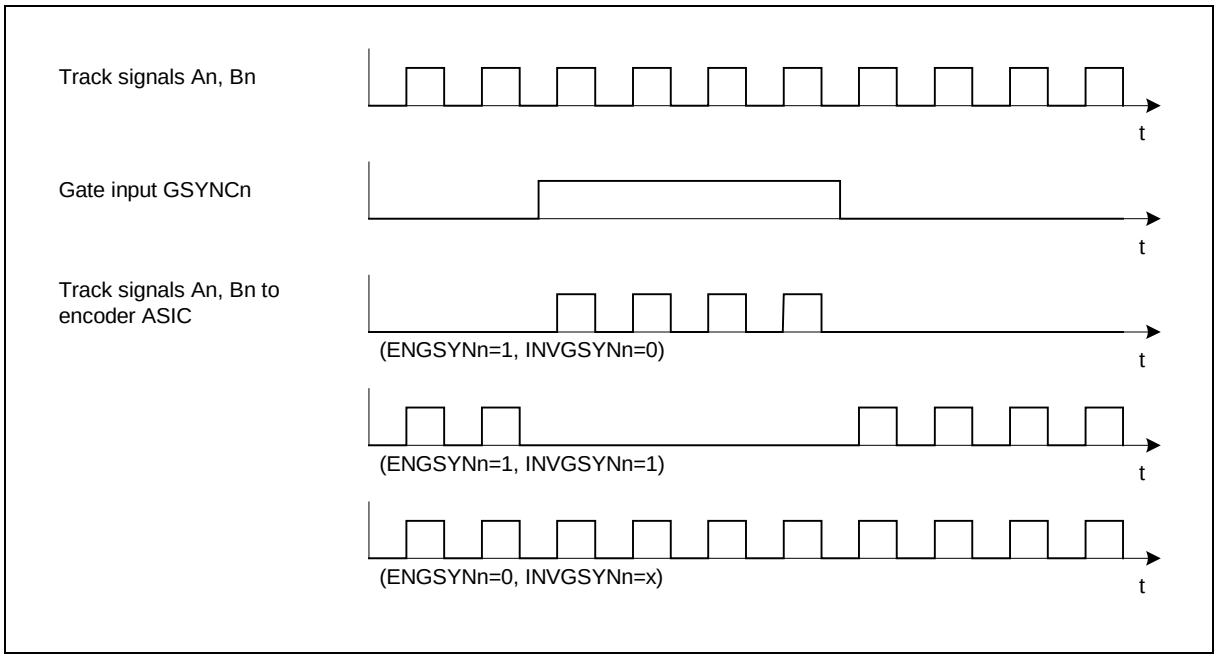



Figure 2.2 Signal form for the gate function for track signals A and B

## 2.4.2 Gate Function for the Zero Marking Signa

The zero marking signal is **always** dependent on the gate input. There are two types of operating modes.

- All zero marking pulses are evaluated when the gate input is high.
- After a falling edge on the gate input, only the next zero marking pulse is forwarded. All other impulses are suppressed until the next falling edge occurs on the gate input.

The gate function for the zero marking signal can be specified separately for each encoder channel. See chapter 5.3. The settings of the gate enable and the active level for the gate input are irrelevant.

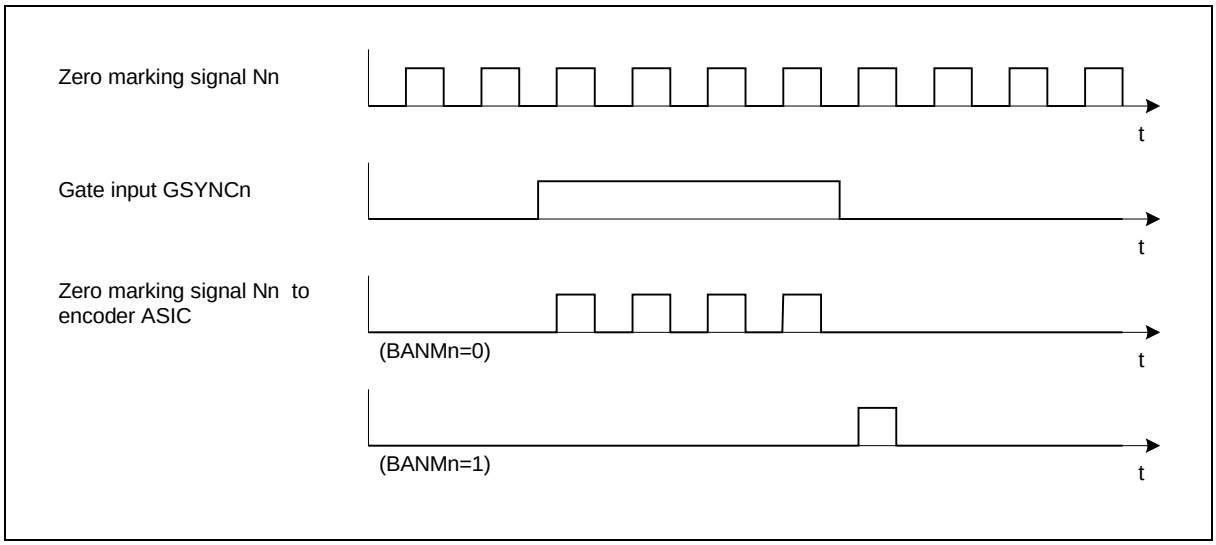



Figure 2.3 Signal form for the gate function for the zero marking signal

**Note:**
When an encoder with zero mark is used, the gate input of the appropriate channel must always be circuited. The enable of the gate function and the selection of the active level of the gate input do not affect the gate function for the zero mark.

## 2.5 Time-Measuring Function

The third channel of each ASIC is used for the time-measuring function. The counter of the time-measuring channel is clocked with a fixed frequency of 1.25 MHz. Evaluation of the counting pulses depends on the gate input of encoder channel 2 (for time-measuring channel 1) or encoder channel 4 (for time-measuring channel 2). This can be used to specify the duration of the signals on the gate input, for example.

The gate function and the active level of the gate input can be specified separately for each channel. See chapter 5.2.

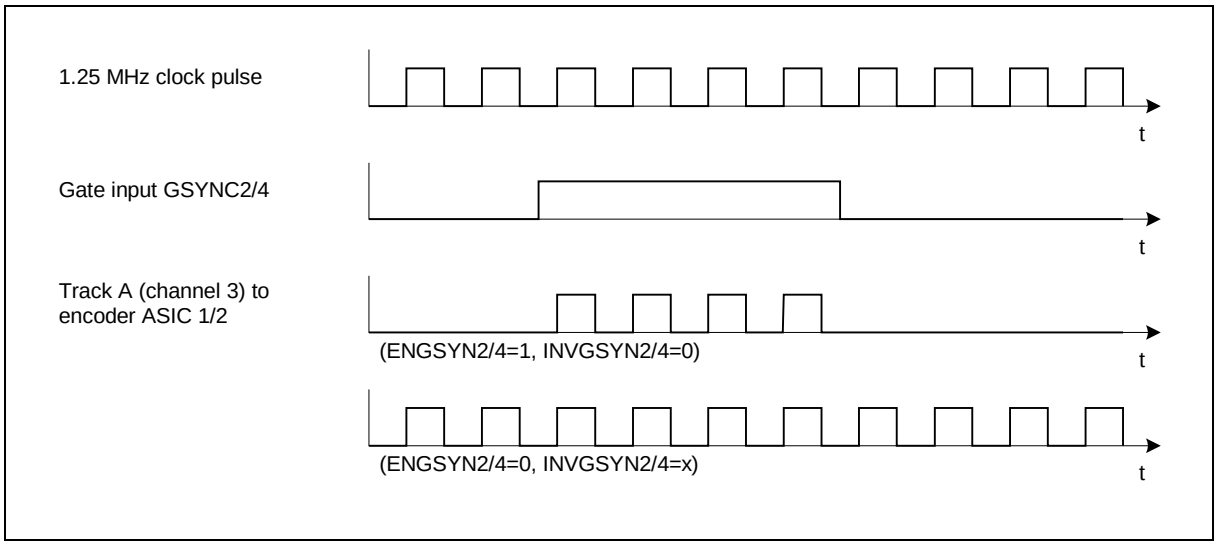



Figure 2.4 Signal form for the time-measuring function

**Note:**
Operating mode "counting without RDC" must be set in the command register of the time-measuring channel. If not, the counter only hovers around ±1.

## 2.6 Power Supply for Encoder

The 5 V encoder power supply is taken directly from the SMP16 bus and fed to the encoder connections via a safety fuse. When dimensioning the system power supply, make sure that the minimum voltage on the encoder is not underranged due to the voltage drop on the board and in the encoder connection cable.

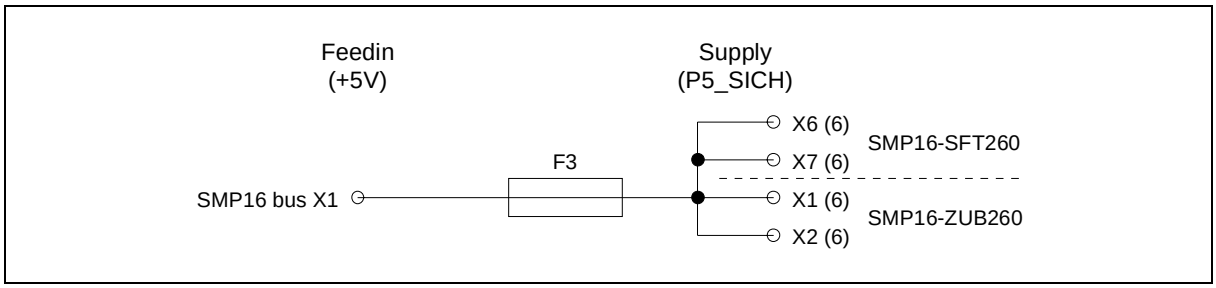



Figure 2.5 Internal wiring of the 5 V encoder power supply with SMP16-ZUB260

The 24 V encoder power supply must be provided externally. The power can be fed in via one of the encoder connections or via the X5 connection. The latter is particularly recommended when several encoders are to be powered this way.

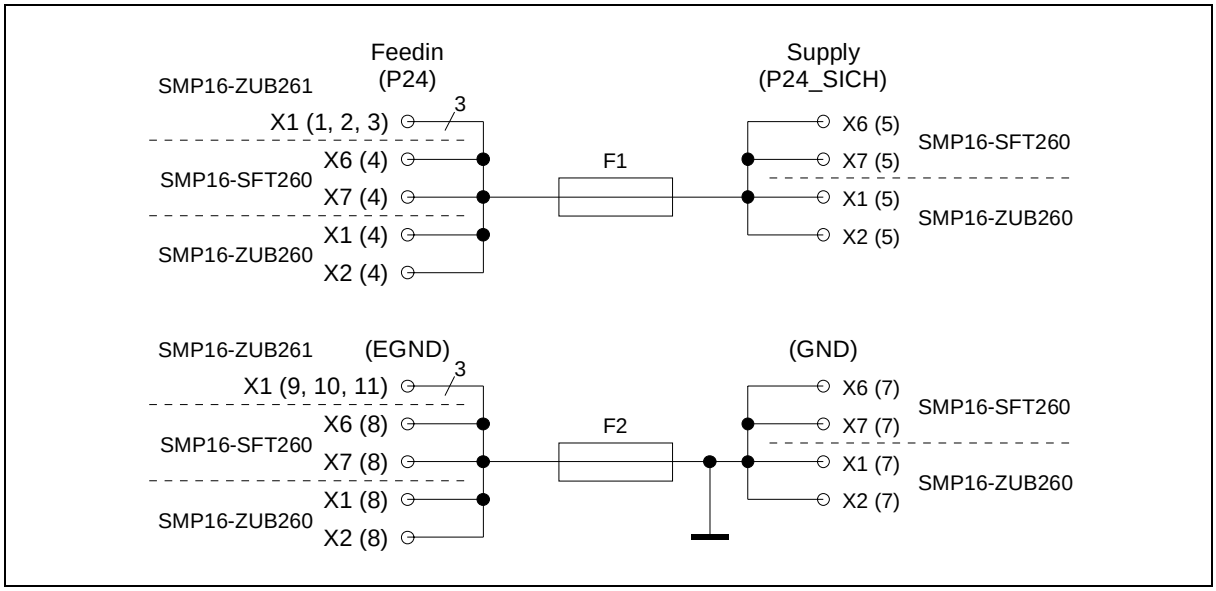



Figure 2.6 Internal wiring of the 24 V encoder power supply with SMP16-ZUB260 and SMP16-ZUB261

**Notes:**
To ensure the interference immunity of the entire SICOMP system, only 24 V encoders should be used when long distances have to be covered or the environment contains strong interference.

The 24 V supply voltage is only passed on to the encoder connections via safety fuses. Interference immunity against voltage fluctuations or drops must be ensured by the encoder being used.

## 2.7 Overview of the Interfaces

Table 2.1 Connection elements of the board

| Con. | Design | Use |
|---|---|---|
| X1 | Multi-point terminal strip, 96-pin | SMP16 bus interface |
| X2 | Socket strip, 20-pin | Reserved |
| X3 | AMP Micromatch connector, 16-pin | Input, encoder channel 3 |
| X4 | AMP Micromatch connector, 16-pin | Input, encoder channel 4 |
| X5 | AMP Micromatch connector, 16-pin | Gate inputs and 24 V power |
| X6 | Sub D socket, 15-pin | Input, encoder channel 1 |
| X7 | Sub D socket, 15-pin | Input, encoder channel 2 |

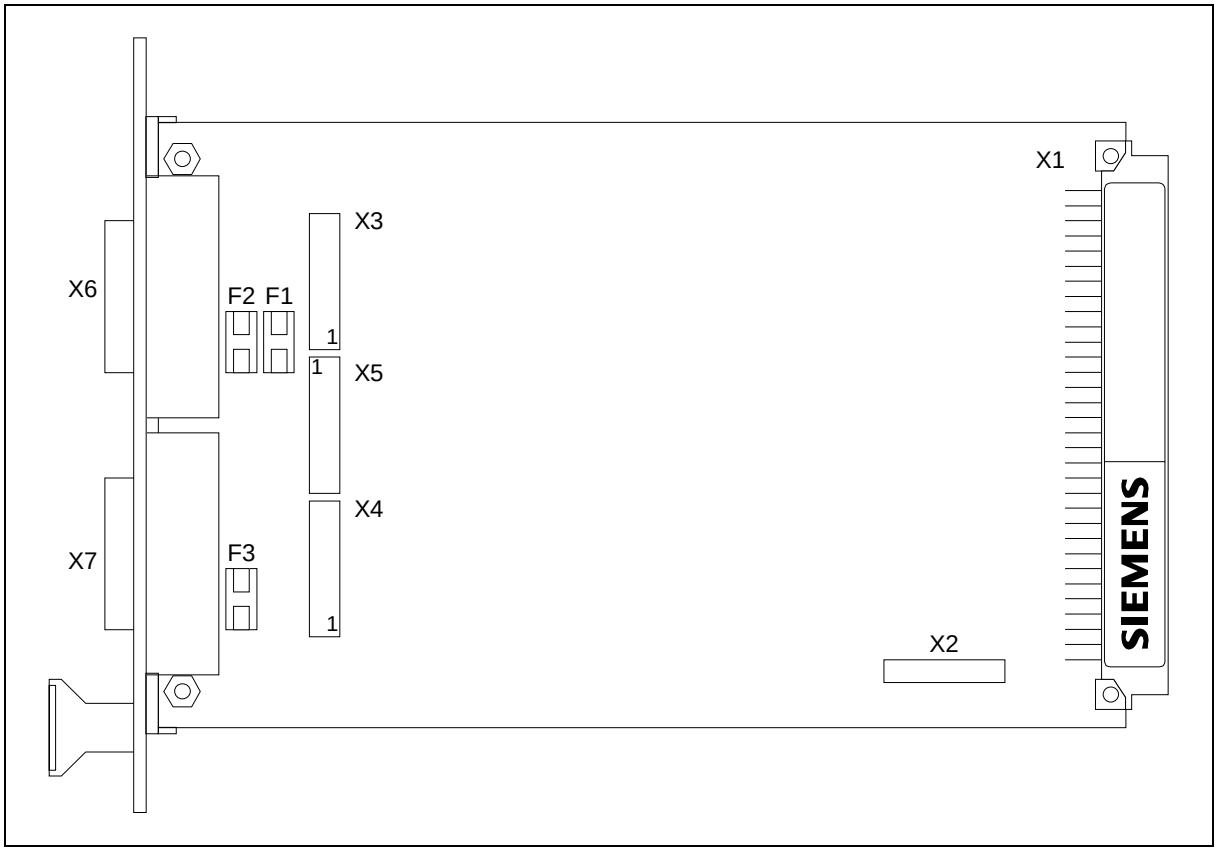



Figure 2.7 Location of the connection elements

## 2.8 Fuses

Table 2.2 Fuses on the board

| Fuse | Design | Use |
|---|---|---|
| F1 | SMD, 750 mA, rapid-action [1)] | 24 V power (P24) |
| F2 | SMD, 750 mA, rapid-action [1)] | Reference potential for 24 V power (EGND) |
| F3 | SMD, 750 mA, rapid-action [1)] | 5 V encoder power supply (outputs) |

*1) Order number R451.750 from Littlefuse*

For the location of the fuses on the board, see Figure 2.7.

## 2.9 Operational Values

| | | |
|---|---|---|
| **Voltage Supply from the SMP16 Bus** | | |
| Nominal voltage | | +5 V ±5 % [1] |
| Current consumption (without 5 V encoder power) | Typ. | 0.4 A |
| **Encoder interfaces** | | |
| Number | | 4 |
| Physical interface design of encoder signals A, B and N or CLK and DAT | | RS 485/RS 422 |
| Input frequency for incremental encoders | Without wire break monitoring<br>With wire break monitoring | Max. of 1.25 MHz<br>Max. of 200 kHz |
| Data width for SSI encoders | | 13, 21 and 25 bits |
| Clock pulse supply of the encoder ASICs | | 10 MHz |
| **SSI encoder (CLK)** | | |
| Error-voltage clock-pulse output (at $R_L$ = 330 Ω) | Typ. | 3 V |
| Shift clock pulse | | 78 kHz to 1.25 MHz |
| **Incremental encoder (A, B, N) / SSI encoder (DAT)** | | |
| Error voltage for wire break monitoring (at $R_L$ = 110 Ω) | Min. | ±2.5 V |
| Error voltage without wire break monitoring | | In accordance with RS 422/RS 485 |
| Common mode voltage with wire break monitoring | Max. | 2.75 V |
| Common mode voltage without wire break monitoring | Max. | 10 V |
| Clock pulse cycle for SSI encoders | Min. | 800 nsec |
| Delay, clock pulse → data | Max. | 300 nsec |
| Time requirements for incremental encoder | | See chapter 2.10. |
| **Gate inputs** | | |
| Number | | 4 |
| Input voltage, low level | | –3 to +5 V |
| Input voltage, high level | | +15 to +30 V |
| Input current, high level | Typ.<br>Max. | 8 mA<br>10 mA |
| Switching time | Max. | 50 µsec |
| **5 V encoder power supply (outputs)** | | |
| Single current consumption, encoder channels 1 and 2 | Max. | 0.72 A |
| Single current consumption, encoder channels 3 and 4 | Max. | 0.2 A |
| Total current of all encoder channels | Max. | 0.72 A |
| Conducting-state d.c. resistance of the encoder power supply | Typ. | 0.6 Ω [1] |
| **24 V encoder power supply** | | |
| Fed in supply voltage (P24 against EGND) | | 0 to 28.8 V |
| Single current consumption, encoder channels 1 and 2 | Max. | 0.72 A |
| Single current consumption, encoder channels 3 and 4 | Max. | 0.2 A |
| Total current of all encoder channels | Max. | 0.72 A |
| Conducting-state d.c. resistance of the encoder power supply | Typ. | 1.2 Ω |

*1) With the 5 V encoder power supply, make sure that the minimum voltage on the encoder is not underranged.*

Additional general prerequisites (e.g., environmental requirements) are listed in the SICOMP IMC system manual. See chapter 2.12.

## 2.10 Time Requirements for Incremental Encoders

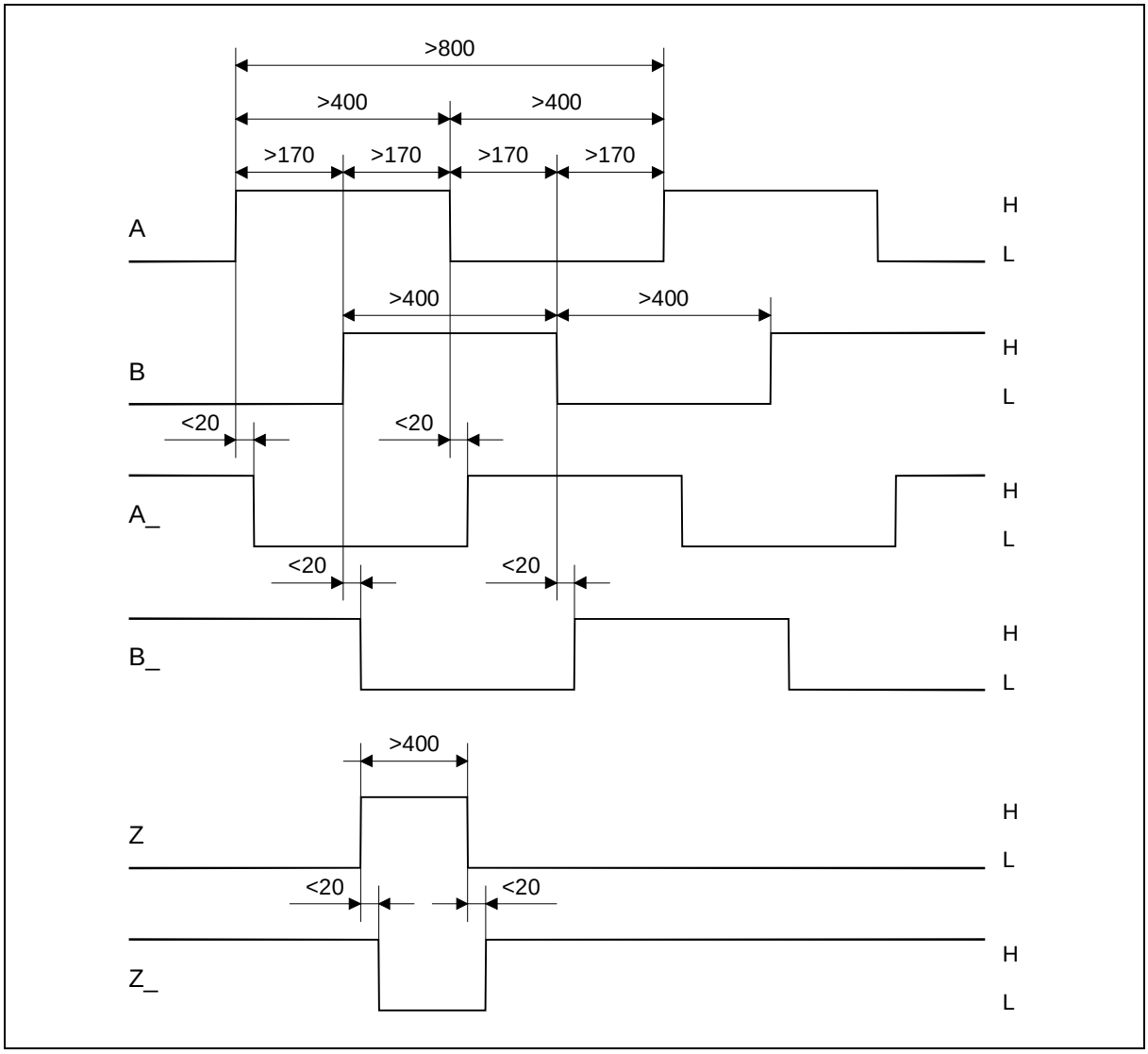



Figure 2.8 Time requirements for the signals of incremental encoders (specified in nanoseconds)

## 2.11 Time Requirements on the SMP16 Bus Interface

The command recovery time between two write accesses must be greater than 115 nsec.

## 2.12 Recommended Accessories

**SMP16-AKO**

Autoconfiguration software for MS-DOS and Windows to set the SMP bus interface

Order number: 6AR1400-0FA10-3AA0

The product includes online help with a detailed description of the function and handling of the configuration software.

**SMP16-ZUB260**

Front plate, single width, with two 15-pin sub D sockets for connection of encoder channels 3 and 4.

Order number: 6AR1508-0AA16-0AA0

**SMP16-ZUB261**

Front plate, single width, with a 15-pin sub D pin strip for connection of the gate inputs (see chapter 3.2.3) and for feeding in the 24 V encoder power supply

Order number: 6AR1508-0AA17-0AA0

**SICOMP IMC System Manual**

Order number: 6AR1950-7AA00-2CA0

The system manual is also available from the Internet in PDF files.

http://www.ad.siemens.de/faq_sev3/html_76/support.htm

# 3 Interfaces

## 3.1 Pin Connector X1 to SMP16 Bus

The following table shows the bus signals used by the board.

| Connection | a | b | c |
|---|---|---|---|
| 1 | – | A16 | – |
| 2 | – | A17 | GND |
| 3 | – | **AEN** | +5 V |
| 4 | – | – | MMIO* |
| 5 | MEMCS16* | – | A12 |
| 6 | RESET* | – | A0 |
| 7 | – | – | A13 |
| 8 | MEMR* | – | A1 |
| 9 | RESIN* | – | A14 |
| 10 | MEMW* | – | A2 |
| 11 | – | **ACEN** | A15 |
| 12 | RDYIN | – | A3 |
| 13 | BUSEN | **ACDONE** | **NMI*** |
| 14 | DB0 | – | A4 |
| 15 | – | +5 V | – |
| 16 | DB1 | GND | A5 |
| 17 | – | GND | – |
| 18 | DB2 | – | A6 |
| 19 | – | – | – |
| 20 | DB3 | – | A7 |
| 21 | IOCS16* | – | – |
| 22 | DB4 | DB8 | A8 |
| 23 | – | DB9 | – |
| 24 | DB5 | DB10 | A9 |
| 25 | – | DB11 | – |
| 26 | DB6 | DB12 | A10 |
| 27 | – | DB13 | **INT1*** |
| 28 | DB7 | DB14 | A11 |
| 29 | – | DB15 | **INT2*** |
| 30 | IOW* | BHEN | IOR* |
| 31 | – | A18 | GND |
| 32 | +5 V | A19 | – |

### 3.1.1 Interrupt Signals

**INT1*, INT2*** Interrupt outputs, open collector (c27, c29)

Interrupts of the encoder ASICs. See chapter 6.2.

- INT1*: Encoder channels 1 and 2, time-measuring channel 1
- INT2*: Encoder channels 3 and 4, time-measuring channel 2

**NMI*** Non Maskable Interrupt, output, open collector (c13)
Characteristics: low: 0.4 V/8 mA

Can be connected with the NMI* or IOCHCK* input to the CPU

This output signals an irresolvable access conflict on one of the encoder ASICs. This state can only occur when hardware is defective.

The NMI* outputs of several boards can be combined.

### 3.1.2 Signals for the Daisy Chain

**ACEN,**
**ACDONE** Input (b11)
Output, open collector (b13)

The ACEN input signals a board that it has been selected for configuration of the ASBIC chip. Using the ACDON output, it indicates that it has finished its own configuration and the next board can be configured. See chapter 1.1.

### 3.1.3 Other Special Signals

**AEN** Address Enable, input (b3)

Control signal for PC–compatible bus accesses, must be connected with AEN (b3) to the CPU slot for PC-I/O addressing (up to 3FFh).

# 3.2 Interfaces of the Board

## 3.2.1 Inputs for Encoder Channels 1 and 2 (X6 and X7)

The inputs of encoder channels 1 and 2 (X6 and X7) are 15-pin sub D sockets on the front plate of the SMP16-SFT260. The signal allocation depends on the type of encoders used. See also chapter 1.4.

Table 3.1 Allocation of X6 and X7

| Pin | For Incremental Encoders | | For SSI Encoders | |
|---|---|---|---|---|
| | **Signal Name** | **Meaning** | **Signal Name** | **Meaning** |
| 1 | GSYNC*n* | Gate input | – | Reserved |
| 2 | B*n* | Encoder track B | CLK*n* | Clock pulse output |
| 3 | B*n*_ | Encoder track B inverted | CLK*n*_ | Clock pulse output inverted |
| 4 | P24 | 24 V power | | |
| 5 | P24_SICH | 24 V encoder power supply, with fuse protection | | |
| 6 | P5_SICH | 5 V encoder power supply, with fuse protection | | |
| 7 | GND | Reference potential for encoder power supply | | |
| 8 | EGND | Reference potential for 24 V power | | |
| 9 | GSYNC*n*_ | Gate input inverted | – | Reserved |
| 10 | N*n* | Encoder zero mark | – | Reserved |
| 11 | N*n*_ | Encoder zero mark inverted | – | Reserved |
| 12 | B*n*_ | Encoder track B inverted | CLK*n*_ | Clock pulse output inverted |
| 13 | B*n* | Encoder track B | CLK*n* | Clock pulse output |
| 14 | A*n*_ | Encoder track A inverted | DAT*n*_ | Data input inverted |
| 15 | A*n* | Encoder track A | DAT*n* | Data input |

*n = Encoder channel number*

**Note:**
When SSI encoders are used, the unused N track signals are circuited as outputs. This ensures that wire break monitoring functions reliably.

In observer mode with SSI encoders, the clock pulse signal is circuited as an input. The zero marking signal must be terminated to prevent a permanent wire break message for this signal. See chapter 1.4.2.

### 3.2.2 Inputs for Encoder Channels 3 and 4 (X3 and X4)

The inputs of encoder channels 3 and 4 (X3 and X4) are 16-pin AMP Micromatch connectors on the SMP16-SFT260. The signal allocation depends on the type of encoders used.

Table 3.2 Allocation of X3 and X4

| Pin | For Incremental Encoders | | For SSI Encoders | |
|---|---|---|---|---|
| | **Signal Name** | **Meaning** | **Signal Name** | **Meaning** |
| 1 | GSYNC*n* | Gate input | – | Reserved |
| 2 | GSYNC*n*_ | Gate input inverted | – | Reserved |
| 3 | B*n* | Encoder track B | CLK*n* | Clock pulse output |
| 4 | N*n* | Encoder zero mark | – | Reserved |
| 5 | B*n*_ | Encoder track B inverted | CLK*n*_ | Clock pulse output inverted |
| 6 | N*n*_ | Encoder zero mark inverted | – | Reserved |
| 7 | P24 | 24 V power | | |
| 8 | B*n*_ | Encoder track B inverted | CLK*n*_ | Clock pulse output inverted |
| 9 | P24_SICH | 24 V encoder power supply, with fuse protection | | |
| 10 | B*n* | Encoder track B | CLK*n* | Clock pulse output |
| 11 | P5_SICH | 5 V encoder supply, with fuse protection | | |
| 12 | A*n*_ | Encoder track A inverted | DAT*n*_ | Data input inverted |
| 13 | GND | Reference potential for encoder power supply | | |
| 14 | A*n* | Encoder track A | DAT*n* | Data input |
| 15 | EGND | Reference potential for 24 V power | | |
| 16 | – | Not used | | |

*n = Encoder channel number*

**Note:**
When the SMP16-ZUB260 accessory module is used, encoder channel 3 is available on X1 on the module's front plate, and encoder channel 4 is available on X2. The signal allocation on the sub D sockets of the accessory module is then identical to that of X6 and X7. See chapter 3.2.1.

### 3.2.3 Gate Inputs and 24 V Power (X5)

X5 is a 16-pin AMP Micromatch connector on the SMP16-SFT260.

Table 3.3 Allocation of X5

| Pin | Signal Name | Meaning |
|---|---|---|
| 1 | – | Not used |
| 2 | P24 | 24 V power |
| 3 | EGND | Reference potential for 24 V power |
| 4 | P24 | 24 V power |
| 5 | EGND | Reference potential for 24 V power |
| 6 | P24 | 24 V power |
| 7 | EGND | Reference potential for 24 V power |
| 8 | – | Not used |
| 9 | GSYNC4_ | Gate input, encoder channel 4 inverted |
| 10 | GSYNC4 | Gate input, encoder channel 4 |
| 11 | GSYNC3_ | Gate input, encoder channel 3 inverted |
| 12 | GSYNC3 | Gate input, encoder channel 3 |
| 13 | GSYNC2_ | Gate input, encoder channel 2 inverted |
| 14 | GSYNC2 | Gate input, encoder channel 2 |
| 15 | GSYNC1_ | Gate input, encoder channel 1 inverted |
| 16 | GSYNC1 | Gate input, encoder channel 1 |

When the SMP16-ZUB261 accessory module is used, the gate inputs and the encoder power supply are available on the module's X1 sub D plug connector. The following signal allocation is used.

Table 3.4 Allocation of X1 on SMP16-ZUB261

| Pin | Signal Name | Meaning |
|---|---|---|
| 1 | P24 | 24 V power |
| 2 | P24 | 24 V power |
| 3 | P24 | 24 V power |
| 4 | – | Not used |
| 5 | GSYNC4 | Gate input, encoder channel 4 |
| 6 | GSYNC3 | Gate input, encoder channel 3 |
| 7 | GSYNC2 | Gate input, encoder channel 2 |
| 8 | GSYNC1 | Gate input, encoder channel 1 |
| 9 | EGND | Reference potential for 24 V power |
| 10 | EGND | Reference potential for 24 V power |
| 11 | EGND | Reference potential for 24 V power |
| 12 | GSYNC4_ | Gate input, encoder channel 4 inverted |
| 13 | GSYNC3_ | Gate input, encoder channel 3 inverted |
| 14 | GSYNC2_ | Gate input, encoder channel 2 inverted |
| 15 | GSYNC1_ | Gate input, encoder channel 1 inverted |

# 4 Configuration with Software

The configuration data of the SMP16-SFT260 are stored by the ASBIC chip on the serial EEPROM of the board. The tables below show the default settings of the values which can be changed by the automatic configuration software SMP16-AKO.

**Note:**
The configuration data must be adjusted each time a system is changed by inserting or removing a board or module since the board or the module may not be able to be addressed otherwise.

## Required settings in the "chip select channel 0 to 3" dialog fields

| Channel | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| Setting | **Enabled** | Disabled | Disabled | Disabled |
| Address mode | **SMP-I/O** | SMP-I/O | SMP-I/O | SMP-I/O |
| Base address | **400 hex** | 400 hex | 400 hex | 400 hex |
| Address range | 64 bytes | 1 byte | 1 byte | 1 byte |
| Function | Registers of the SFT260 | Not used | Not used | Not used |

***Bold*** *Sample values which you must change to meet your own requirements*

The base address of chip select channel 0 must be a whole number which is divisible by 64 (40h) (e.g., 400h, 440h, 480h, and so on).

## Default settings in the "ASBIC channel settings" dialog field

| Parameters | Default Setting |
|---|---|
| ASBIC channel | Disabled |
| Address mode | PC-I/O |
| Base address | 200 hex |

## Default settings in the "general" dialog field

| Parameters | Default Setting |
|---|---|
| Memory address range | Includes MMIO range |

# 5 Programming the Board

The SMP16-SFT260 occupies a 64-byte consecutive address area which must begin with a base address which is divisible by 64 (40h).

**Note:**
The board can be addressed by byte or by word. Word accesses must use even addresses. When byte accesses are used, the low byte must be read or written first and then the high byte.

Table 5.1 Organization of the board's address area

| Address Offset | Write Access | Read Access |
|---|---|---|
| 00h to 07h | Encoder channel 1 of the board (channel 1 of the GE2003N-1) | |
| 08h to 0Fh | Encoder channel 2 of the board (channel 2 of the GE2003N-1) | |
| 10h to 15h | Time-measuring channel 1 of the board (channel 3 of the GE2003N-1) | |
| 16h | EPLD register 1 | |
| 18h | EPLD register 2 | |
| 1Ah | EPLD register 3 | |
| 1Ch | Reserved | Status register GE2003N-1 |
| 1Eh | Interrupt mask register of the GE2003N-1 (INT1) | |
| 20h to 27h | Encoder channel 3 of the board (channel 1 of the GE2003N-2) | |
| 28h to 2Fh | Encoder channel 4 of the board (channel 2 of the GE2003N-2) | |
| 30h to 35h | Time-measuring channel 2 of the board (channel 3 of the GE2003N-2) | |
| 36h to 3Bh | Reserved | |
| 3Ch | Reserved | Status register GE2003N-2 |
| 3Eh | Interrupt mask register of the GE2003N-2 (INT2) | |

Each encoder channel occupies 8 byte-addresses on the GE2003N ASICs which are set up identically.

Table 5.2 Organization of the address area of an encoder channel

| Address | Write Access | Read Access |
|---|---|---|
| x + 0 | Command register | Output register A |
| x + 2 | Counting operating mode: Reset counter A, B<br>Write operating mode: Parameterization of the zero crossing monitor | Output register B |
| x + 4 | Comparison register A | Shift internal sequence counter |
| x + 6 | Comparison register B | Shift internal sequence counter |

*x = Base address of the respective encoder channel*

Each time-measuring channel occupies 6 byte-addresses on the GE2003N ASICs which are set up identically.

Table 5.3 Organization of the address area of a time-measuring channel

| Address | Write Access | Read Access |
|---|---|---|
| x + 0 | Command register | Output register A |
| x + 2 | Counting operating mode: Reset counter A, B | Output register B (irrelevant) |
| x + 4 | Comparison register A | Shift internal sequence counter (irrelevant) |

*x = base address of the respective encoder channel*

## 5.1 EPLD Register 1

Table 5.4 Meaning of bits 0 to 7 in EPLD register 1

| Access | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read | LBR4 | LBR3 | GATE4 | GATE3 | LBR2 | LBR1 | GATE2 | GATE1 |
| Write | RLBR4 | RLBR3 | – | – | RLBR2 | RLBR1 | – | – |

**GATE1 to GATE4** Status on gate input (encoder channels 1 to 4)

0: Low (0 V)
1: High (24 V)

**LBR1 to LBR4** Status of wire break identification (encoder channels 1 to 4)

0: No wire break
1: Wire break

**RLBR1 to RLBR4** Reset wire break message (encoder channels 1 to 4)

0: Do not reset
1: Reset

Bits 8 to 15 can be disregarded.

**Note:**
The values written in EPLD register 1 cannot be read back.

### Status after reset

Depends on the levels on the gate inputs and the status of wire break monitoring

## 5.2 EPLD Register 2

Table 5.5 Meaning of bits 0 to 7 in EPLD register 2

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| INVGATE4 | INVGATE3 | EN_GATE4 | EN_GATE3 | INVGATE2 | INVGATE1 | EN_GATE2 | EN_GATE1 |

**EN_GATE1 to EN_GATE4** Enable gate function for track signals (encoder channels 1 to 4). See chapter 2.4.

0: Gate function inactive
1: Gate function active

**INVGATE1 to INVGATE4** Active level of the gate input signal (encoder channels 1 to 4)

0: Active level = high (+24 V)
1: Active level = low (0 V)

**Caution**

The gate function may only be activated with incremental encoders.

Bits 8 to 15 can be disregarded.

### Status after reset

00h

## 5.3 EPLD Register 3

Table 5.6 Meaning of bits 0 to 7 in EPLD register 3

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| – | – | BANM4 | BANM3 | – | – | BANM2 | BANM1 |

**BANM1 to BANM4** Gate function for zero marking signal (encoder channels 1 to 4). See chapter 2.4.

0: Gate function inactive
1: Gate function active

Bits 8 to 15 can be disregarded.

### Status after reset

CCh

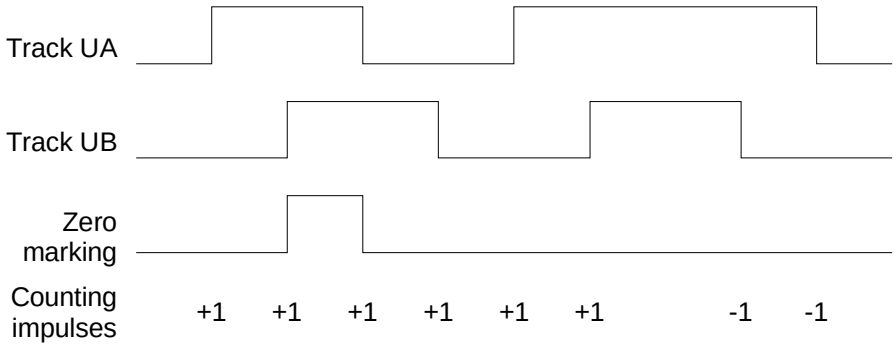
# 6 Encoder ASIC GE2003N

## 6.1 Operating Modes for Position Encoding

The encoder controller GE2003N has two primary operating modes based on the type of encoder.

- **Counting/screwing** for incremental encoders
- **Shifting** with SSI (i.e., synchronous serial interface) for absolute value encoders

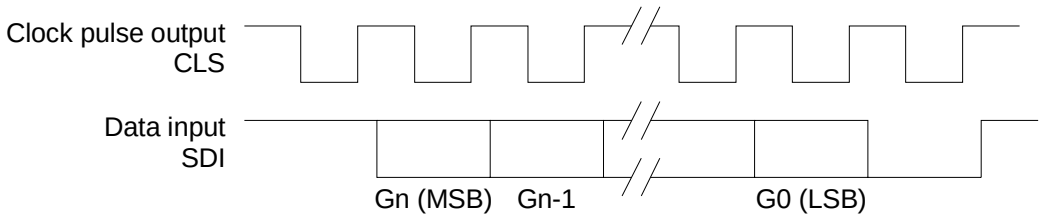
### Principle of counting/screwing for two-track encoders




Incremental encoders supply two pulses displaced by 90 degrees (UA and UB). These are counted with the correct sign up to a length of 16 bits (counter A or counter B). The current counting value can be read at all times by the microprocessor.

When the zero marking pulse signal (N) arrives, the counting value (counter A) is stored in output register B when the **counting** operating modes are being used. This can also be read by the microprocessor at all times.

### Principle of SSI




The controller (SSI control) sends 13, 21 or 25 clock pulses (can be parameterized in the command register) to the absolute value encoder. Its SSI accepts the internally, simultaneously queued data in a shift register the first time the clock pulse signal changes from high to low. The first time the clock pulse signal changes from low to high, the most significant bit (MSB) of the gray-coded angle information is applied to the serial data input (SDI) of the GE2003N. At each additional rising edge, the next less significant bit is shifted to the data input. After the least significant bit (LSB) has been transferred, the data line switches to low until monoflop time $t_m$ has expired. The data line thus indicates that the absolute value encoder is not yet ready for an additional transmission. The encoder is ready for further transmissions when the data line switches to high again.

Six operating modes can be derived from the two primary operating modes.

1. **Counting with direction discriminator** (RDC) for two-track incremental encoders
2. **Counting without direction discriminator** for single-track incremental encoders
3. **Screwing with direction discriminator** for two-track incremental encoders
4. **Screwing without direction discriminator** for single-track incremental encoders
5. **Shifting** for encoders with SSI
6. **Observer mode** for test purposes with SSI

An operating mode with its related options is set by writing in the command register.

### 6.1.1 Counting with Direction Discriminator

Track signals UA and UB, and zero marking pulse N pass through a digital filter with a limit frequency based on the frequency of the system clock pulse.

Table 6.1 Limit frequency of the filter based on the system clock pulse

| **Clock Pulse Frequency $f_{Cl}$ (MHz)** | **Limit Frequency of the Filter $f_g$ (MHz)** |
|---|---|
| 8 | 1.33 |
| **10** | **1.66 (used with SMP16-SFT260)** |
| 12 | 2.0 |
| 16 | 2.66 |

The direction discriminator (RDC) generates a counting impulse (CNTOUT) and a counting direction signal (UP) from the two track signals UA and UB. These two signals are fed directly to up/down counter A.

Counter A counts the signals with the correct sign up to a length of 16 bits. The direction of counting can be parameterized by inverting input UA with a command. This creates a counting impulse which increments or decrements counter A. The counting value can be read out at all times via 16-bit output register A.

**Note:**
After a hardware reset, counter A is incremented if track A is high.

The zero marking pulse of the encoder is connected to the N input of the GE2003N.

The following N input functions can be parameterized.

- For rising and falling edge on input N: The counter status of counter A is latched in the 16-bit output register B, and an interrupt which can be masked is generated.
- For rising edge only: The counter status is latched in output register B, and an interrupt which can be masked is generated.
- For falling edge only: The counter status is latched in output register B, and an interrupt which can be masked is generated.

Although counter A cannot be loaded, it can be reset with a hardware reset or a command.

### 6.1.2 Counting without Direction Discriminator

The counting signal is fed to input UA and passes through a digital filter with a limit frequency based on the frequency of the system clock pulse. See chapter 6.1.1. It can be parameterized whether counting is to be performed with the rising or falling edge of UA. Input UB is not used.

The parameterized CNTOUT counting signal is fed directly to counter A as a counting impulse signal. Counter A is permanently set to counting up. It counts the CNTOUT signal up to a length of 16 bits. The counting value can be read out at all times via 16-bit output register A.

The functions of input N are the same for the modes **counting with direction discriminator** and **counting without direction discriminator**. See chapter 6.1.1.

### 6.1.3 Screwing with Direction Discriminator

Track signals UA and UB are fed to the direction discriminator (RDC) via the digital filter. The outputs of the direction discriminator, the CNTOUT counting impulse and the UP counting direction signal are fed to the outside via pins. The CNTOUT counting pulse is verified externally with a factor. The verified signal is fed to the GE2003N via CNTIN and synchronized. The duration of the CNTIN impulse must be at least one clock pulse cycle. When counting up (UP is low), 16-bit counter A is incremented. When counting down (UP is high), 16-bit counter B is incremented.

The direction of counting can be parameterized by inverting the UA input with a command.

The value of counter A can be read out at all times via 16-bit output register A. The value of counter B can also be read out at all times via 16-bit output register B.

Although counters A and B cannot be loaded, they can be reset with a hardware reset or a command.

### 6.1.4 Screwing without Direction Discriminator

The counting signal is fed to input UA and passes through a digital filter with a limit frequency based on the frequency of the system clock pulse. See chapter 6.1.1. It can be parameterized whether counting is to be performed with the rising or falling edge of UA. Input B is not used.

The parameterized CNTOUT counting signal is fed to the outside and verified externally with a factor. The verified signal is fed to the GE2003N via CNTIN and synchronized. The duration of the CNTIN impulse must be at least one clock pulse cycle. The direction of screw rotation is specified with a software bit. This is also fed via UP to the external factor-verification logic.

When counting the verified signal in the up direction, 16-bit counter A is incremented. When counting down, 16-bit counter B is incremented.

The value of counter A can be read out at all times via 16-bit output register A. The value of counter B can also be read out at all times via 16-bit output register B.

Although counters A and B cannot be loaded, they can be reset with a hardware reset or a command.

### 6.1.5 Command Register for Counting/Screwing

The various operating modes with their options can be set by writing in the command register.

| **Command bit** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** |
|---|---|---|---|---|---|---|---|---|
| | x | X | X | X | X | X | X | ÜV |
| **Command bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| | ÜZ | N1 | N0 | DRB | DRA | BA2 | BA1 | BA0=0 |

The remaining command bits have the following meaning for the **counting/screwing** primary operating modes (BA0 = 0).

**BA1, BA2** Setting the operating mode

| **Operating Mode** | **Command Bit** | |
|---|---|---|
| | **BA2** | **BA1** |
| Counting with RDC | 0 | 0 |
| Counting without RDC | 0 | 1 |
| Screwing with RDC | 1 | 0 |
| Screwing without RDC | 1 | 1 |

**DRA** Counting direction for counting/screwing with RDC:
DRA = 0: Normal counting direction (track UA not inverted)
DRA = 1: Inverted counting direction (track UA inverted)
or

Edge evaluation for counting/screwing without RDC:
DRA = 0: Rising edge of UA generates counting impulse.
DRA = 1: Falling edge of UA generates counting impulse.

**DRB** Counting direction for screwing without RDC:
DRB = 0: Counting up. (Counter A is activated.)
DRB = 1: Counting down. (Counter B is activated.)

**N0, N1** Zero marking pulse function (parameterization of which edge of zero marking pulse signal N is to cause the counter value to be latched in output register B)

| **Parameterized Edge** | **Command Bit** | |
|---|---|---|
| | **N1** | **N0** |
| Zero marking pulse edges are not evaluated. | 0 | 0 |
| Rising | 0 | 1 |
| Falling | 1 | 0 |
| Rising and falling | 1 | 1 |

**ÜZ** Monitoring of counting direction
ÜZ = 1: Monitoring active

**ÜV** Monitoring of counting up
ÜV = 1: Monitoring in forward direction

**x** Not used

### 6.1.6 Comparator for Counting/Screwing

A 16-bit value can loaded to comparison register A for the 4 operating modes (i.e., **counting with/without direction discriminator** and **screwing with/without direction discriminator**). If this value matches counter value A, an interrupt which can be masked is generated. A new interrupt is not generated until the comparison register has previously been written again. An unfulfilled comparison can be resolved by loading comparison register B.

The result of the comparison is fed to the outside via the VGL pin for the **counting with/without direction discriminator** modes (VGL = "1" if comparison fulfilled). This pin has a different function for the **screwing with/without direction discriminator** modes. The result of the comparison is reset (i.e., VGL becomes "0") when the comparison register is written.

If the position for the comparison value is more than $2^{16}$ increments away, the final comparison value cannot be loaded immediately. An intermediate value of up to $2^{16}$–1 increments would have to be loaded instead. When this intermediate value is reached, the final value or the next intermediate value can then be loaded.

### 6.1.7 Shifting with the Synchronous Serial Interface (SSI)

The data of an SSI encoder are pulsed right-justified in the 32-bit shift register (A and B). The number of clock pulse groups which are output can be parameterized. The values 13, 21 and 25 can be used.

The data of the SSI encoder are fetched either continuously (i.e., continuous mode) or with a start command (i.e., single-fetch mode). The arrival of a new value is reported via an interrupt (can be masked) after the stop bit is detected.

The data pass through a gray/dual converter (GDW) which can be switched off. The start bit and the stop bit are scanned for 1 and 0. The result is indicated as an error bit at position $2^{31}$ of the actual value transferred with the error, and reported as an interrupt which can be masked.

The shift clock pulse can be parameterized. Shift frequencies from 62 kHz to 2 MHz can be selected depending on the frequency of the system clock pulse. See table of baud rates in chapter 6.1.9. In contrast to the GE2003, with the GE2003N the first low impulse of the shift sequence is **not** twice as long as the others. The monoflop time of the encoder must only be longer than **one** clock pulse period of the shift clock pulse and not 1.5 clock pulse periods.

To conform to the monoflop time of the encoder, the pauses between two consecutive shift procedures can be parameterized in continuous operating mode. Pauses of 16 to 256 µsec can be set depending on the frequency of the system clock pulse. See table on pause times in chapter 6.1.9 .

The duration of one complete shift procedure can be optimized by parameterizing the pause time. The shift cycle duration depends on the number of bits of the clock pulse group and the pause time parameterized. The wide range of possible pause time settings permits use of standard encoders with 15 to 40 µsec monoflop times even with highest shift frequencies of 1 MHz.

At the end of every transmission the actual values are transferred from the A and B shift registers to the A and B output registers. After the A output register has been read by the processor, the two output registers are not updated until register B has also been read even when additional actual values have been transferred with the SSI protocol in the meantime. This ensures that reliable actual values are always read.

### 6.1.8 Observer Mode for Test Purposes on the SSI

In **observer** mode the GE2003N can monitor the signals of the SSI (CLS and SDI). The following conditions apply.

- The internal shift clock pulse must correspond to the external shift clock pulse in frequency.
- The group of clock pulses received is not monitored for correct clock pulse number.
- The data of the encoder are acquired. Prerequisite: The number of bits parameterized in the command register corresponds to the number of bits of the encoder.
- Only the start bit is monitored. The monitoring result is indicated as an error bit at position $2^{31}$ of the actual value transferred with the error, and is reported as an interrupt which can be masked. There is no point in monitoring the stop bit since the monitoring channel cannot detect this bit (i.e., and cannot monitor it either) with the SSI protocol.

#### Starting observer mode:

If the master channel is on its own board, the observer channel should be activated first and then the master channel.

If the master channel is not on its own board, one shift procedure will have probably occurred already when observer mode is activated. The pause time of the master encoder must be at least as long as the duration of the transmission so that the observer channel can synchronize itself to the SSI protocol.

It is still difficult for the higher-level software of the observing channel to decide when synchronization has occurred and correct actual values are available. For this reason, initial actual values on the observer channel and any error messages should always be rejected.

The comparison registers should not be loaded until later so that initial incorrect values do not trigger the comparator prematurely.

#### Changing the comparison condition in observer mode

If the comparison condition was changed (e.g., from >= to <=) on the GE2003 by writing in the command register during observer mode, this also affected the command start bit which represents the internal operating state. If it was changed, a running transmission was terminated or a transmission was started.

With the GE2003N the command start bit does not represent the internal operating state during observer mode. Because it can be written with any values without affecting the function, the comparison condition can be changed at all times during observer mode.

### 6.1.9 Command Register during Shifting

The various operating modes with their options can be set by writing in the command register.

| **Command bit** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** |
|---|---|---|---|---|---|---|---|---|
| | x | X | BR2 | BR1 | BR0 | MZ2 | MZ1 | MZ0 |
| **Command bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| | GA1 | GA0 | GDE | ST | CON | VG | MH | BA0=1 |

The other command bits have the following meaning in primary operating mode **shifting** (BA0 = 1).

**MH**

Observer mode
MH = 0: Shift mode with SSI
MH = 1: Observer mode

**VG**

Comparator setting: greater than/less than
VG = 0: Interrupt if SSI data <= comparison value
VG = 1: Interrupt if SSI data >= comparison value

**CON**

SSI continuous /single-fetch
CON = 0: Single-fetch mode or stop for continuous mode
CON = 1: Continuous mode

**ST**

SSI start for single-fetch
ST = 0: Stop for single-fetch
ST = 1: SSI start

**GDE**

Gray/dual converter on/off
GDE = 0: Direct transmission of the bits
GDE = 1: Gray/dual converter on

**GA0, GA1**

Encoder type

| **Number of Encoder Bits** | **GA1** | **GA0** |
|---|---|---|
| 13 | 0 | 0 |
| 21 | 0 | 1 |
| 25 | 1 | 0 |

The combination GA1 = 1 and GA0 = 1 cannot be used since no useful shift procedures occur.

**MZ0 to MZ2**

Pause (monoflop time) plus 2 shift clock pulse periods

| **Monoflop Time (in µsec) Depending on the Clock Pulse Frequency** | | | | **Command Bit** | | | |
|---|---|---|---|---|---|---|---|
| 8 MHz | **10 MHz** [1)] | 12 MHz | 16 MHz | **MZ2** | **MZ1** | **MZ0** | **N** |
| 32 | **25.6** | 21.3 | 16 | 0 | 0 | 0 | 0 |
| 64 | **51.2** | 42.6 | 32 | 0 | 0 | 1 | 1 |
| 96 | **76.8** | 64.0 | 48 | 0 | 1 | 0 | 2 |
| 128 | **102.4** | 85.3 | 64 | 0 | 1 | 1 | 3 |
| 160 | **128.0** | 106.6 | 80 | 1 | 0 | 0 | 4 |
| 192 | **153.6** | 128.0 | 96 | 1 | 0 | 1 | 5 |
| 224 | **179.2** | 149.3 | 112 | 1 | 1 | 0 | 6 |
| 256 | **204.8** | 170.6 | 128 | 1 | 1 | 1 | 7 |

*1) These values must be used for SMP16-SFT260.*

When parameterized appropriately, maintenance of the monoflop time ($t_M$) of 15 to 40 µsec is ensured for standard encoders for all clock pulse frequencies between 8 and 16 MHz. In addition, other values for shorter or longer monoflop times can be achieved.

When clock pulse frequency ($f_{Cl}$) of the GE2003N and monoflop time ($t_M$) are specified, whole-number monoflop code N can be calculated with the following formula.

$$N = \frac{(t_M * f_{Cl})}{256} - 1$$

Restriction: $0 \leq N \leq 7$

Due to the internal design of the GE2003N hardware, the minimum monoflop time is 7 shift clock pulse periods even when a shorter monoflop time is parameterized.

In addition, 2 shift clock pulse periods must be added to the monoflop times specified above.

$$t_P = t_M + 2T_{CLS}$$

$t_P$: Pause between two transmissions
$t_M$: Monoflop time
$T_{CLS}$: Period duration of the shift clock pulse

**BR0 to BR2**

Baud rates

| **Shift Frequency (in MHz) for Clock Pulse Frequency of** | | | | **Command Bit** | | |
|---|---|---|---|---|---|---|
| 8 MHz | **10 MHz** [1)] | 12 MHz | 16 MHz | **BR2** | **BR1** | **BR0** |
| 1.0 | **1.25** | 1.5 | 2.0 | 0 | 0 | 0 |
| 0.5 | **0.625** | 0.75 | 1.0 | 0 | 0 | 1 |
| 0.25 | **0.313** | 0.375 | 0.5 | 0 | 1 | 0 |
| 0.125 | **0.156** | 0.188 | 0.25 | 0 | 1 | 1 |
| 0.062 | **0.078** | 0.094 | 0.125 | 1 | 0 | 0 |

*1) These values must be used for SMP16-SFT260.*

The other combinations of BR0 to BR2 are only used for special test modes.

### 6.1.10 Comparators for Shifting and Observing

In SSI mode, the comparison value is written right-justified in the two 16-bit comparison registers (A and B). The order in which this must be performed is shown below.

1. Load comparison register A.
2. Load comparison register B (even for 13-bit data format).

| Comparison Register B | | | Comparison Register A | | |
|---|---|---|---|---|---|
| 15 | Bit | 0 | 15 | Bit | 0 |
| MSB | | | | | LSB |

The data arriving from the encoder are compared serially with the value in the comparison register. Only the applicable right-justified bits of the A and B comparison registers are used for the comparison with SSI encoder data (13, 21 or 25-bit). (LSB = bit 0 of comparison register A, and MSB = bit 15 of comparison register B.) The remaining bits in the comparison register do not need to be loaded with a defined 0 or 1. In contrast to the GE2003, the comparator of the GE2003N does **not** ignore the LSB.

Since not every increment is transferred, the serial comparator must scan for <= or >= here. When the comparison condition is fulfilled for the first time, an interrupt which can be masked is generated. Another interrupt cannot be generated until comparison registers A **and** B are loaded again. Remember that comparison register A must be loaded first and then comparison register B.

The result of the comparison is fed to the outside with the VGL pin. The comparison result is reset (VGL is low) when the A and B comparison registers are write-accessed again.

The A and B comparison registers can be loaded at all times, even when a shift procedure is running or the comparator is enabled. The comparator is then disabled while the shift procedure is running. Not until the two A and B comparison registers have been loaded is the comparator enabled again for the beginning of a new shift procedure.

Whether a scan for <= or for >= is made depends on the traversing direction parameterized.

#### Reloading new comparison values

New comparison values can be reloaded and the comparison condition can be changed while an SSI transmission is in progress. The method is shown below.

- Loading of comparison register A disables the comparison.
- The comparison condition can now be changed if desired.
- Loading of comparison register B enables the comparison again, and a new comparison result is determined for the next SSI transmission.

SSI transmissions in progress may not be interrupted.

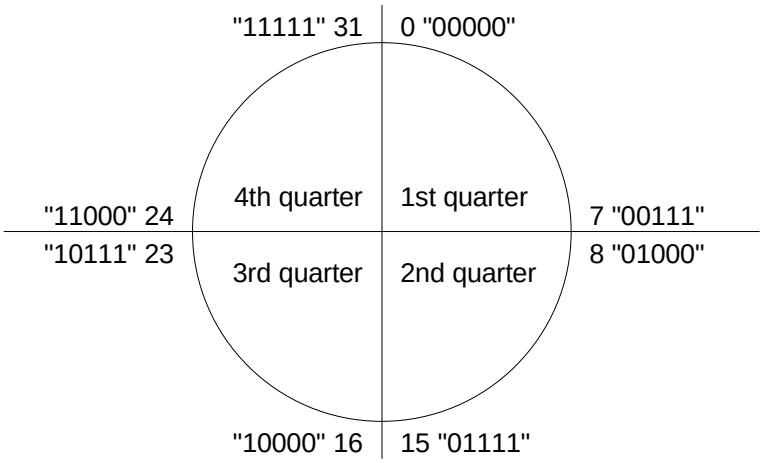
If the SSI transmission is stopped, the comparison remains in force when this does not occur during processing (i.e., after the end of a single-fetch or during the monoflop time for continuous operation). Stopping while an SSI transmission is running destroys the comparison values and the comparison is disabled.

A comparison with the actual value is **not** performed when a start/stop bit error occurs during the SSI transmission.

### 6.1.11 Monitoring the Zero Crossing for SSI Encoders

Zero crossing is detected when the two most significant bits of the absolute value encoder change from "11" to "00" (i.e., zero crossing in forward direction) or vice versa (i.e., zero crossing in backward direction). If you picture the counting range of the absolute value encoder as a circle, this means a jump from the 4th quarter to the 1st quarter or vice versa.

The following figure shows an example (total encoder steps = 32). The two most significant bits of the binary numbers code the quarters.




When zero crossing occurs, a status bit is set which also has interrupt capability. The status register (see chapter 6.2.4) is shown below for shift mode.

| **Status bit** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** |
|---|---|---|---|---|---|---|---|---|
| | VS1 | VS0 | x | AÜ | VG3 | VG2 | VG1 | NW3 |
| **Status bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| | NW2 | NW1 | ND3 | ND2 | ND1 | SS3 | SS2 | SS1 |

Status bits ND3 to ND1 are shown for the respective channel during zero crossing. These bits are also inserted at the same position in the interrupt mask register. See chapter 6.2.5.

When a single-turn encoder with the 13-bit SSI protocol is being used, it is obvious that the two most significant bits are SSI data bits 12 and 11. When multi-turn encoders are being used, the position of the monitored data bits in the 25-bit protocol depends on the resolution of rotations. This must then be parameterized on the GE2003N.

Addresses 1H, 5H, and 9H, which are used to reset counters A and B of each channel during incremental encoder operation, have a double function.

In addition to resetting the counter regardless of the data written, the four least significant data bits are used to parameterize the zero crossing monitor.

| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | x | x | x | x | x | x | NÜ3 | NÜ2 | NÜ1 | NÜ0 |

**NÜ3 to NÜ0** These bits specify the most significant bit for monitoring of zero crossing.

| | |
|---|---|
| "0000", "0001" | Zero crossing monitor disabled |
| "0010", "0011" | 12/11 |
| "0100" | 13/12 |
| "0101" | 14/13 |
| "0110" | 15/14 |
| "0111" | 16/15 |
| "1000" | 17/16 |
| "1001" | 18/17 |
| "1010" | 19/18 |
| "1011" | 20/19 |
| "1100" | 21/20 |
| "1101" | 22/21 |
| "1110" | 23/22 |
| "1111" | 24/23 |

Following a reset, the four data bits (NÜ3 to NÜ0) are equal to "0000". This disables the zero crossing monitor.

Parameterizing the data bits for the zero crossing monitor while SSI mode is already activated prevents the shift counter from being reset.

After parameterization of the zero crossing monitor, a check for zero crossing is first performed on the actual value of the third successful SSI transmission. SSI encoders must meet the following requirements for the zero crossing monitor.

- Resolution of at least four steps
- At least one scanning value of the SSI cycle during a rotation must be located in the 1st and 4th quarters even when the axis is operating at maximum speed.
- Capped code must contain encoder values with most significant bits = "00" and "11". The above requirement is particularly important for these value ranges in regard to the SSI cycle at maximum speed.

When an SSI value has been transferred with start/stop bit errors, this value is not used to monitor zero crossing.

### 6.1.12 Toggling the Comparison Bit During Zero Crossing of the SSI Encoder

When a comparison is activated (i.e., after comparison register B has been loaded), the comparison condition is toggled each time the zero point is crossed (i.e., if the comparison condition was >=, it becomes <= after the zero point is crossed, and vice versa). The new comparison condition is already valid for the actual value with which the zero crossing was detected. This provides solutions to the following application problems.

## Application problem 1:

The total number of encoder steps of an absolute value encoder is to be 32 (counting range from 0 to 31). A comparison value of 3 with comparison condition >= is to be parameterized. The direction of rotation is forward. The last SSI transmission resulted in an actual value of 28, and additional actual values are expected to arrive before zero is crossed. Therefore, the comparison value 3 with the comparison condition >= cannot be loaded immediately since the comparison would be fulfilled immediately by the actual values arriving before the zero point (29 to 31).

For problem 1, the toggle function means that the comparison value with the comparison condition <= is loaded although a comparison for >= is actually desired. The next zero crossing corrects this, however. The <= condition is not fulfilled before zero crossing. After zero crossing the comparison condition >= is correct, and the comparison is fulfilled as desired after the comparison value is crossed in the forward direction.

## Application problem 2:

Just after zero crossing, the axis is located at actual position 3. The new comparison value 6 (forward direction and comparison condition >=) has already been loaded. After the axis has started and the brakes are enabled, the load pulls the axis backward over the zero point. Actual positions on the other side of the zero point (i.e., 31 or less) are achieved which fulfill the comparison and thus activate the comparison interrupt/comparator pin which is not desired.

In problem 2, the comparison condition is toggled from >= to <= when the zero point is crossed backwards. The comparison is thus not fulfilled. After the drive has equalized the pull of the load (which causes the zero point to be crossed again), this toggles the comparison condition to >= again. The comparison is then performed correctly.

## Application problem 3 (scanning gap):

The total number of encoder steps of an absolute value encoder is to be 32 (counting range from 0 to 31). A comparison value of 30 is to be parameterized with a comparison condition of >=. The direction of rotation is forward. An SSI transmission results in the actual value 28. The next transmission results in a value of 1. Due to the pause between two transmissions, the actual values 29 to 31 and 0 are not acquired. Although the comparison value was crossed, no comparison interrupt is triggered since the pure comparison for >= was not fulfilled by the two actual values.

By toggling the comparison condition from >= to <= when zero is crossed, a comparison for <= comparison value 30 is performed with actual value 1. This condition is fulfilled, and the problem of scanning gaps is remedied.

Since the parameterization sequence (loading of comparison register A, command register and comparison register B) requires time, a zero crossing can already occur during this sequence. The next zero crossing would then be one rotation later, and the comparison condition would not be toggled until then (i.e., too late).

For this reason, the register is given an additional VLN data bit (load comparison value when close to zero crossing) for parameterization of the zero crossing monitor. This bit is used to indicate that a zero crossing is probable during the parameterization sequence of the comparison.

The effect of zero crossing (i.e., toggling the comparison condition) is performed on the GE2003N with the VLN bit set if the following is true when comparison register B is loaded.

- The current comparison condition is <=, and the two most significant bits of the actual value are "00" (actual value in 1st quarter).
- The current comparison condition is >=, and the two most significant bits of the actual value are "11" (actual value in 4th quarter).

In both cases it is assumed that zero crossing occurred during the parameterization sequence and toggling during this zero crossing was desired.

Parameterization must be performed in the following order.

- Load low portion of the comparison value in comparison register A to simultaneously deactivate the last comparison and the toggling of the comparison condition when zero crossing occurs.
- Set comparison condition (>= or <=) in command register.
- Set/reset the VLN bit.
- Load high portion of the comparison value in comparison register B.

Both comparison and the capability of toggling the comparison condition during zero crossing are active. The time sequence of the evaluation at the end of an SSI transmission is designed so that zero crossing detection takes place first, followed by the scanning of the comparison result. This ensures that the SSI transmission, with which the zero crossing is detected and via which the comparison condition is toggled, is used for the comparison with the new comparison condition.

Register for parameterization of the zero crossing monitor:

| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | x | x | x | x | x | VLN | NÜ3 | NÜ2 | NÜ1 | NÜ0 |

Following a reset, the four data bits (NÜ3 to NÜ0) are equal to "0000". This disables the zero crossing monitor. Bit VLN also equals "0".

**Note:**
The new functions (i.e., zero crossing monitor and toggling the comparison bit) have no effect if one of the following is true.

- The zero crossing monitor is not activated (i.e., D4 to D0 are written with "00000" or "00001" when writing the addresses for resetting the counters).

Or:

- The zero crossing monitor is activated but the channel is only used for incremental encoder operation.

Or:

- The zero crossing monitor is activated and the channel is used for SSI operation but:

  * The new, previously unused status bits are ignored.

  * The corresponding interrupt masks are set.

  * The comparators are not used.

## 6.2 Generating Interrupts

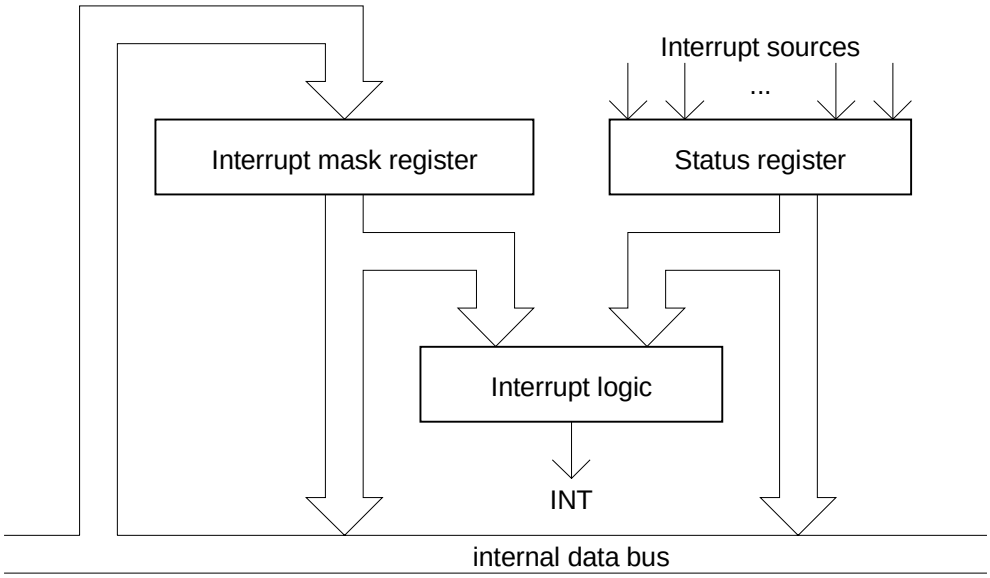



Figure 6.1 Diagram of the interrupt unit

Certain events on the GE2003N generate a group interrupt (INT). Each of these events can be masked (by appropriate loading of the interrupt mask register) and can also be read out via the status register. Reading this register resets all active interrupts and status bits. The status bit "shift procedure running on DA interface" is an exception. This status bit is not reset by reading the status register. Instead, it is reset after the shift procedure on the DA interface has been concluded.

The interval between two active interrupt requests is at least one clock pulse period in length. An active interrupt request lasts the same minimum time.

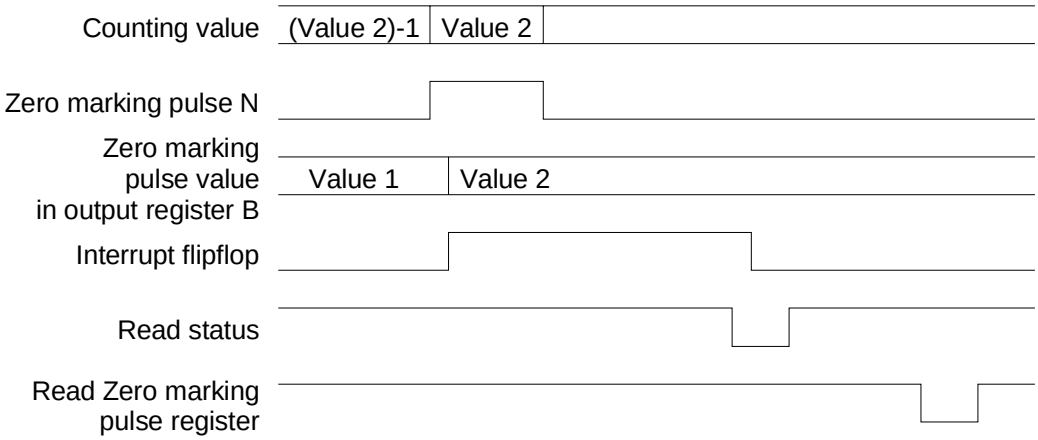
After a hardware reset, all interrupts are masked.

### 6.2.1 Zero Marking Pulse Interrupt

When a parameterized edge of the N zero marking pulse signal is detected during operating mode **counting with direction discriminator** or **counting without direction discriminator**, the current counter status is latched in the zero marking pulse register (output register B) and an interrupt is generated. The value is retained in output register B until the next parameterized edge of the zero marking pulse signal. The interrupt request (INT) is withdrawn when the status register is read. If a new parameterized edge of the zero marking pulse signal arrives before the interrupt is reset, the new value is latched. The second interrupt is lost, however. If a parameterized edge of the zero marking pulse signal arrives while the zero marking pulse register is being read, the new counter value cannot be latched since it would be "mixed" with the old counter value when read. If the interrupt bit was already reset, it is set again.

## Normal case

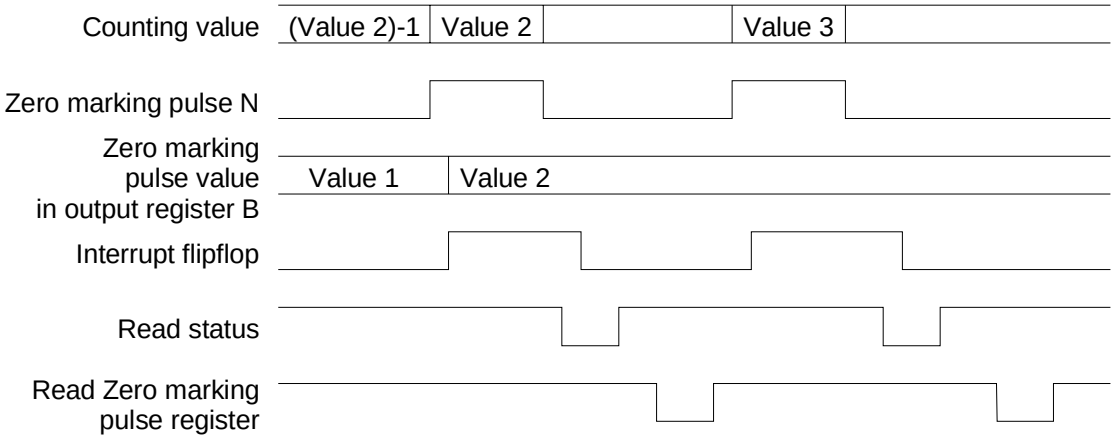
Assumption: Rising edge of N is parameterized.




The interrupt is withdrawn with the falling edge of read INT status, but the status bits are still retained until the rising edge of read INT status.

## Special case

Assumption: Rising edge is parameterized.




In this special case it is evident that, although a second interrupt is requested, the new zero marking pulse value (value 3) cannot be latched. Value 3 in our example is lost. This only occurs when the reaction to the interrupt continues until a new zero marking pulse arrives (i.e., one rotation of the encoder).

### 6.2.2 Comparator Interrupt

During the four modes **counting with/without direction discriminator** and **screwing with/without direction discriminator**, the 16 bits of comparison register A are continuously compared with counter value A.

If equal, an interrupt is generated. The interrupt is withdrawn by reading the status register. A new interrupt cannot be generated until a new comparison value has been written in comparison register A.

When SSI is involved, the bits (13, 21 or 25) of comparison registers A and B are compared with the bits of the SSI shift register.

The condition which will cause the interrupt can be selected.

- Actual value >= comparison value
- Actual value <= comparison value

In this case also, a new interrupt cannot be generated until a new comparison value has been loaded in comparison registers A **and** B.

### 6.2.3 Error Interrupts

The following errors can cause interrupts.

**During shifting**

Start/stop bit error
Start bit not equal to 1 or stop bit not equal to 0 (for observer mode: only start bit not equal to 1)

**During counting/screwing**

- Edge error between track UA and UB
  When the edges of UA and UB follow each other too quickly (i.e., within one clock pulse cycle), an edge error is reported.
- Direction discriminator: Direction error
  There are three states. Traversing forward, traversing backward and standstill. If the direction monitor is activated on the GE2003N and the direction to be monitored is parameterized, any deviation (i.e., counting impulse for the other direction) is reported as an error interrupt. This monitor must be disabled during standstill. See command register.

### 6.2.4 Status Register

Depending on the primary operating mode set (**counting/screwing** or **shifting**), the status bits have different meanings.

| **Status bit** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** |
|---|---|---|---|---|---|---|---|---|
| Counting/screwing | VS1 | VS0 | X | AÜ | VG3 | VG2 | VG1 | NM3 |
| Shifting | VS1 | VS0 | X | AÜ | VG3 | VG2 | VG1 | NW3 |
| **Status bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Counting/screwing | NM2 | NM1 | RF3 | RF2 | RF1 | FF3 | FF2 | FF1 |
| Shifting | NW2 | NW1 | ND3 | ND2 | ND1 | SS3 | SS2 | SS1 |

The digit in the status bit designations specifies the channel number to which the status bit refers.

## Meaning of the status bits:

FF: Edge error
FF = 1: Edge error detected

RF: Direction error
RF = 1: Direction error detected

NM: Zero marking pulse
NM = 1: New parameterized zero marking pulse edge detected

SS: Start/stop bit error while shifting
SS = 1: Start or stop bit error occurred

ND: Zero crossing while shifting
ND = 1: Zero crossing was detected.

NW: New SSI value
NW = 1: New SSI value latched in output register A and B

VG: Comparison result
VG = 1: Comparison value was reached.

AÜ: Analog value transmission
AÜ = 1: Analog value transmission running on DA unit

VS1, VS0: Version no. GE2003N: "01"

X: Not used. "1" is read.

### 6.2.5 Interrupt Mask Register

Interrupts can be enabled by writing in the interrupt mask register.

The meaning of the interrupt mask bits depends on the primary operating mode set (i.e., **shifting** and **counting/screwing**). Interrupt mask bits 14 and 15 are an exception. These bits are used for setting the test modes for device testing, and not for interrupt masking. These two bits are set to 1 when the device is reset and may only be changed during the device test.

| **Interrupt mask bit** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** |
|---|---|---|---|---|---|---|---|---|
| Counting/screwing | TM1 | TM0 | X | X | MVG3 | MVG2 | MVG1 | MNM3 |
| Shifting | (="1") | (="1") | X | X | MVG3 | MVG2 | MVG1 | MNW3 |
| **Interrupt mask bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Counting/screwing | MNM2 | MNM1 | MRF3 | MRF2 | MRF1 | MFF3 | MFF2 | MFF1 |
| Shifting | MNW2 | MNW1 | MND3 | MND2 | MND1 | MSS3 | MSS2 | MSS1 |

The digit in the interrupt mask bit designation specifies the channel number to which the interrupt mask bit refers. Exception: TM1 and TM0.

#### Meaning of the interrupt mask bits:

MFF: Interrupt mask, edge error (counting/screwing)

MRF: Interrupt mask, direction error (counting/screwing)

MNM: Interrupt mask, zero marking pulse signal (counting/screwing)

MSS: Interrupt mask, start/stop bit error (SSI)

MND: Interrupt mask, zero crossing (SSI)

MNW: Interrupt mask, new value (SSI)

MVG: Interrupt mask, comparator (SSI and counting/screwing)

TM0, TM1: Test mode

X: Not used

The interrupts are masked when the appropriate interrupt mask bit is set.

#### Test mode

Test modes are only set for the device check.

TM1 = 0: Internal counters which are cascaded during normal operation are switched in parallel.

TM0 = 0: Test of the input pins

# 7 Sample Programs

The board is parameterized and processed with simple I/O commands. The following examples illustrate this fact.

## 7.1 Incremental Encoders

```
/* Base address (0x400) */
/* Set mode for counter channel 1 (command register 1)*/

      outport(0x400, 0x0000);

/* Read counter status (output register A, channel 1) to "count" variable
   and output on monitor screen*/

      count = inport(0x400);
      printf("Positioning board SMP16-SFT260\n\n");
      printf("Counter value A:           %4d\n",count);
```

## 7.2 SSI Encoders

```
/* Evaluate an SSI encoder with 21 bits
   indication in revolutions and impulses/revolttion*/

      int main(void)
      {
      unsigned int ivalue1l, ivalue1h, irotation, ipulse;

/* Setting of command register, channel 3 of the SFT260
   Setting of SFT260 in continuous mode with 21 bits
   Boundary between revolutions and number of impulses/rev. at 9/10 bits
   Transmission errors are not evaluated

      outport(0x420,0x0b69);

      while(!kbhit())
            {
            irotation=0;
            ipulse=0;

/* Read value from GE2003 (output registers A and B, channel 3*/
            ivalue1l = inport(0x420);
            ivalue1h = inport(0x422);

            ivalue1l=ivalue1l >> 2;
            ipulse=ivalue1l & 0x03ff;

            irotation=ivalue1l >> 10;
            irotation=irotation & 0x000f;
            ivalue1h=ivalue1h << 4;
            irotation=irotation | ivalue1h;
            irotation=irotation & 0x01ff;
```

```
/* Output of revolutions and impulses on the monitor screen */

            printf("Positioning board SMP16-SFT260\n\n");
            printf("Number of rotations:           %4d\n",irotation);
            printf("Number of pulses:              %4d\n",ipulse);
            gotoxy (0,0);
            }
            return 0;
      };
```

## 7.3 Evaluation of Wire Break

```
/* Base address (0x400) */

/* Read EPLD register 1 and write in variable*/

      Wire break = inport(0x416);

/* Reset wire break of all channels in EPLD register 1*/

      outport(0x416, 0x00cc);
```