SMP212

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 10 W from rectified 220 VAC input, 5 W from rectified universal (85 to 265 VAC) input
- External transformer provides isolated output voltages
- Integrated solution minimizes overall size

High-voltage, Low-capacitance MOSFET Output
- Designed for 120/220 V off-line applications
- Can also be used with DC inputs from 36 V to 400 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- Wide V_{BIAS} voltage range
- Designed for use with optocoupler feedback

Built-In Self-protection Circuits
- Adjustable cycle-by-cycle current limit
- Latching shutdown can be used for output overvoltage protection
- Shutdown/auto-restart cycling
- Input undervoltage lockout
- Thermal shutdown

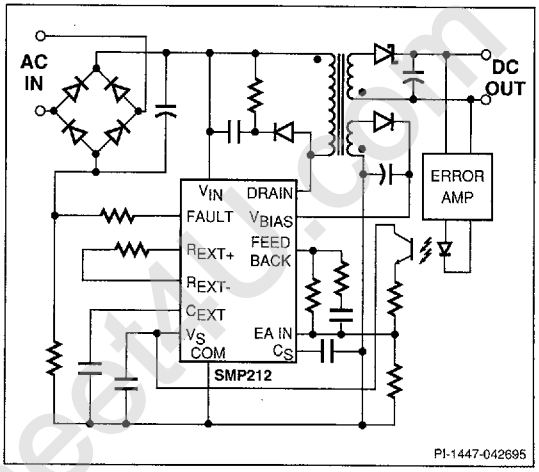

Figure 1. Typical Application

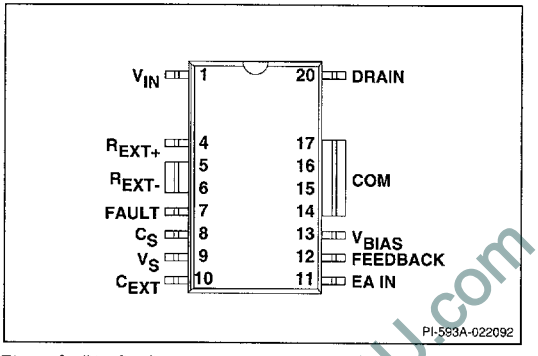

Figure 2. Pin Configuration

Description

The SMP212, intended for 220 V or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a small, low-cost, isolated, off-line power supply.

The high-speed power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low threshold voltage. Low capacitance and low threshold voltage reduce gate drive and bias power, allowing higher frequency operation.

The controller section of the SMP212 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, error amplifier, gate driver, and circuit protection. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies, but may be used with other topologies as well.

The SMP212 is available in a 20-pin batwing SOIC package.

ORDERING INFORMATION		
PART NUMBER	PACKAGE OUTLINE	T_j RANGE
SMP212SRI	S20B	-40 to 125°C

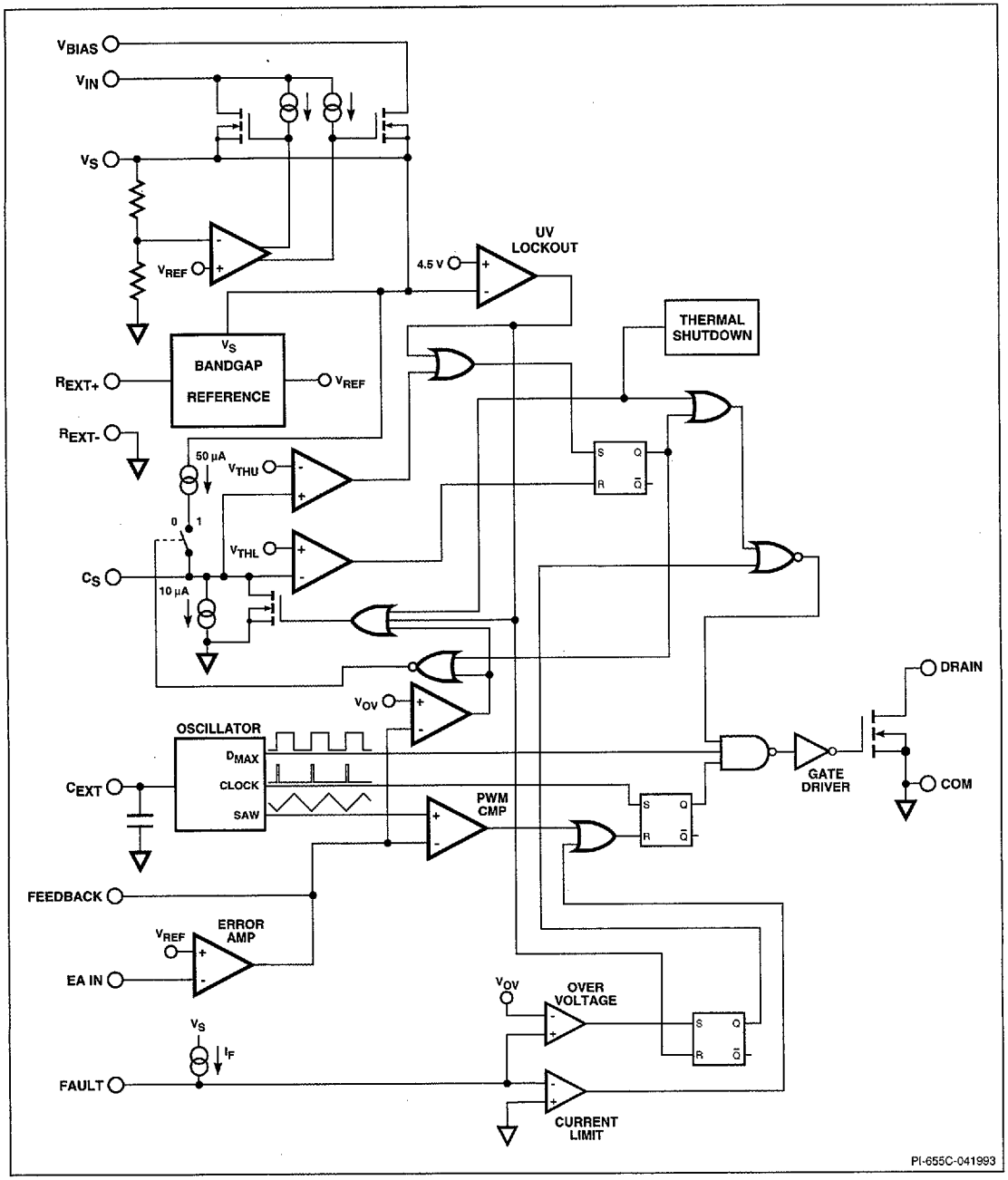

Figure 3. Functional Block Diagram of the SMP212.

Pin Functional Description

Pin 1:
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 4:
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 5, 6:
R_{EXT-} is the return for the reference current.

Pin 7:
The **FAULT** pin is used with an external resistor to provide protection of the output during overcurrent and overvoltage conditions.

Pin 8:
C_S is used to set the shutdown/auto-restart cycle time.

Pin 9:
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 10:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 11:
EA IN is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 12:
FEEDBACK is the error amplifier output for connection to the external compensation network.

Pin 13:
V_{BIAS} is the bootstrap voltage used to self-power the device once the supply is operating.

Pin 14, 15, 16, 17:
COM connections. Ground or reference point for the circuit.

Pin 20:
Open **DRAIN** of the output MOSFET.

SMP212 Functional Description

Bias Regulator
The onboard supply voltage (V_S) is supplied from either of two high-voltage linear regulators. The V_{IN} linear regulator draws current from the high-voltage bus while the V_{BIAS} regulator draws current from a voltage generated from a transformer winding. The V_{IN} regulator dissipates significant power levels and should be cut off during normal operation for improved efficiency. The V_S error amplifier has a built-in preference for generating V_S from the V_{BIAS} regulator, which automatically cuts off the V_{IN} regulator during normal operation. During start-up and under power supply fault conditions, the bias error amplifier generates V_S from the V_{IN} regulator.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and noise immunity. The value of V_S also determines when the internal undervoltage lockout is enabled. Undervoltage lockout disables the power MOSFET until V_S is within its normal operating range.

Bandgap Reference
V_{REF} is a 1.25 V reference voltage generated by the temperature compensated bandgap reference. This reference voltage is used for setting thresholds for comparators, amplifiers, and the thermal shutdown circuit. The external resistor connected between R_{EXT+} and R_{EXT-} and the bandgap reference set the proper internal bias current levels for the various internal circuits.

Oscillator
The oscillator linearly charges and discharges the combined internal and external capacitance between two different voltage levels to create a sawtooth waveform for the pulse width modulator. Two digital signals, D_{MAX} and CLOCK are also generated. D_{MAX} corresponds to the rising portion of the sawtooth waveform, and is used to gate the MOSFET driver. A short CLOCK pulse is used to reset the pulse width modulator and current limit latch at the beginning of each cycle.

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop by driving the power MOSFET with a duty cycle proportional to the voltage on the FEEDBACK pin as shown in Figure 4. The duty cycle signal is generated by a comparator which compares the FEEDBACK voltage with the sawtooth waveform generated on the C_{EXT} pin. As the input voltage increases the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the power MOSFET. The pulse width modulator resets the latch, turning off the power MOSFET. The D_{MAX} signal from the oscillator limits the maximum duty cycle by gating the output driver.

SMP212 Functional Description (cont.)

Fault Protection
The FAULT pin is used to implement both cycle-by-cycle MOSFET transistor current limiting and latching output shutdown protection.

The FAULT pin turns off the power MOSFET switch when an overcurrent condition causes the voltage on this pin to drop below the FAULT current limit threshold. The DRAIN current is converted to a voltage by an external sense resistor. An internal current source applied to an external offset resistor biases the FAULT signal to a positive voltage when no DRAIN current is flowing. During an overcurrent condition, current flowing in the sense resistor will cause the FAULT voltage to decrease. When the FAULT voltage falls below the fault current limit threshold for a time period exceeding the current limit delay, the power switch will be latched off until the beginning of the next clock cycle as shown in Figure 4. If this condition persists over many switching cycles, the output voltage will fall out of regulation, the output of the error amplifier (FEEDBACK) will saturate in a high state, and the external C_s autorestart capacitor capacitor will begin to charge.

For latching output overvoltage protection, an external optocoupler can be used to drive the FAULT pin above the FAULT OV threshold as shown in Figure 5. A latch is set that turns off the power MOSFET switch. Cycling the undervoltage lockout circuit by removing and restoring input power is necessary to reset the latch and resume normal power supply operation.

Shutdown/Autorestart
The shutdown/autorestart feature turns the power supply on and off at a duty cycle of 20% if an overcurrent fault condition persists. An overcurrent fault condition causes the output voltage to fall out of regulation, which then causes the internal error amplifier output to saturate at maximum output voltage. The saturated high output voltage is detected by a comparator which switches a charging current source on to the C_s pin. The 50 µA switched-charging current source is greater than the 10 µA fixed-discharging current source which creates a net C_s capacitor charge current of 40 µA. The net current charges the external C_s capacitor while the power supply is still operating into the excessive load condition. When the upper threshold is reached, the power supply is turned off, the charging current source is switched off, causing the discharging current source to slowly discharge the C_s capacitor. When the lower threshold is reached, the power suppy is turned back on, and the cycle begins again as shown in Figure 5. When the excessive load condition is removed, the output voltage becomes regulated again, the error amplifier output voltage is reduced back into the linear range (1.2 to 2.4 V), and the C_s capacitor is quickly reset to zero volts by an internal MOSFET switch.

The thermal shutdown and UV lockout circuits also reset the C_s capacitor prior to turn-on so that the power supply will always start from a known state regardless of the fault or operating condition.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off and reduces supply current when the switch junction gets too hot (typically 140°C). When the circuit has cooled past the hysterisis temperature, normal operation resumes.

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General Circuit Operation

The flyback power supply circuit shown in Figure 6 is a dual 5/12 V, 5 W power supply that operates from 85 to 265 V(rms) AC input voltage. The 5 V output voltage is directly sensed and accurately regulated by a secondary-referenced error amplifier. The error amplifier drives an error signal through an optocoupler to the SMP212 which directly controls the duty cycle of the integrated high voltage MOSFET switch. The effective output voltage can be fine-tuned by adjusting the resistor divider formed by R18 and R29. Other output voltages are possible by adjusting the transformer turns ratios as well as the resistor divider.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of transformer T1. The other side of the transformer primary is driven by the integrated high voltage MOSFET transistor within the SMP212. The clamp circuit implemented by R10, C9, and D5 clamps the leading-edge voltage spike caused by transformer leakage inductance to a safe value. Ringing caused by parasitic capacitance and leakage inductance is damped by C15 and R9. The 5 V power secondary winding is rectified and filtered by D2, C2, C14, and L5 to create the 5 V output voltage. The effective 12 V winding is created by stacking a 7 V winding on top of the 5 V winding. D6, C24, C26, and L6 perform rectification and filtering for the 12 V output voltage. R31 and C27 damp the secondary leakage inductance ringing voltage caused by the stored charge in diode D6. R22 provides a slight pre-load on the 12 V output to improve load regulation at light loads. The bias winding is rectified and filtered by D3 and C5 to create a bias voltage to the SMP212, which effectively

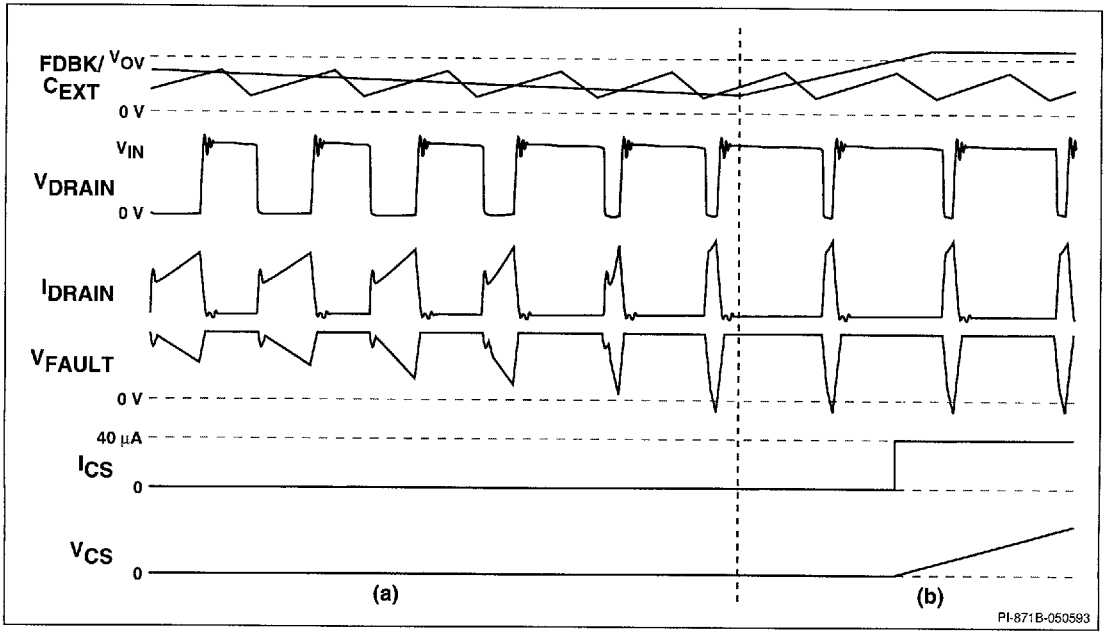

Figure 4. Typical Waveforms for (a) Normal Operation, and (b) Overcurrent Shutdown.

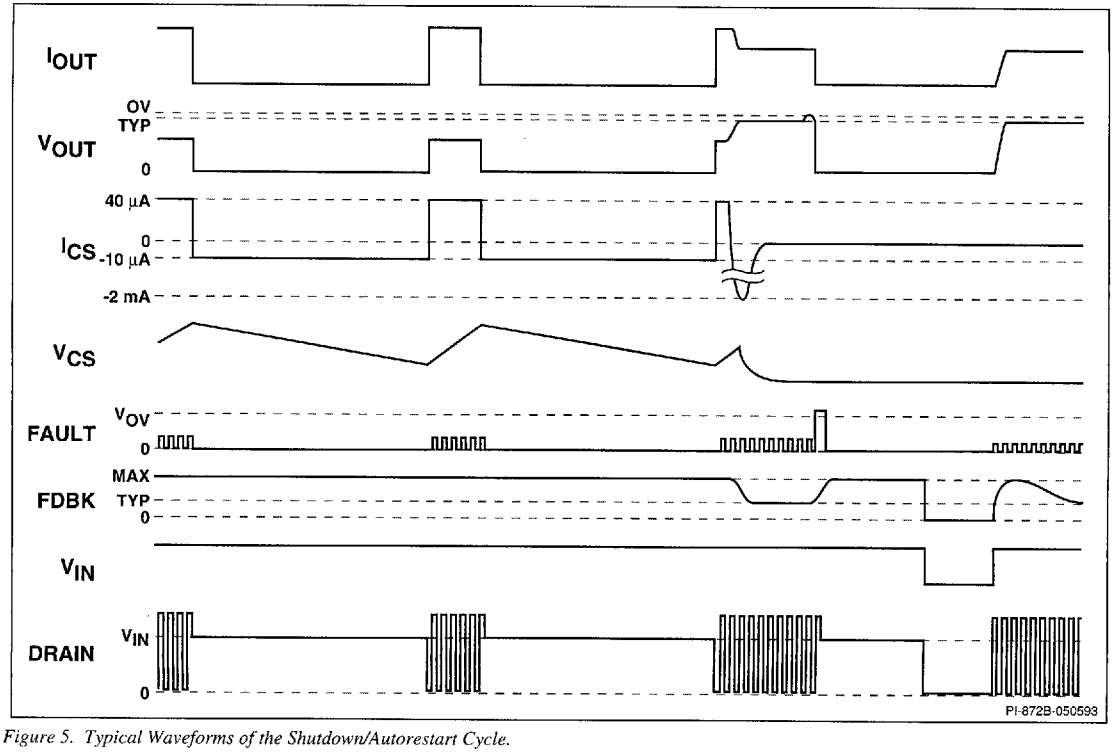

Figure 5. Typical Waveforms of the Shutdown/Autorestart Cycle.

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5 W Universal Off-line Power Supply with Optocoupler Feedback

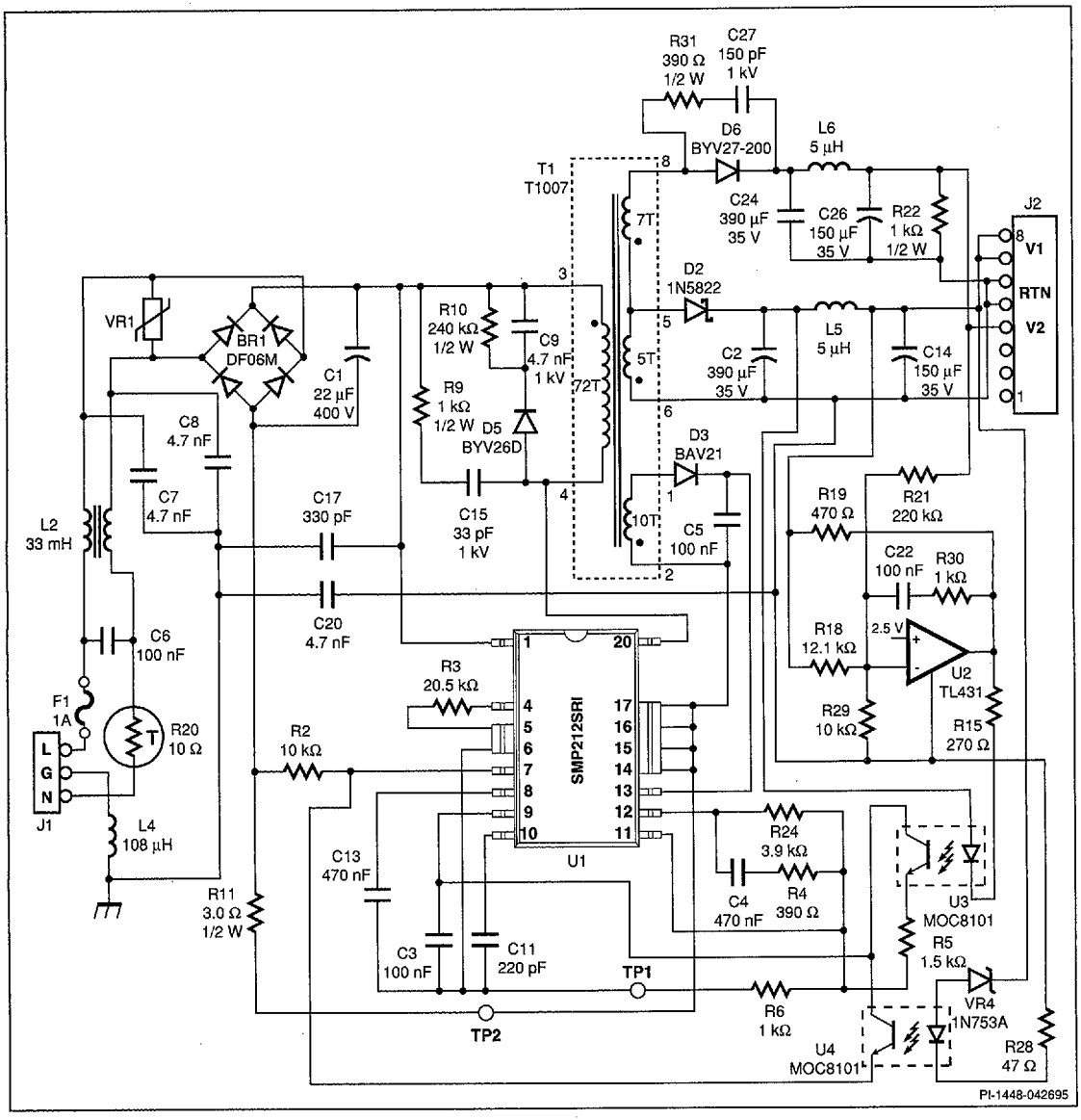


Figure 6. Schematic Diagram of a dual output 5 W Universal Input Power Supply Utilizing the SMP212.

General Circuit Operation (cont.)

cuts off the high-voltage internal linear regulator.

Common-mode emission currents which flow between the primary windings of the transformer and the secondary output circuitry are attenuated by C7, C8, C17, C20, L2, and L4. Differential-mode emission currents caused by pulsating currents at the input of the power supply are attenuated by C6 and L2. Voltage spikes on the line are clamped by VR1. Thermistor R20 limits initial surge currents at turn on to a safe value.

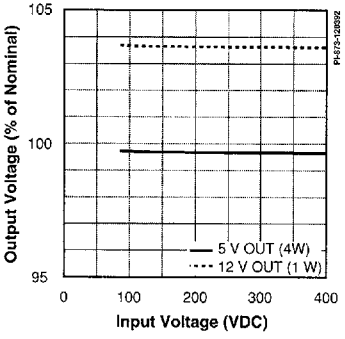
Internal bias currents are accurately set by R3. Bypass capacitor C3 filters current spikes on the internally generated voltage source V_S. The oscillator frequency is determined by C11. Transistor switch current is sensed by R11. The offset voltage level at the FAULT pin is determined by R2 and the internal FAULT current source. C13 determines the auto-restart time interval.

The secondary-referenced error amplifier is implemented with a TL431 shunt regulator (U2). This device consists of an accurate 2.5 V bandgap reference , error amplifier, and driver. The output voltage is sensed, divided by R18 and R29, and applied to the inverting input of the error amplifier. R21 provides limited sensing of the 12 V output to improve cross regulation. The non-inverting input of the error amplifier is internally connected to the bandgap reference voltage. The frequency response of the error amplifier is determined by the compensation network consisting of R30, C22, and the high frequency gain setting resistor R18. Bias current of 2 mA for U2 is provided by R19. The LED current in optocoupler U3 is limited by R15. The collector of the optocoupler output transistor is connected to V_S of the SMP212. R5 and the effective capacitance of the optocoupler filter high-frequency switching noise. R6 sets the DC bias current through the optocoupler to a maximum value of 1.25 mA. During normal operation, the voltage across R6 is constant and equal to the internal bandgap reference voltage. R24 determines the DC and low frequency AC gain of the SMP212 error amplifier and optocoupler circuit. C4 and R4 provide additional compensation for the control loop as well as additional noise filtering.

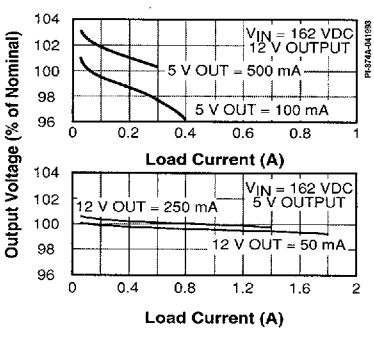
The overload shutdown/automatic restart

Typical Performance Characteristics (Figure 6 Power Supply)

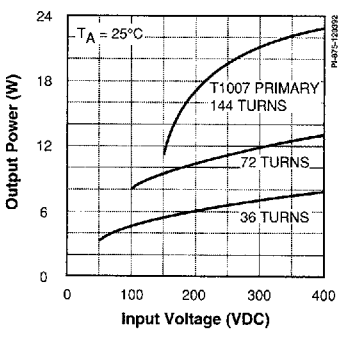
LINE REGULATION



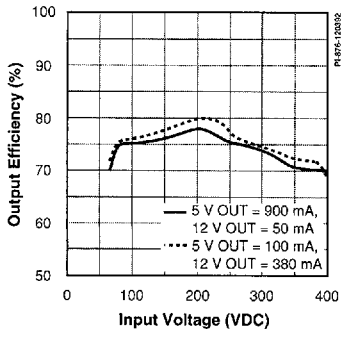
LOAD REGULATION



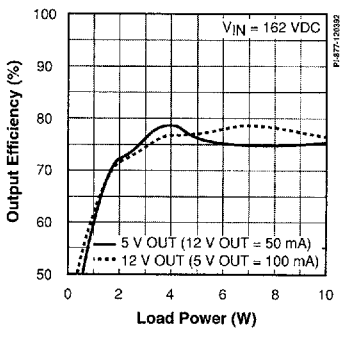
MAXIMUM OUTPUT POWER



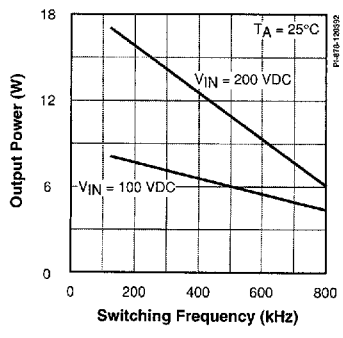
EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



OUTPUT POWER vs. FREQUENCY



General Circuit Operation (cont.)

timing function is activated when ever the output voltage is out of regulation. C_S and current sources internal to the IC set the time delays. The C_S capacitor is normally held low. C_S is charged toward the shutdown threshold whenever the output of the internal error amplifier is saturated in the maximum duty cycle state. The internal error amplifier is saturated whenever the circuit is in current limit, which occurs at turn-on and overload conditions

During an overload, the auto-restart feature turns the power supply on and off at a typical duty cycle of 20% to reduce the effective power delivered to the output rectifier.

Optocoupler U4 drives the FAULT pin high and latches the power supply off if an output overvoltage condition exists. Optocoupler U4 will turn on if the output overvoltage exceeds the specified voltage of Zener diode VR4. R28 limits photodiode current to a safe value.

To reduce device power dissipation and temperature rise during normal operation, the voltage applied to V_{BIAS} must be greater than the minimum specified value to ensure complete cutoff of the high-voltage linear regulator. Ensure that the maximum specified voltage on the V_{BIAS} pin is not exceeded when adjusting the value of the output voltage.

The peak current limit circuit will turn off the MOSFET switch when the voltage across R11 is approximately equal to the voltage across R2.

Performance data is shown on the previous page for the circuit given in Figure 6.

The line and load regulation graphs were measured when operated from a DC source. The switching frequency of the power supply was measured at 125 kHz.

The maximum output power curve shows the power output capability for the normal transformer, and the performance with twice and half the normal number of primary turns.

The output power versus frequency curve was generated by characterization of the SMP212 at various frequencies. Several different power transformers, optimized for each frequency, were used to generate the maximum power at each point. The curves illustrate the trade-off between AC and DC power losses within the device. As AC losses rise with frequency, DC losses and output power must be reduced to maintain the same device maximum power dissipation.

ABSOLUTE MAXIMUM RATINGS[1]

Drain Voltage	800 V
V_{IN} Voltage	500 V
V_{BIAS} Voltage	35 V
Drain Current[2]	800 mA
Input Voltage[3]	- 0.3 V to V_S + 0.3 V
Storage Temperature	–65 to 125°C
Operating Junction Temperature[4]	-40 to 150°C
Lead Temperature[5]	260°C
Power Dissipation (T_A = 25°C)	3.33 W
(T_A = 70°C)	1.83 W
Thermal Impedance (θ_{JA})	30°C/W
Thermal Impedance (θ_{JC})[6]	6°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 300 µs, 2% duty cycle.
3. Does not apply to V_{IN} or DRAIN.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Measured at pin 15/16.

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V R_{EXT}=20.5 kΩ, C_S=560 nF, C_{EXT}=100 pF T_j = -40 to 125°C (See Note 1)	Min	Typ	Max	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = Open		900		kHz
			193	233	272	
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	C_{EXT} = Open		0-40		%
			0-48	0-52		
CIRCUIT PROTECTION						
FAULT Offset Current	I_F		-103	-93	-83	µA
FAULT OV Threshold	V_{OV}		3.5	V_S-1.6 V	4.9	V
FAULT Current Limit Threshold	V_{ILIMIT}		-100		0	mV
Current Limit Delay Time	$t_{d(off)}$	See Figure 7	75	150	250	ns
Thermal Shutdown Temperature			125	140		°C
Thermal Shutdown Hysteresis				15		°C

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V R_{EXT}=20.5 kΩ, C_S=560 nF, C_{EXT}=100 pF T_j = -40 to 125°C (See Note 1)		Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART							
ON Time	t_{ON}	See Figure 8		24	42	61	ms
Reset Impedance	Z_{RESET}	C_S = 4 V			2		kΩ
Duty Cycle	AR_{DC}				20	25	%
Auto-Restart Frequency					4.5		Hz
Upper Threshold Voltage	V_{THU}				4.5		V
Lower Threshold Voltage	V_{THL}				1.4		V
ERROR AMPLIFIER							
Reference Voltage	V_{REF}			1.125	1.25	1.375	V
Reference Voltage Temperature Drift	ΔV_{REF}				±300		ppm/°C
Gain-Bandwidth Product					500		kHz
DC Gain	A_{VOL}			60	80		dB
Output Current	I_{OUT}	VFB = 2.3 V			-2.5		mA
		VFB = 1.1 V			0.7		
Output Impedance	Z_{OUT}				27		Ω
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C		20	25	Ω
			T_j = 100°C		31	37	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V	T_j = 25°C	300	380		mA
			T_j = 100°C	200	260		

2

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V R_{EXT}=20.5 kΩ, C_S=560 nF, C_{EXT}=100 pF T_j = -40 to 125°C (See Note 1)	Min	Typ	Max	Units
OUTPUT (cont.)						
OFF-State Current	I_{DSS}	V_{DRAIN} = 640 V, T_A = 125°C		100	500	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 250 µA, T_A = 25°C	800			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz		45		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 400 V		700		nJ
Rise Time	t_r	See Figure 7		70	150	ns
Fall Time	t_f	See Figure 7		70	150	ns
SUPPLY						
Pre-regulator Voltage	V_{IN}		36		500	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected		3	4.5	mA
		V_{BIAS} > 8.25 V			0.1	
		Thermal Shutdown ON			2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied	8.25		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied		3	4.5	mA
V_S Source Voltage	V_S		5.1		6.4	V
V_S Source Current	I_S	V_{BIAS} > 8.25 V			5	mA

NOTES:

1. Applying >3.5 V to the C_{EXT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the SMP212 is connected to a high voltage power source when the test circuit is activated.

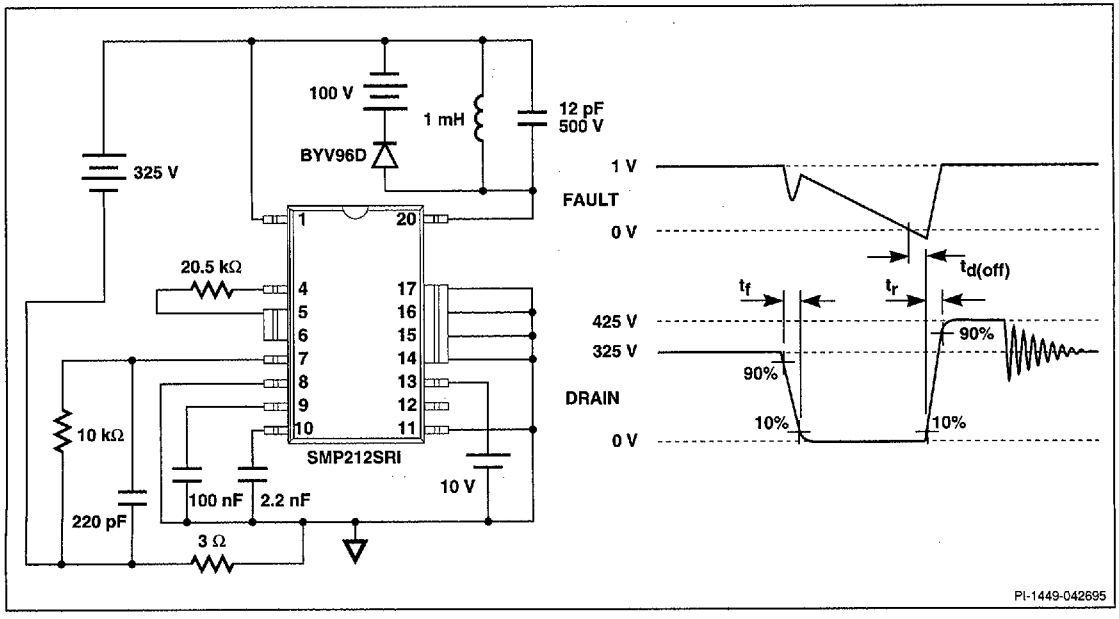


Figure 7. Current Limit Delay/Switching Time Test Circuit.

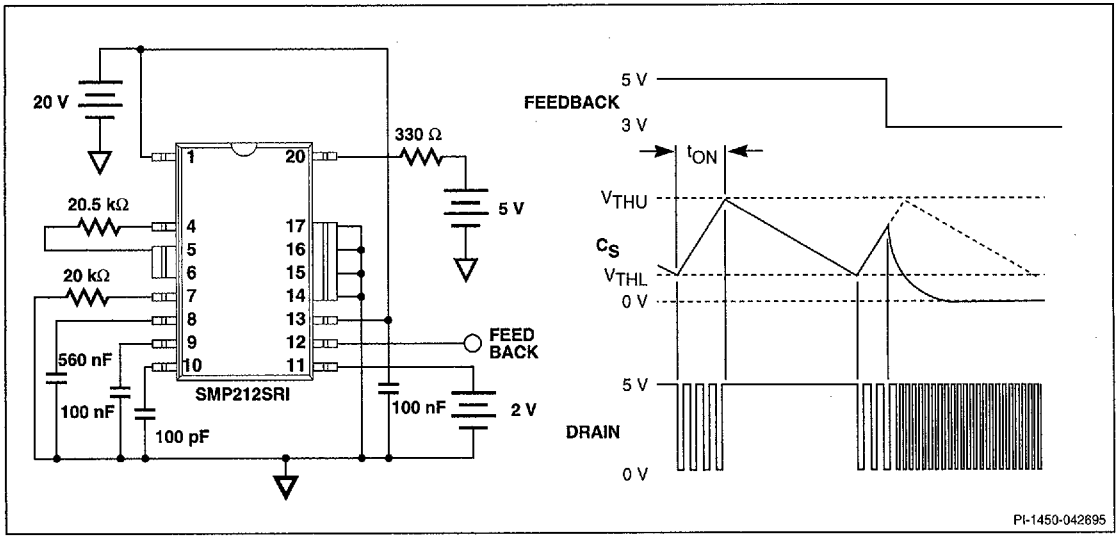
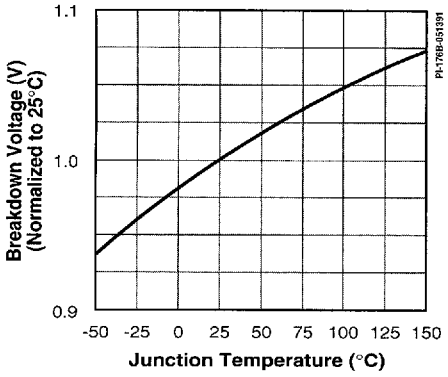
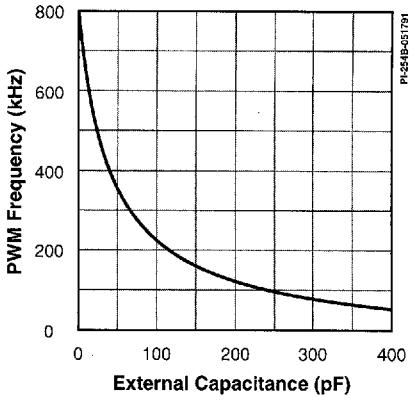


Figure 8. Auto-restart Test Circuit.

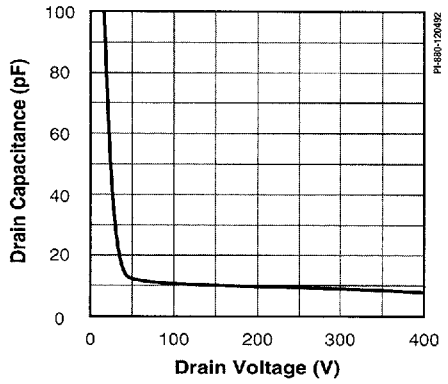
BREAKDOWN vs. TEMPERATURE



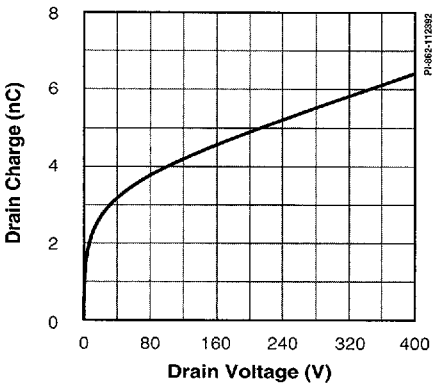
f_{PWM} vs. EXTERNAL CAPACITANCE



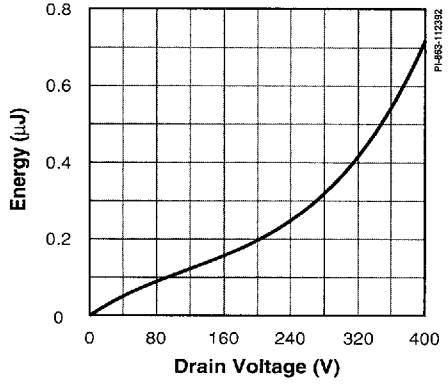
C_{OSS} vs. DRAIN VOLTAGE



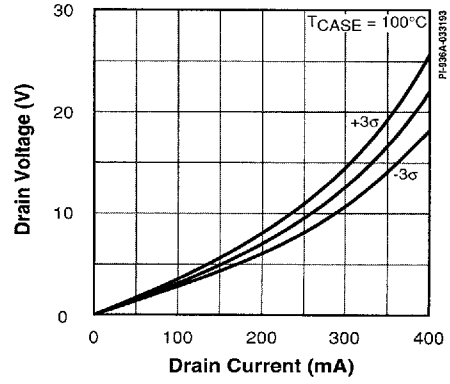
DRAIN CHARGE vs. DRAIN VOLTAGE



DRAIN CAPACITANCE ENERGY



OUTPUT CHARACTERISTICS



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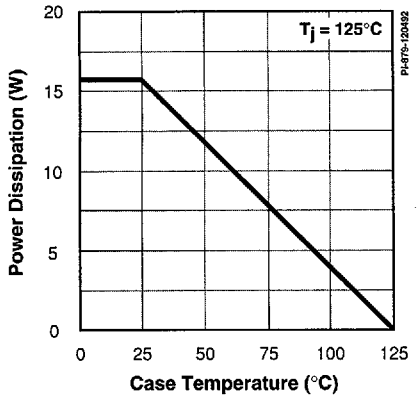
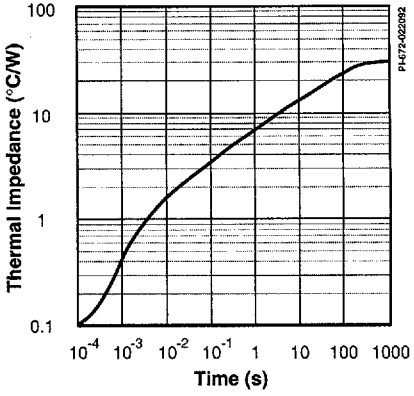
PACKAGE POWER DERATING



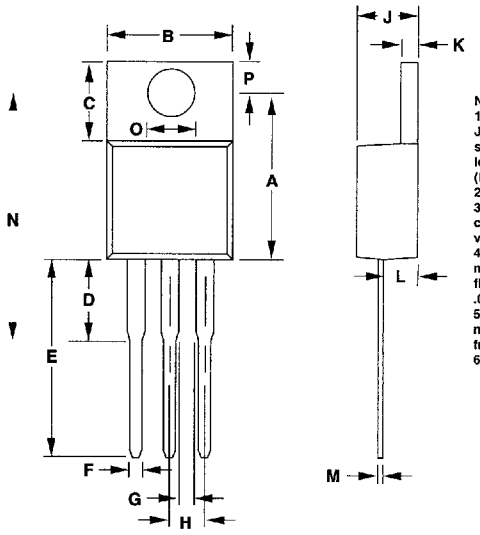
TRANSIENT THERMAL IMPEDANCE



2

Y03A — Plastic TO-220/3

DIM	inches	mm
A	.460-.480	11.68-12.19
B	.400-.415	10.16-10.54
C	.236-.260	5.99-6.60
D	.240 - REF.	6.10 - REF.
E	.520-.560	13.21-14.22
F	.028-.038	.71-.97
G	.045-.055	1.14-1.40
H	.090-.110	2.29-2.79
J	.165-.185	4.19-4.70
K	.045-.055	1.14-1.40
L	.095-.115	2.41-2.92
M	.015-.020	.38-.51
N	.705-.715	17.91-18.16
O	.146-.156	3.71-3.96
P	.103-.113	2.62-2.87

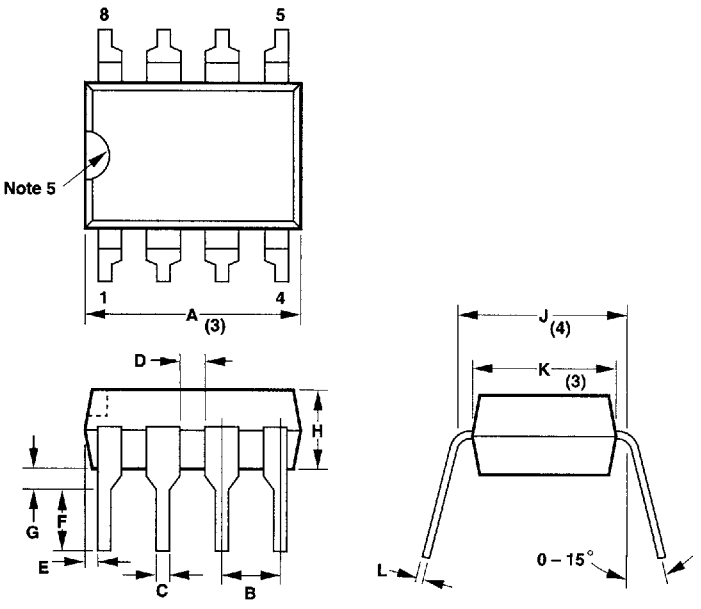


Notes:
1. Package dimensions conform to JEDEC specification TO-220 AB for standard flange mounted, peripheral lead package; .100 inch lead spacing (Plastic) 3 leads (issue J, March 1987)
2. Controlling dimensions are inches.
3. Pin numbers start with Pin 1, and continue from left to right when viewed from the top.
4. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
5. Position of terminals to be measured at a position .25 (6.35 mm) from the body.
6. All terminals are solder plated.

PI-1848-050696

P08A — Plastic DIP-8

Dim.	inches	mm
A	.395 MAX	10.03 MAX
B	.090-.110	2.29-2.79
C	.015-.021	0.38-0.53
D	.040 TYP	1.02 TYP
E	.015-.030	0.38-0.76
F	.125 MIN	3.18 MIN
G	.015 MIN	0.38 MIN
H	.125-.135	3.18-3.43
J	.300-.320	7.62-8.13
K	.245-.255	6.22-6.48
L	.009-.015	0.23-0.38



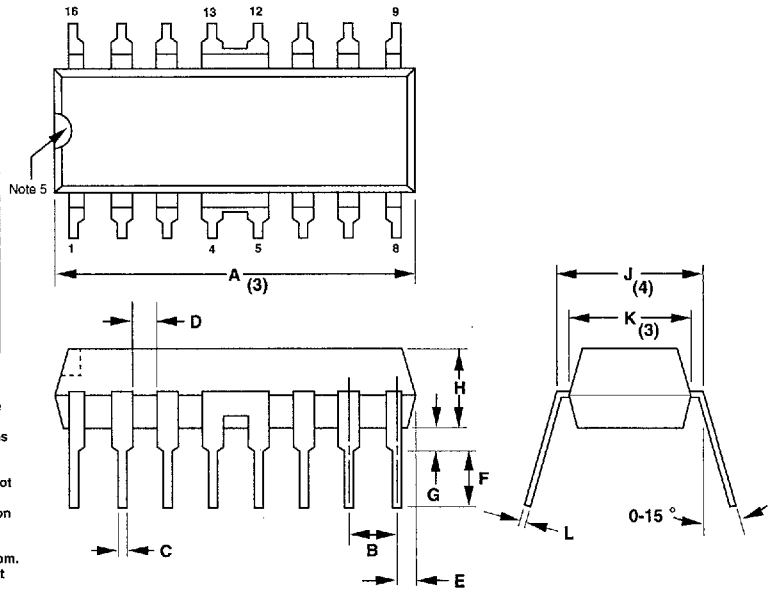
Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85).
2. Controlling dimensions: inches.
3. Dimensions are for the molded body and do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

PI-1842-050196

5

P16B — Plastic DIP-16

DIM	Inches	mm
A	.780 MAX	19.81 MAX
B	.090-.110	2.29-2.79
C	.015-.021	.38-.53
D	.040 TYP	1.02 TYP
E	.015-.030	.38-.76
F	.125 MIN	3.18 MIN
G	.015 MIN	.38 MIN
H	.125-.135	3.18-3.43
J	.300-.320	7.62-8.13
K	.245-.255	6.22-6.48
L	.009-.015	.23-.38

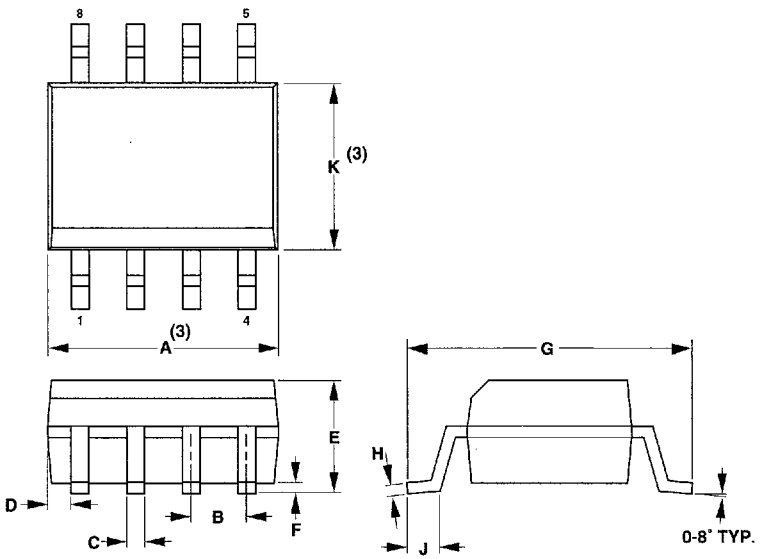


Notes:
1. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B, 7/85). Except for joining of Pins 4-5 and Pins 12-13.
2. Controlling dimension: inches.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

PI-1844-050196

T08A — Plastic SO-8

DIM	Inches	mm
A	0.189-0.197	4.80-5.00
B	0.050 TYP	1.27 TYP
C	0.014-0.019	0.35-0.49
D	0.012 TYP	0.31 TYP
E	0.053-0.069	1.35-1.75
F	0.004-0.010	0.10-0.25
G	0.228-0.244	5.80-6.20
H	0.007-0.010	0.19-0.25
J	0.021-0.045	0.51-1.14
K	0.150-0.157	3.80-4.00



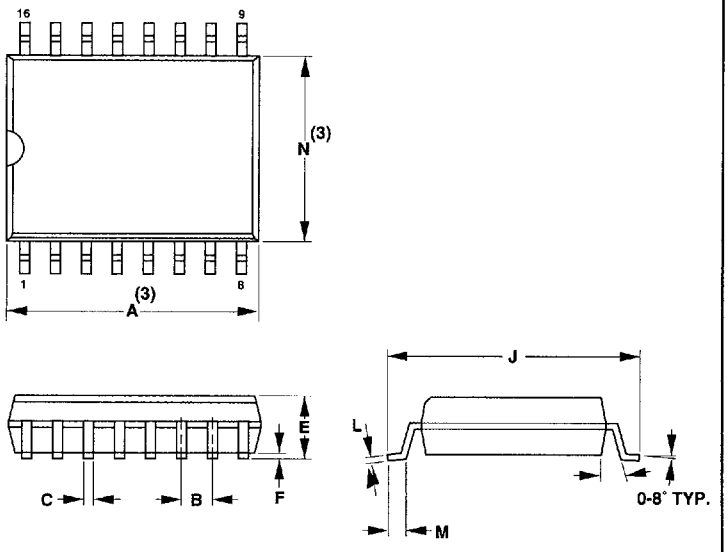
Notes:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75 mm (.150 inch) body width (issue A, June 1985).
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified edge by chamfer on top of the package body or indent on Pin 1 end.

PI-1845-050196

S16A — Plastic SO-16 (W)

DIM	inches	mm
A	.398-.413	10.10-10.50
B	.050 BSC	1.27 BSC
C	.014-.018	0.36-0.46
E	.093-.104	2.35-2.65
F	.004-.012	0.10-0.30
J	.394-.418	10.01-10.62
L	.009-.012	0.23-0.32
M	.020-.040	0.51-1.02
N	.291-.299	7.40-7.60

Notes:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50 mm (.300 inch) body width (issue A, June 1985).
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified by chamfer on top edge of the package body or indent on Pin 1 end.

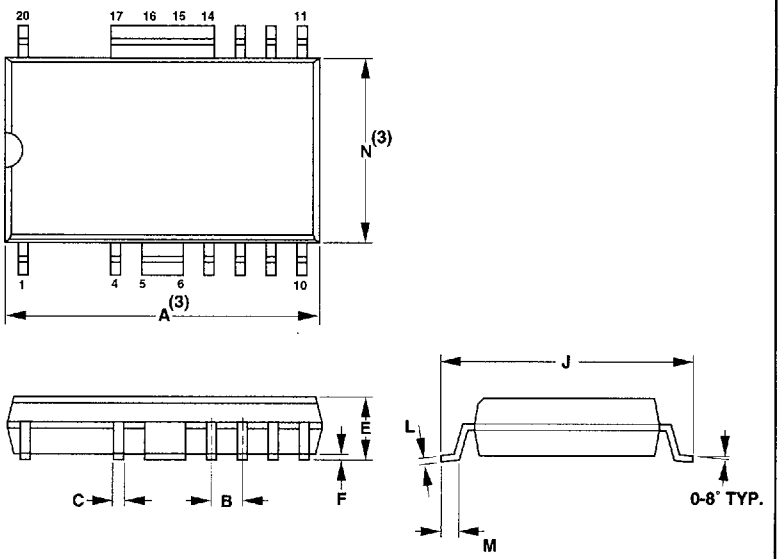


PI-1846-050196

S20B — Plastic SO-20

DIM	inches	mm
A	.496-.512	12.60-13.00
B	.050 BSC	1.27 BSC
C	.014-.019	0.35-0.49
E	.093-.104	2.35-2.65
F	.004-.012	0.10-0.30
J	.394-.419	10.00-10.65
L	.009-.013	0.23-0.32
M	.016-.050	0.40-1.27
N	.291-.299	7.40-7.60

Notes:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50 mm (.300 inch) body width (issue A, June 1985). Except for joining of Pins 5-6 and Pins 13-14-15.
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified by chamfer on top edge of the package body or indent on Pin 1 end.



PI-1847-050196

5

Tape & Reel Ordering Information

Power Integrations, Inc. makes selected surface-mount parts available in tape and reel form for use with automatic pick-and-place equipment. Tape and reel specifications meet or exceed industry standard specification EIA-481.

Ordering Information

Parts available in tape and reel form can be ordered by placing a T&R ordering suffix after the base part number. Standard orientation is Pin 1 Left. The ordering suffix for this orientation (see Figure 1) is TL. For example:

Base Part #	T&R Suffix
INT100S	-TL

Please contact the factory for other options. Minimum order size is 1 reel per line item, and all orders will be in multiples of full reel quantities. The quantity per reel for each package type is shown in Table 1. Power Integrations normal terms and conditions apply.

Electrical Specifications

Parts are subjected to the Power Integrations standard test flow, after which the parts are loaded into the tape cavities and sealed with a cover tape using standard anti-static handling procedures. The tape and cover are constructed of conductive modified polystyrene, providing a surface resistivity of $\leq 10^6$ Ω/square. The reel is made of polystyrene with a topical anti-static coating, providing a surface resistivity of $\leq 10^{11}$ Ω/square.

Physical Specifications

Physical specifications of the tape, cover, and reel are governed by EIA-481. Physical dimensions of the tapes are given in Figure 2 and Table 2, and physical dimensions of the reels are given in Figure 3 and Table 3.

Packaging for Shipment

Power Integrations supplies the following information on the side of each reel for ease of product identification:

- Power Integrations part number (MPN), including orientation suffix
- Encapsulation date code (D/C)
- Assembly lot identification (LOT)
- Quantity (QTY)
- Tape and reel packing date code (R/D)

PACKAGE	TAPE		REEL DIA	REEL QTY
	WIDTH (W)	PITCH (P)		
SO-8	12mm	8mm	330mm	2500
SO-16 (W)	16mm	12mm	360mm	1000
SO-20	24mm	12mm	360mm	1000

Table 1. Primary Tape & Reel Dimensions and Reel Quantities.

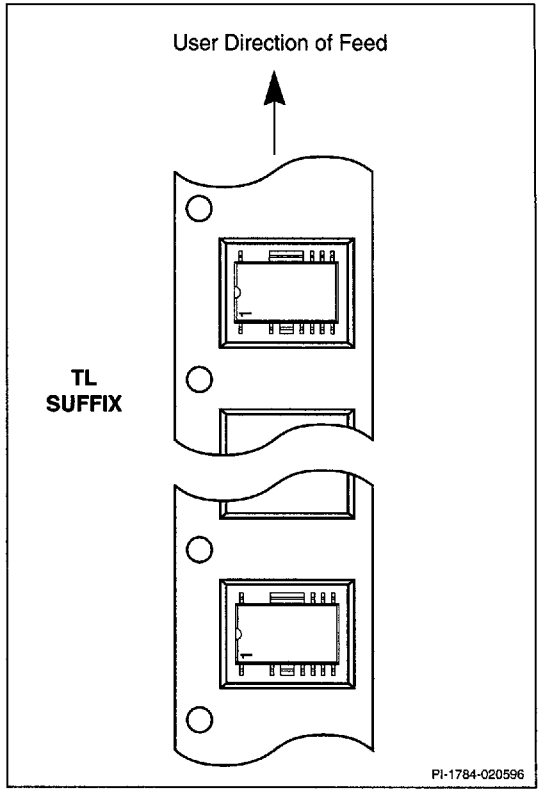


Figure 1. Part Orientation and Ordering Suffix.

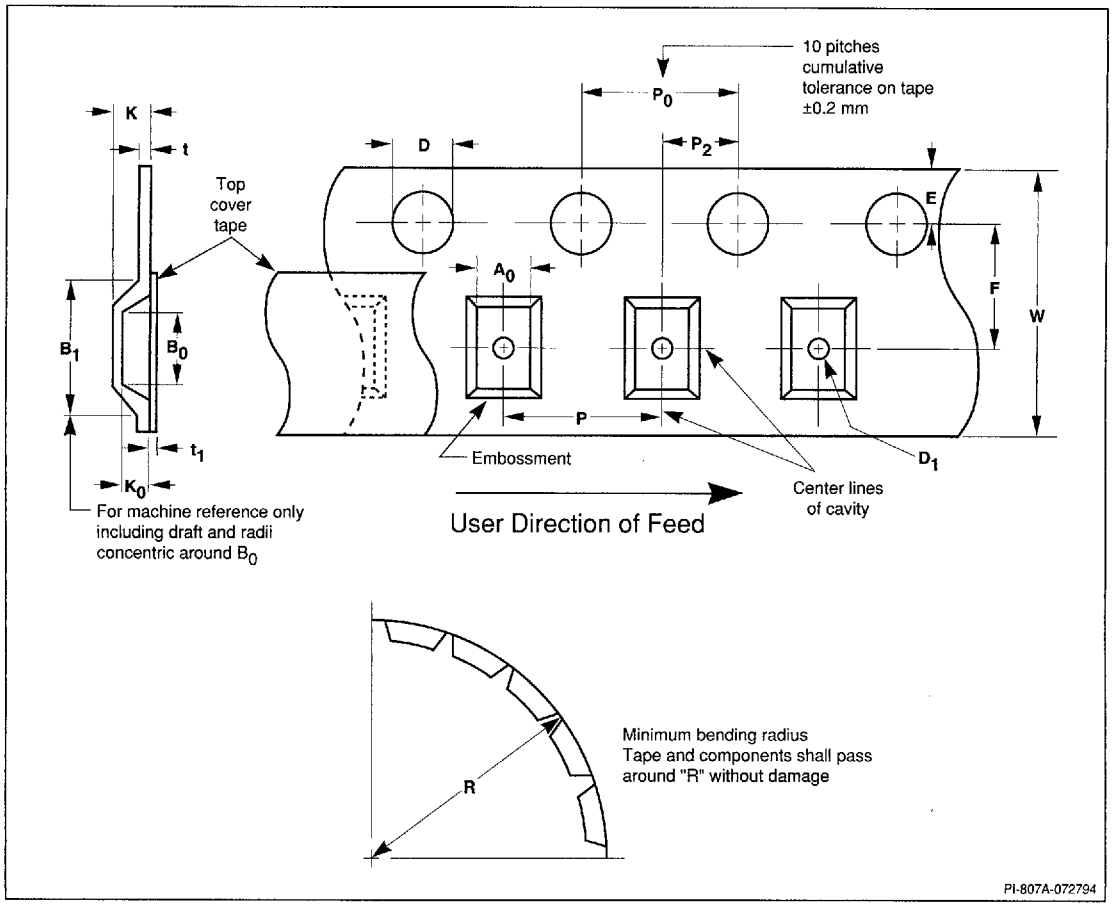


Figure 2. Tape Dimension Index.

Package Type	Tape Size	A_0	B_0	B_1	D	D_1	E	F	K
Plastic SO-8	12 mm	6.3-6.5	5.1-5.3	8.2 (max)	1.5-1.6	1.5 (min)	1.65-1.85	5.45-5.55	4.5 (max)
Plastic SO-16 (W)	16 mm	10.8-11.0	10.6-10.8	12.1 (max)	1.5-1.6	1.5 (min)	1.65-1.85	7.40-7.60	6.5 (max)
Plastic SO-20	24 mm	10.8-11.0	13.2-13.4	20.1 (max)	1.5-1.6	1.5 (min)	1.65-1.85	11.40-11.60	6.5 (max)

Package Type	Tape Size	K_0	P	P_0	P_2	R	t	t_1	W
Plastic SO-8	12 mm	2.00-2.20	7.9-8.1	3.9-4.1	1.95-2.05	30 (min)	0.400 (max)	0.10 (max)	11.7-12.3
Plastic SO-16 (W)	16 mm	2.90-3.10	11.9-12.1	3.9-4.1	1.90-2.10	40 (min)	0.400 (max)	0.10 (max)	15.7-16.3
Plastic SO-20	24 mm	2.90-3.10	11.9-12.1	3.9-4.1	1.90-2.10	50 (min)	0.400 (max)	0.10 (max)	23.7-24.3

Table 2. Tape Dimensions (in mm).

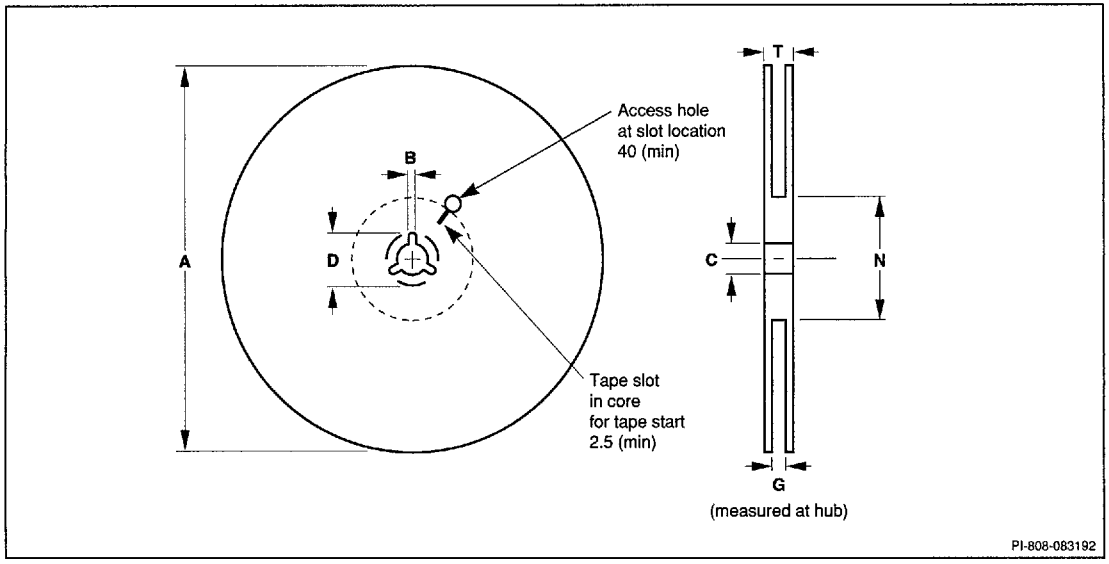


Figure 3. Reel Dimension Index.

Package Type	Tape Size	A	B	C	D	G	N	T
Plastic SO-8	12 mm	330 (max)	1.5 (min)	12.80-13.20	20.2 (min)	12.4-14.4	50 (min)	18.4 (max)
Plastic SO-16 (W)	16 mm	360 (max)	1.5 (min)	12.80-13.20	20.2 (min)	16.4-18.4	50 (min)	22.4 (max)
Plastic SO-20	24 mm	360 (max)	1.5 (min)	12.80-13.20	20.2 (min)	24.4-26.4	50 (min)	30.4 (max)

Table 3. Reel Dimensions (in mm).

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