



SMP60N06/05, SMP50N06/05

N-Channel Enhancement Mode Transistors

T-39-13

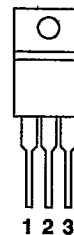
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
SMP60N06	60	0.023	60
SMP60N05	50	0.023	60
SMP50N06	60	0.028	50
SMP50N05	50	0.028	50

TO-220AB



TOP VIEW



- 1 GATE
- 2 DRAIN (Connected to TAB)
- 3 SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	SMP				UNITS	
		60N06	60N05	50N06	50N05		
Gate-Source Voltage	V_{GS}	± 20	± 20	± 20	± 20	V	
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	60	60	50	50	A
		$T_C = 100^\circ\text{C}$	38	38	31	31	
Pulsed Drain Current ¹	I_{DM}	240	240	200	200		
Avalanche Current (See Figure 9)	I_{AR}	60	60	50	50		
Avalanche Energy	E_A	90	90	62	62	mJ	
Repetitive Avalanche Energy ²	E_{AR}	18	18	18	18		
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	125	125	125	125	W
		$T_C = 100^\circ\text{C}$	50	50	50	50	
Operating Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150				$^\circ\text{C}$	
Lead Temperature ($1/16$ " from case for 10 sec.)	T_L	300					

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

¹Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

²Duty cycle $\leq 1\%$.

SMP60N06/05, SMP50N06/05



ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted) **T-39-13**

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS		UNIT
				MIN	MAX	
STATIC						
Drain-Source Breakdown Voltage	SMP60N06, 50N06 SMP50N06, 50N05	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	65 55	60 50	V
Gate Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0 4.0	
Gate-Body Leakage		I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V	10		±100 nA
Zero Gate Voltage Drain Current		I _{DSS}	V _{DS} = V _{(BR)DSS} , V _{GS} = 0 V			250 μA
			V _{DS} = 0.8 × V _{(BR)DSS} , V _{GS} = 0 V, T _J = 125°C			1000
On-State Drain Current ¹	SMP60N06, 60N05 SMP50N06, 50N05	I _{D(on)}	V _{DS} = 25 V, V _{GS} = 10 V		60 50	A
Drain-Source On-State Resistance ¹	SMP60N06, 60N05 SMP50N06, 50N05	r _{DS(on)}	V _{GS} = 10 V, I _D = 30 A	0.019 0.023		0.023 0.028 Ω
			V _{GS} = 10 V, I _D = 30 A T _J = 125°C	0.025 0.030		0.030 0.036
Forward Transconductance ¹		g _{fs}	V _{DS} = 25 V, I _D = 30 A	18	15	S
DYNAMIC						
Input Capacitance		C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	2900		pF
Output Capacitance		C _{oss}		1500		
Reverse Transfer Capacitance		C _{rss}		500		
Total Gate Charge ²		Q _g	V _{DS} = 0.5 × V _{(BR)DSS} , V _{GS} = 10 V, I _D = 60 A	70	100	nC
Gate-Source Charge ²		Q _{gs}		22	35	
Gate-Drain Charge ²		Q _{gd}		35	50	
Turn-On Delay Time ²		t _{d(on)}	V _{DD} = 30 V, R _L = 1 Ω I _D ≈ 130 A, V _{GEN} = 10 V, R _G = 2.5 Ω	20	40	ns
Rise Time ²		t _r		25	50	
Turn-Off Delay Time ²		t _{d(off)}		30	60	
Fall Time ²		t _f		20	40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	SMP60N06, 60N05 SMP50N06, 50N05	I _S			60 50	A
Pulsed Current ³		I _{SM}			190	
Forward Voltage ¹	SMP60N06, 60N05 SMP50N06, 50N05	V _{SD}	I _F = I _S , V _{GS} = 0 V		2.5 2.4	V
Reverse Recovery Time		t _{rr}	I _F = I _S , di _F /dt = 100 A/μs	75	100	ns
Reverse Recovery Charge		Q _{rr}		0.19		μC

¹Pulse test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).



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TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

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Figure 1. Output Characteristics

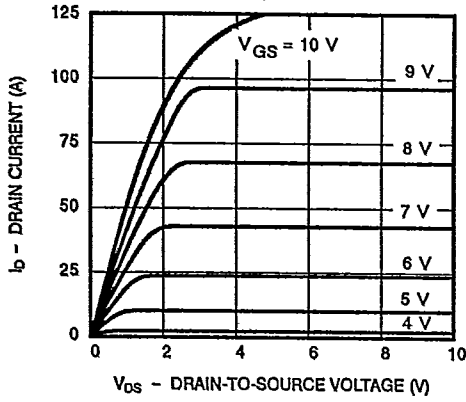


Figure 2. Transfer Characteristics

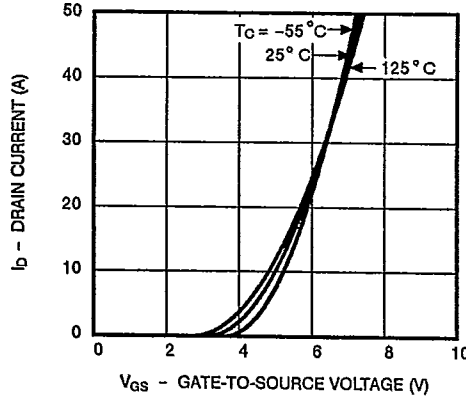


Figure 3. Transconductance

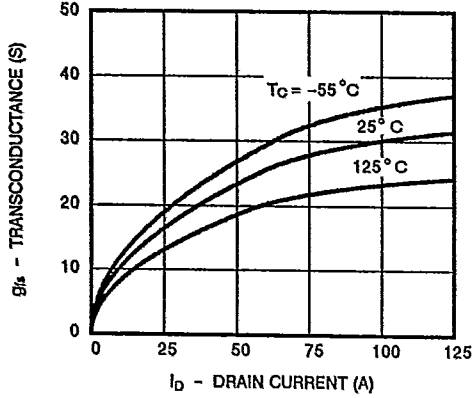
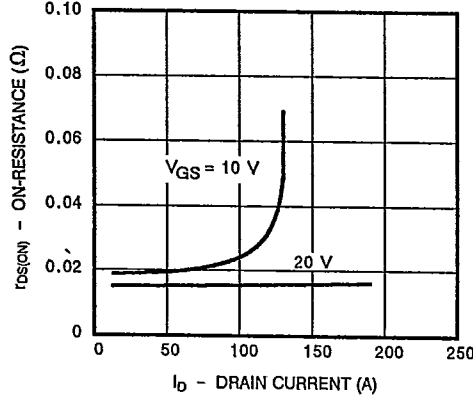


Figure 4. On-Resistance



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Figure 5. Capacitance

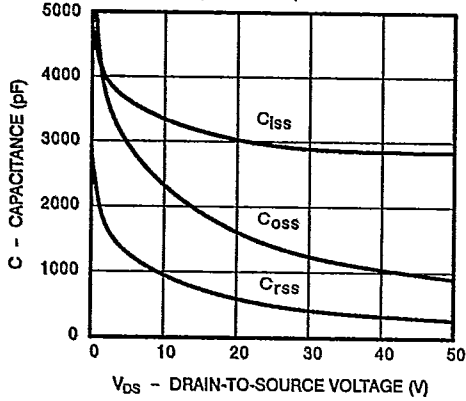
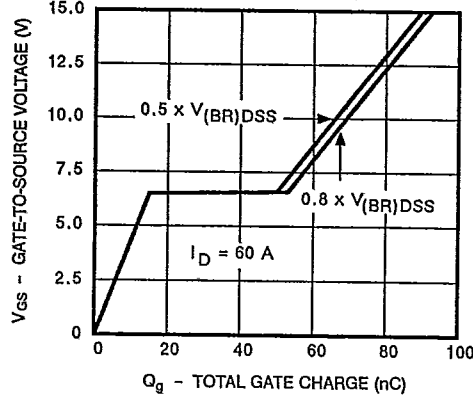


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

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Figure 7. On-Resistance vs. Junction Temperature

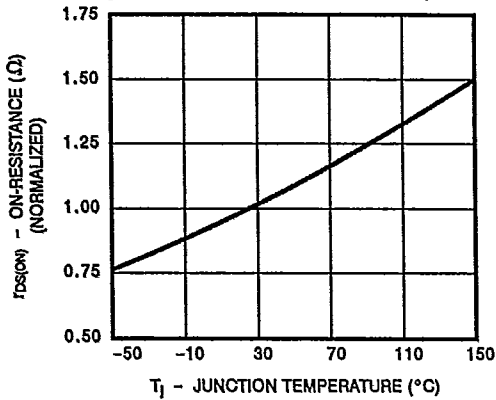
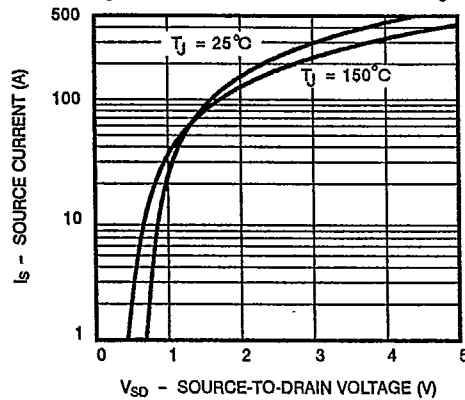


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

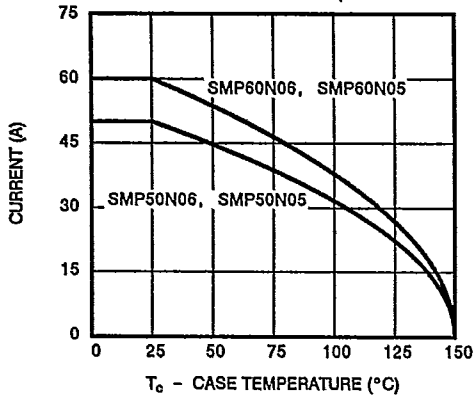


Figure 10. Safe Operating Area

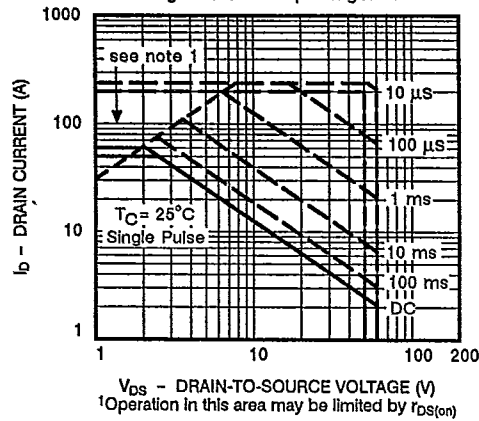


Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

