SMR200
Data Sheet

DUAL-TRACK
MAGNETIC STRIPE F2F
DECODER IC

For More Information

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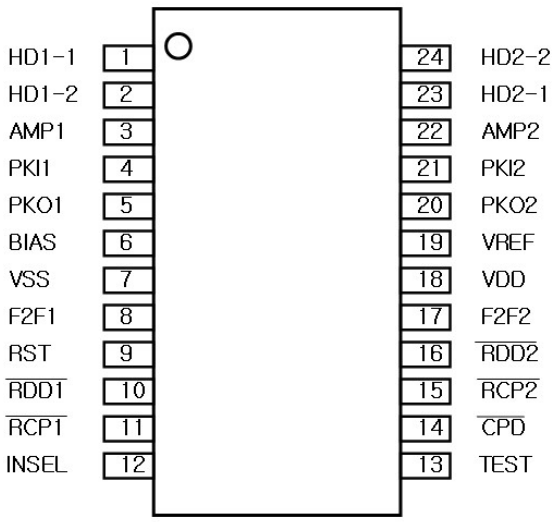
DESCRIPTION

SMR200 is a CMOS Integrated Circuit device, which is providing high functional F2F Decoding for Magnetic Card Reader. SMR200 provides decoding function for magnetic stripe storage system, with all the analog and digital circuits in a single chip.

PACKAGE (TOP VIEW)

24PIN SSOP

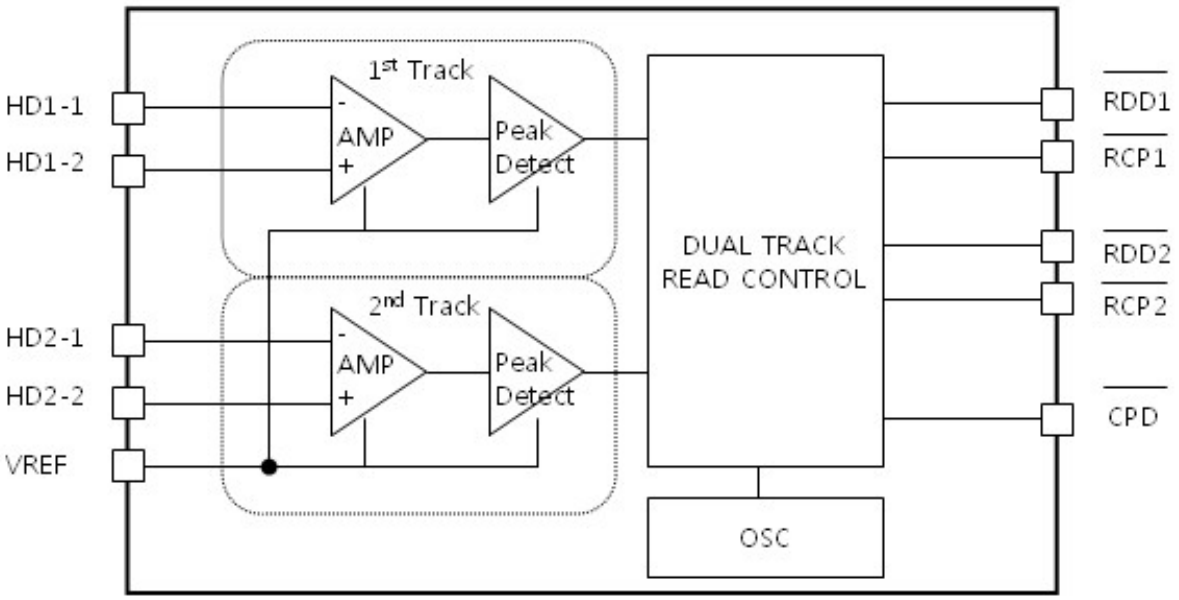


FEATURES

- Low power CMOS Technology
- Dual Track F2F decode
- Enhanced Noise Protection
- Low power dissipation

- Wide operating voltage range :
  VDD= 3.0V ~ 5.5V
- Wide operating temperature range :
  Ta = -35°C ~ +75°C

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No	Name	I/O	Description	Notes
1	HD1-1	I	Head Input 1(-)	Track-1
2	HD1-2	I	Head Input 1(+)	Track-1
3	AMP1	O	Amplifier Output 1	Track-1
4	PKI1	I	Peak Detect Input 1	Track-1
5	PKO1	O	Peak Detect Output 1	Track-1
6	BIAS	I	External Bias	Bias resistor
7	VSS	G	Negative Power Supply	Ground
8	F2F1	I/O	F2F Input/Output 1	Track-1
9	/RST	I	Reset	Active low
10	/RDD1	O	Read Data 1	Track-1
11	/RCP1	O	Read Clock Pulse 1	Track-1
12	INSEL	I	F2F Input Select	F2F external input at low
13	TEST	O	Test Out	Test Out
14	/CPD	O	Card Present Detect	Internally Pulled-up
15	/RCP2	O	Read Clock Pulse 2	Track-2
16	/RDD2	O	Read Data 2	Track-2
17	F2F2	I/O	F2F Input/Output 2	Track-2
18	VDD	P	Positive Power Supply	3.0V~5.5V
19	VREF	O	Reference Voltage	VDD/2
20	PKO2	O	Peak Detect Output 2	Track-2
21	PKI2	I	Peak Detect Input 2	Track-2
22	AMP2	O	Amplifier Output 2	Track-2
23	HD2-1	I	Head Input 2(-)	Track-2
24	HD2-2	I	Head Input 2(+)	Track-2

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Non-Operating)

DC Supply Voltage	0 to 7 Volt
Voltage Input Range	0 to V_{DD}
Input Current	20 mA
Output Current	10 mA
Storage Temperature Range	-55°C ~ +150°C
Lead Temperature	260°C

Recommended Operating Conditions

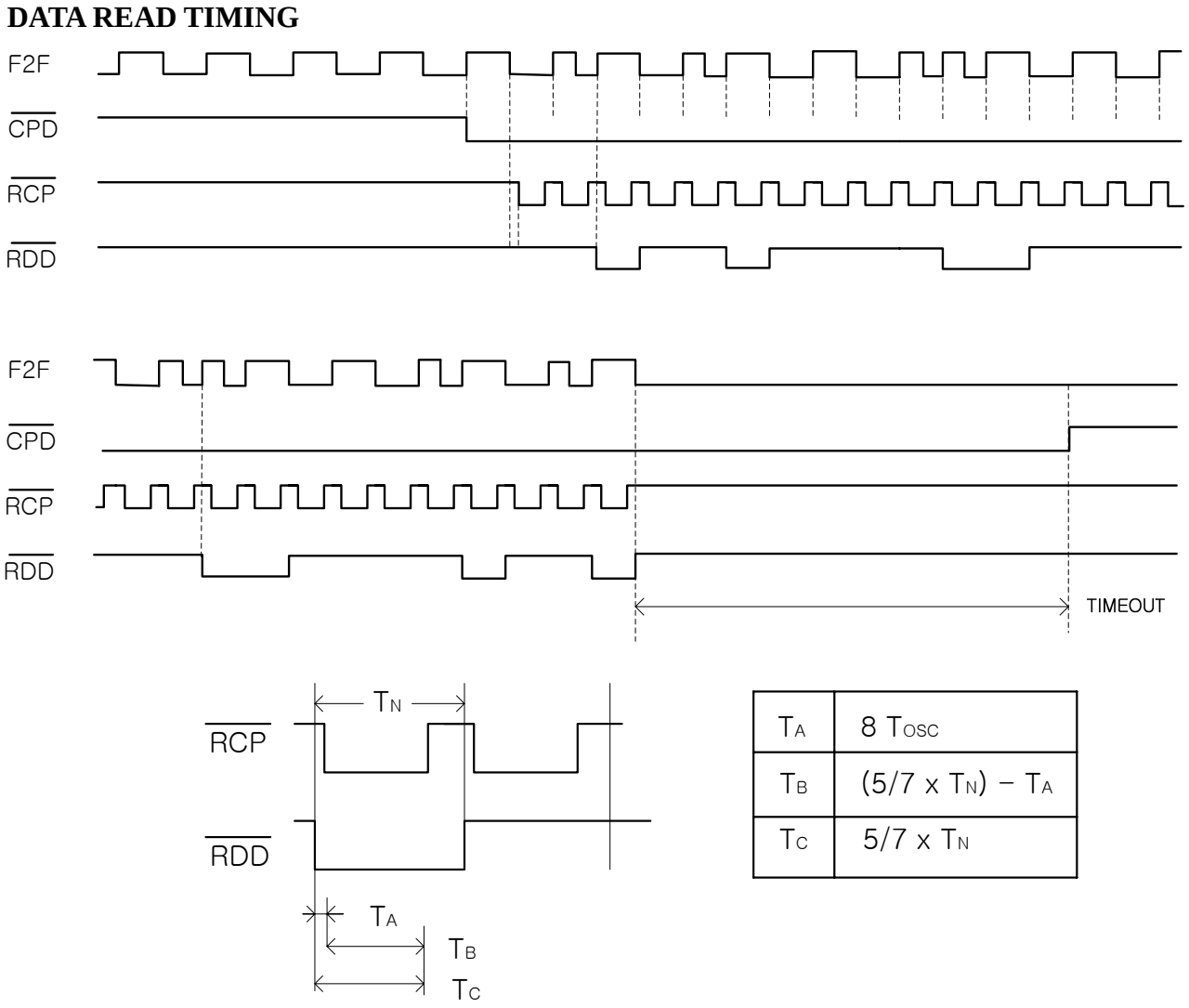
Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		3.0		5.5	V
Operating Temperature	T_{OPR}		-35		+75	°C
Reference Voltage	V_{REF}			$V_{DD}/2$		V
Oscillator Frequency	Osc	V_{DD}=5.0V	2.0	2.5	3.0	MHz
Output Voltage /RDD,/RCP,/CPD	V_{OH}	V_{DD} =5.0V I_{OH}=10mA	4.5			V
		V_{DD} =3.0V I_{OH} =8mA	2.5			V
	V_{OL}	V_{DD} =5.0V I_{OL} =10mA			0.4	V
		V_{DD} =3.0V I_{OL} =6mA			0.4	V
Operating Current	I_{DD}	V_{DD} =5.0V		1.8		mA
		V_{DD} =3.0V		1.2		mA
Standby Current	I_{STBY}	V_{DD} =5.0V		1.8		mA
		V_{DD} =3.0V		0.8		mA

FUNCTIONAL DESCRIPTION

SMR200 provides decoding function for magnetic stripe storage system, with all the analog and digital circuits in a single chip. F2F pattern signal is generated by analog signal processing through an amplifier OP1, peak detector OP2 and comparator. The operation of digital logic for data generation is activated by triggering oscillation circuit as soon as detecting F2F pattern transition. Card Present Detect ($\overline{CPD}$) signal becomes active state after null 8 bits from the first bit reading. And also proper $\overline{RDD}$ and $\overline{RCP}$ signals are generated. Misreading prevention circuits are implemented to provide high reliability by fixing up new reference bit when broken bits are detected.

SIGNAL TIMING DIAGRAM

DATA READ TIMING



T_A	8 T_{OSC}
T_B	(5/7 x T_N) − T_A
T_C	5/7 x T_N

Fig. 1

NOTE:

1. 8 or 9 head flux reversal for low density configuration.
2. TIMEOUT of the $\overline{CPD}$ signal occurs approx. 18 ms after last Head Signal transition.
3. The $\overline{RDD}$ is valid at 8 T_{OSC}(3.2 μs min.) before the negative edge of the $\overline{RCP}$.
4. The low pulse width of $\overline{RCP}$ is approx. 70% of bit time.

- $\overline{RDD}$
  The Data signal is valid while the $\overline{RCP}$ is low. If $\overline{RDD}$ signal is high, the logical value of the bit is zero(0). If low, then the logical value of the bit is high(1).

- $\overline{RCP}$
  The $\overline{RCP}$ signal indicates that $\overline{RDD}$ is valid. The $\overline{RDD}$ should be loaded and stable before the RCP signal goes low (negative edge).

- $\overline{CPD}$
  Card Present Detect signal goes low after the 8 or 9th flux reversal, and it returns to high when approx. 18 ms was elapsed.
  When no card is being inserted through magnetic reader system, the $\overline{RDD}$, $\overline{RCP}$ and $\overline{CPD}$ signals stay high.

RECOMMENDED OPERATING CONDITIONS

DUAL TRACK

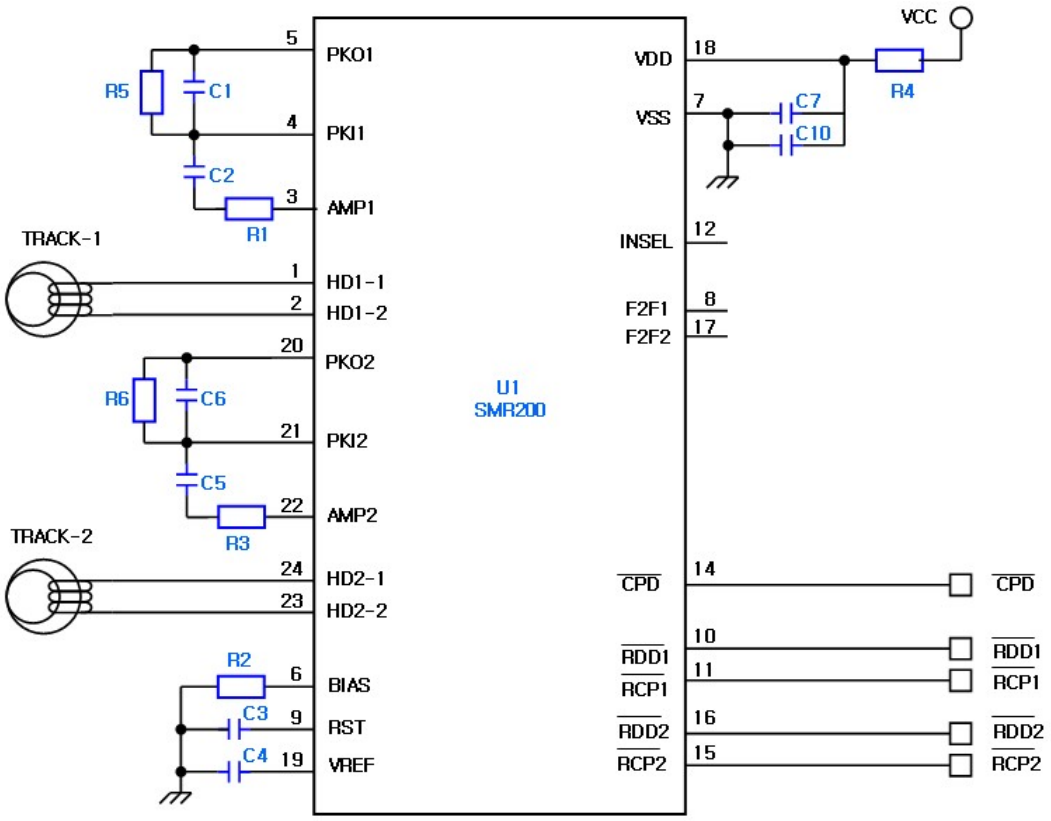


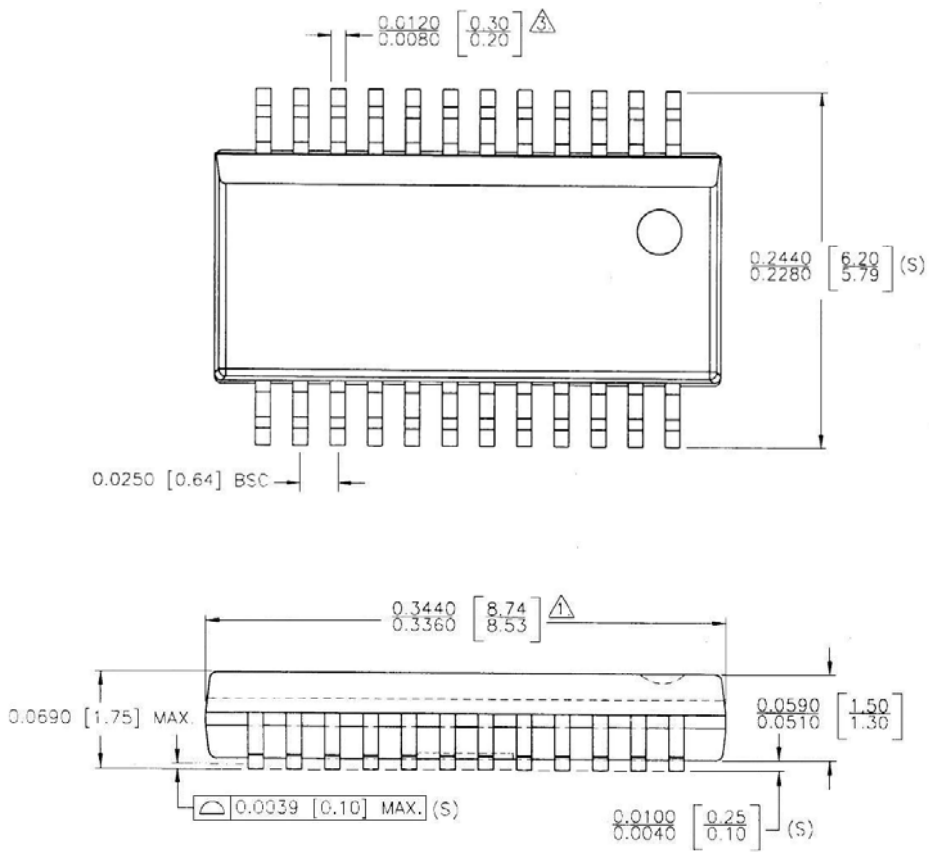
Fig. 2

Recommended component values

PART	210BPI	75BPI	REMARK
R1, R3	1 KΩ	2.7 KΩ	
R2	24KΩ		OSC=1.5MHz~2.5MHz
R5, R6	10MΩ	10MΩ	
R4	4.7Ω		
C1, C6	470 pF	750 pF	
C2, C5	0.022 µF	0.022µF	
C3, C4, C7	0.1 µF		
C10	10 µF		

The above schematics and part values are provided only for reference.

PACKAGE DIMENSION



1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .006 IN PER SIDE.
2. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN PER SIDE.
3. DOES NOT INCLUDE DAMBAR PROTRUSIONS. ALLOWABLE DAMBAR PROTRUSIONS SHALL BE 0.004 IN.
4. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-137 AE.