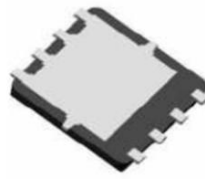
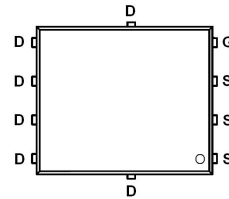
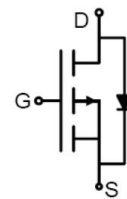


Main Product Characteristics:

V_{DS}	-30V
$R_{DS(on)}$	1.9m Ω (typ.)
I_D	-131A


PDFN5x6-8L

Pin Assignments

Schematic Diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ①	-131	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ①	-83	
I_{DM}	Pulsed Drain Current ②	-524	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ③	69	W
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

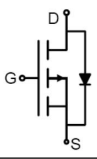
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	1.8	$^{\circ}\text{C}/\text{W}$

Electrical Characteristics @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

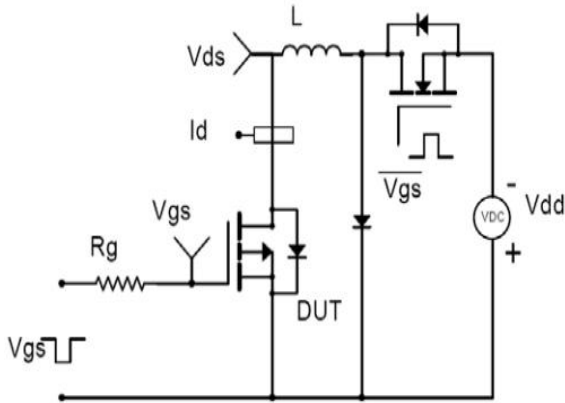
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	-30	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	1.9	2.5	m Ω	$V_{GS} = -10\text{V}, I_D = -20\text{A}$
		—	2.7	3.6		$V_{GS} = -4.5\text{V}, I_D = -20\text{A}$
$V_{GS(th)}$	Gate threshold voltage	-1	—	-2.5	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
I_{DSS}	Drain-to-Source leakage current	—	—	-1	μA	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
		—	—	-100		$V_{GS} = -20\text{V}$
C_{iss}	Input capacitance	—	12750	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output capacitance	—	1330	—		$V_{DS} = -15\text{V}$
C_{rss}	Reverse transfer capacitance	—	1200	—		$f = 1\text{MHz}$
Q_g	Total gate charge	—	20	—	nC	$I_D = -20\text{A},$
Q_{gs}	Gate-to-Source charge	—	2.5	—		$V_{DS} = -15\text{V},$
Q_{gd}	Gate-to-Drain("Miller") charge	—	3	—		$V_{GS} = -10\text{V}$
$t_{d(on)}$	Turn-on delay time	—	20	—	ns	$V_{GS} = -10\text{V}, V_{DS} = -15\text{V},$ $R_{GEN} = 3\Omega, R_L = 0.75\Omega$
t_r	Rise time	—	4	—		
$t_{d(off)}$	Turn-Off delay time	—	23	—		
t_f	Fall time	—	37	—		

Source-Drain Ratings and Characteristics

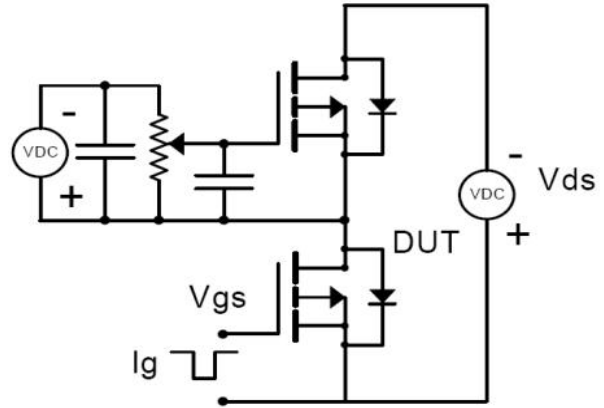
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-131	A	MOSFET symbol showing the integral reverse p-n junction diode 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	-524	A	
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$I_S = -20\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	40	—	ns	$T_J = 25^{\circ}\text{C}, I_F = -20\text{A}, di/dt = -100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge	—	30	—	nC	

Test Circuits and Waveforms

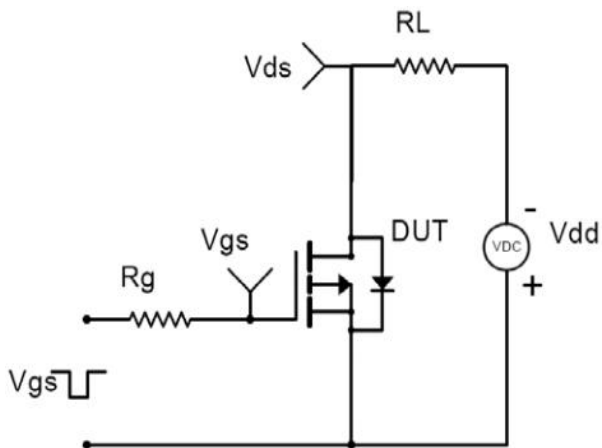
EAS Test Circuit:



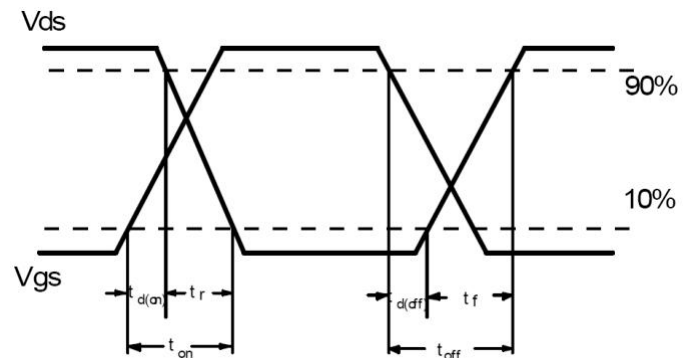
Gate Charge Test Circuit:



Switching Time Test Circuit:

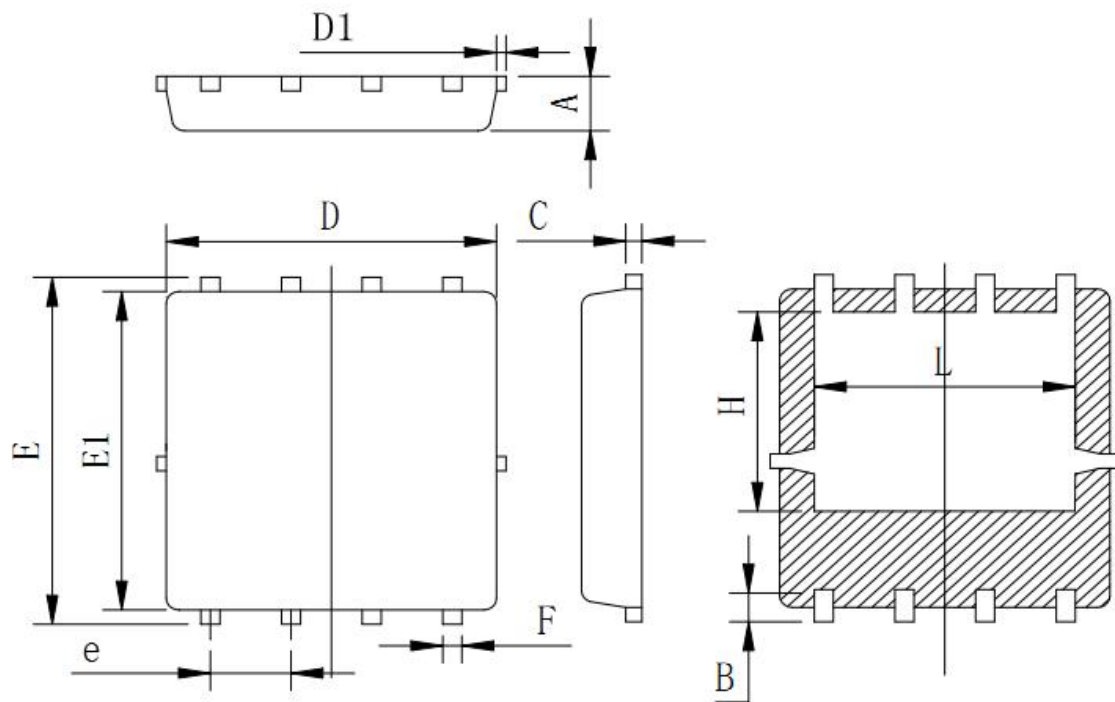


Switching Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.

Mechanical Data:


Symbol	Min	Typ	Max
A	0.90	0.95	1.00
B	0.48	0.58	0.68
C	0.20	0.254	0.30
D	5.00	5.20	5.40
D1			0.15
E	5.90	6.05	6.20
E1	5.40	5.55	5.70
e	1.22	1.27	1.32
F	0.25	0.30	0.35
H	3.27	3.47	3.67
L	3.80	4.00	4.20

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