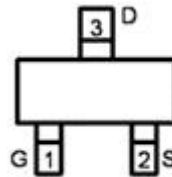


Main Product Characteristics:

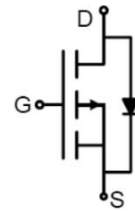
V_{DSS}	-30V
$R_{DS(on)}$	50.5m Ω (typ)
I_D	-3.3A



SOT-23



Pin Assignments



Schematic Diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature



Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

Absolute Max Rating:

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$ ①	-3.3	A
I_{DM}	Pulsed Drain Current ②	-13.2	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ③	1.14	W
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	$^\circ\text{C}$

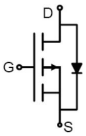
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ($t \leq 10s$) ^④	—	110	°C/W

Electrical Characteristics @ $T_A=25^\circ\text{C}$ unless otherwise specified

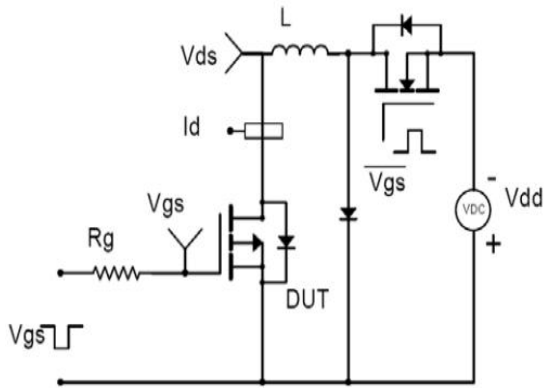
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	50.5	65	m Ω	$V_{GS}=-10V, I_D = -3A$
		—	68	90	m Ω	$V_{GS}=-4.5V, I_D = -2A$
$V_{GS(th)}$	Gate threshold voltage	-1	—	-2	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
I_{DSS}	Drain-to-Source leakage current	—	—	-1	μA	$V_{DS} = -30V, V_{GS} = 0V$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source reverse leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	5.6	—	nC	$I_D = -3A$
Q_{gs}	Gate-to-Source charge	—	0.9	—		$V_{DD}=-15V$
Q_{gd}	Gate-to-Drain("Miller") charge	—	1.4	—		$V_{GS} = -10V$
$t_{d(on)}$	Turn-on delay time	—	11	—	nS	$V_{GS}=-10V,$
t_r	Rise time	—	55	—		$V_{DS} = -15V,$
$t_{d(off)}$	Turn-Off delay time	—	15	—		$R_{GEN}=2.5\Omega$
t_f	Fall time	—	8	—		$I_D = -3A$
C_{iss}	Input capacitance	—	262	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	52	—		$V_{DS} = -15V$
C_{rss}	Reverse transfer capacitance	—	42	—		$f = 1MHz$

Source-Drain Ratings and Characteristics

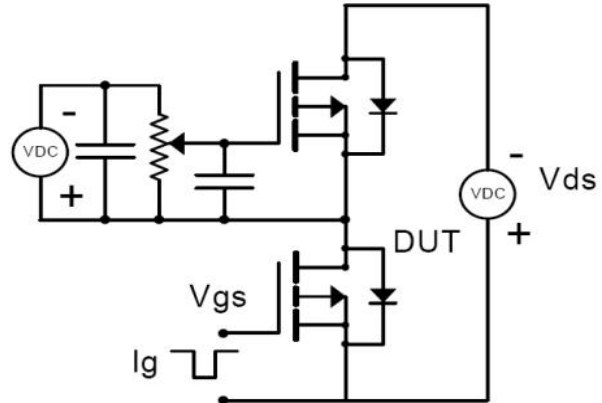
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ①	—	—	-3.3	A	MOSFET symbol showing the integral reverse p-n junction diode 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-13.2	A	
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$I_S=-3A, V_{GS}=0V, T_J = 25^\circ\text{C}$
t_{rr}	Reverse Recovery Time	—	8	—	ns	$T_J = 25^\circ\text{C}, I_F = -3A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	3	—	nC	

Test Circuits and Waveforms:

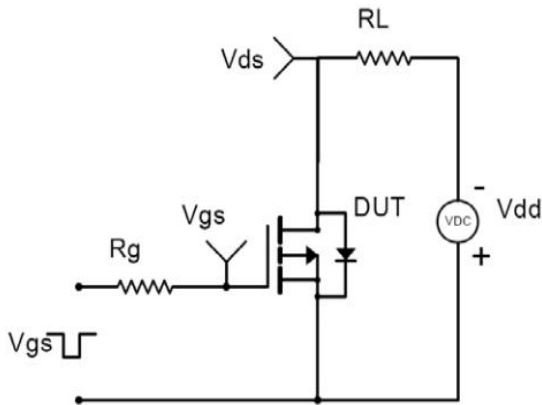
EAS Test Circuit:



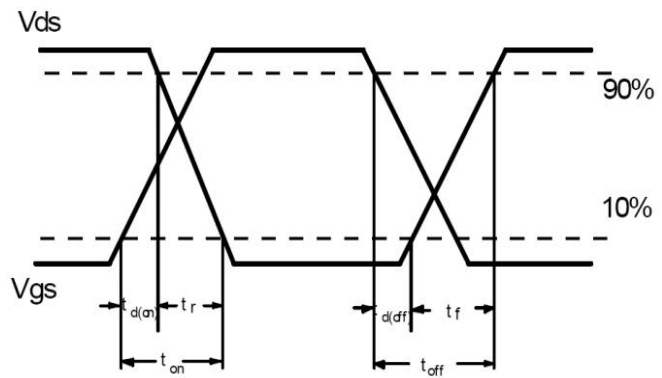
Gate Charge Test Circuit:



Switching Time Test Circuit:

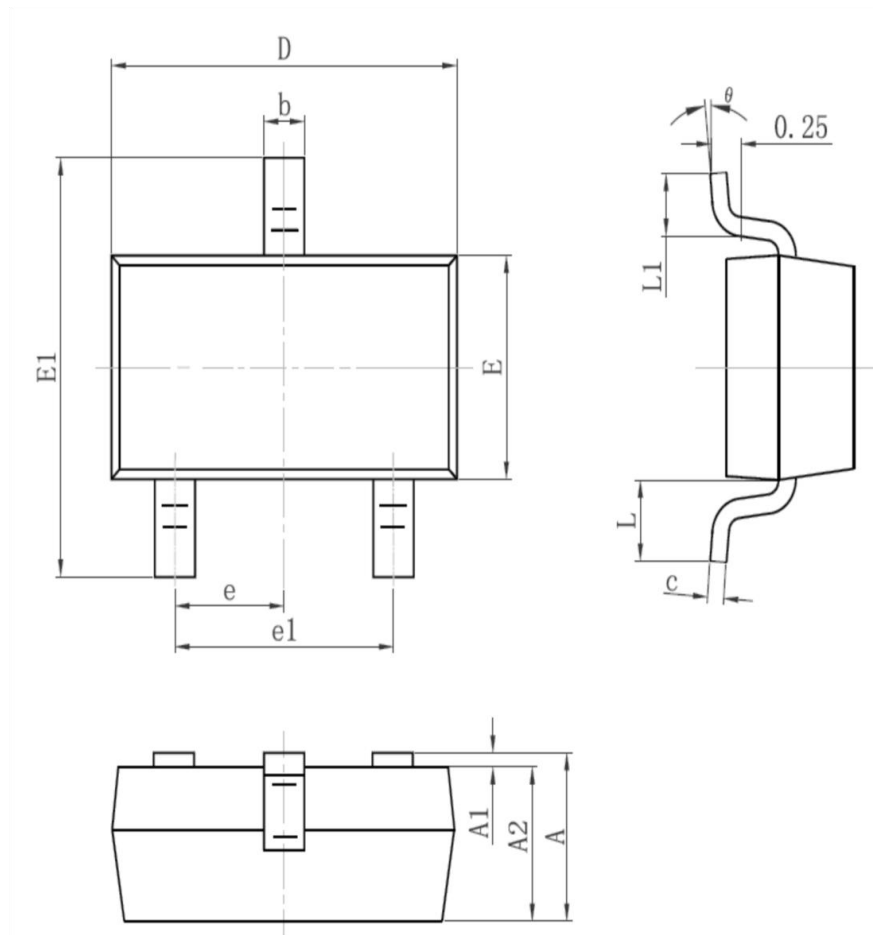


Switching Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Mechanical Data:
SOT-23 PACKAGE OUTLINE DIMENSION


Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.95TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.55REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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