Preliminary Information[1] *(See Last Page)*

Four-Channel Loss-Less Trakker™ Power Supply Manager

FEATURES & APPLICATIONS

- **Loss-Less Tracking function**
  - **No power MOSFET switches**
- **Programmable Slew-Rate, Tracking and Voltage Monitoring Functions**
- **Directly Interfaces to DC-DC Converters, Monolithic Controllers or LDOs**
- **Programmable Sequence Orders**
- **Programmable Tracking Slew Rates**
- **Eliminates Series Power MOSFETs**
- **Programmable OV/UV Threshold Limits**
- **Under Voltage Lock-Out (VDD and VCTRL_SUP)**
- **4k-Bit user configurable Nonvolatile Memory**
- **I^2C 2-wire serial bus for programming configuration and monitoring status**

Applications

- **Monitor, Sequence and Slew-Rate Control of Distributed Power and Point of Use Power Supplies**
- **Multi-voltage Processors, DSPs, ASICs used in Telecom, CompactPCI or server systems**

INTRODUCTION

The SMT4504 is an intelligent power supply sequencer, tracker, and voltage monitor. The SMT4504 tracks or sequences up to 4 power supplies by uniquely controlling the Enable and TRIM (Soft-Start) functions of DC-DC converters, Monolithic Controllers or LDOs. Each Channel is individually programmable for undervoltage/overvoltage threshold settings, sequence position and slew rates. Two or more supplies allocated to the same sequence position are tracked, while assigning individual supplies to a unique sequence position causes them to be sequenced with controlled slew rates.

The SMT4504 monitors the supplies for faults and is programmable to take any of several actions upon the occurrence of a fault. The voltage monitoring threshold step size is better than ±1%.

Power supply sequencing can be executed in any order. During power-off sequencing, the SMT4504 sequences the supplies in the reverse order as power-on.

Using the I^2C interface, a host system can communicate with the SMT4504 status register, optionally control power-on/off software and utilize 4K-bits of nonvolatile memory.

SIMPLIFIED APPLICATIONS DRAWING

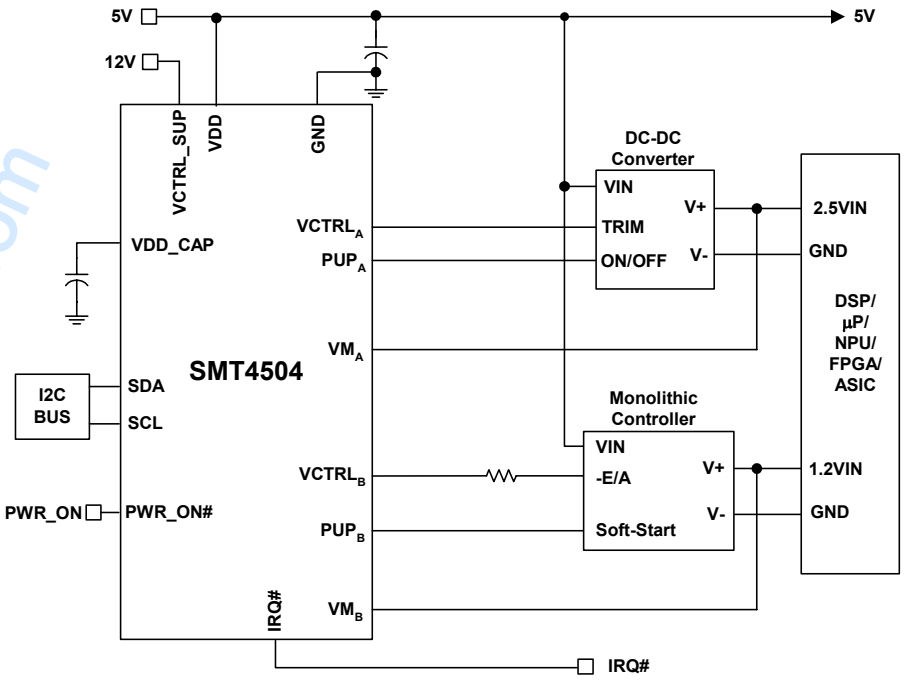


Figure 1 – Applications Schematic, the SMT4504 Loss-Less Trakker™ can track different types of supplies together. Note: This is an applications example only. Some pins, components and values are not shown.

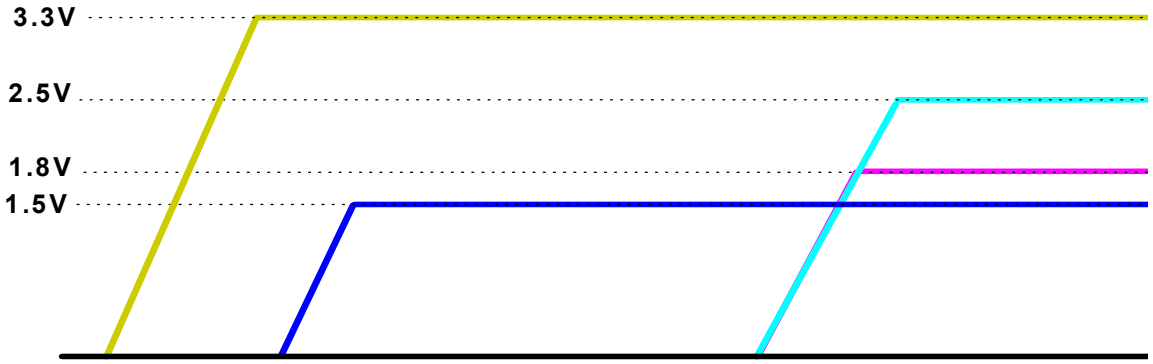


Figure 2A – Example Power Supply Sequencing and Tracking using the SMT4504. Any order of supply sequencing/tracking can be applied using the SMT4504.

GENERAL DESCRIPTION

The SMT4504 consists of several major functional blocks: the power supply monitors, the sequencing and tracking outputs; the programmable output circuitry; the timing and control block; the I^2C interface and the nonvolatile memory array.

The analog acquisition system monitors all channels via the OV/UV sensors. The UV/OV sensors are the four power supply voltage channels and the VDD and VCTRL_SUP supplies. The setting of the OV/UV trip points is made via the I^2C serial data port.

Once PWR_ON is asserted a programmable delay timer must first expire after which the PUP (Point of Use Power) output(s) so required are enabled. The PUPs are generally connected to the Enable pin of the converter controlled by the SMT4504 Any channel not requiring closed-loop tracking of the voltage is programmed to assert its output (PUP) once the previous sequence timer has expired. Otherwise all PUPs are asserted upon the completion of the PWR_ON delay timer.

The power supply manager block is also used to assign a given power supply a sequence position; sequence timeout period and track-up/down slew rate setting. These settings determine the time and the rate at which each supply is turned on. When more than one supply is assigned to a sequence position their voltages will be tracked during the period of time when they are turned on via the $VCTRL_X$ pins and monitored via the VM_X pins. These events are controlled by the sequence and tracking block.

An additional feature of the SMT4504 allows the supplies that are assigned the same sequence position to be tracked at the same or different slew rates for applications requiring supplies to be started at the same time but to ramp up at different rates. (Figure 2A)

The next major block is a programmable output block. The SMT4504 provides a great deal of flexibility in choosing the fault trigger source for the fault outputs. The sources include multiple combinations of UV/OV conditions. The fault outputs' assertion polarities are also programmable.

Programming of the SMT4504 is performed over the industry standard I^2C, 2-wire serial data interface. It allows configuration of the device, real-time control of the power-on/power-off processes and reading of the status registers. The bus interfaces the host to 4k bits of nonvolatile memory and the programmable configuration registers.
The 4k bits of user configurable nonvolatile memory uses industry standard non-volatile memory technology.

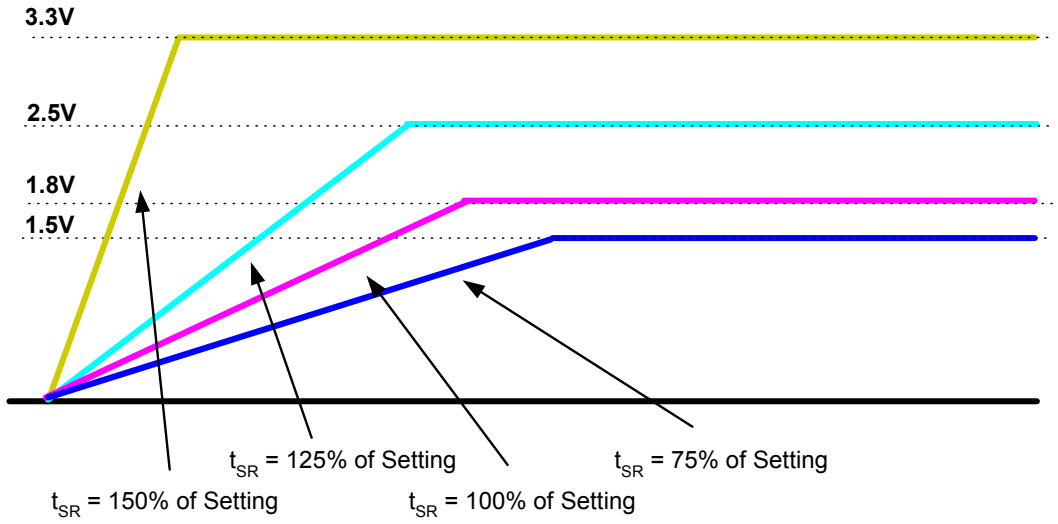
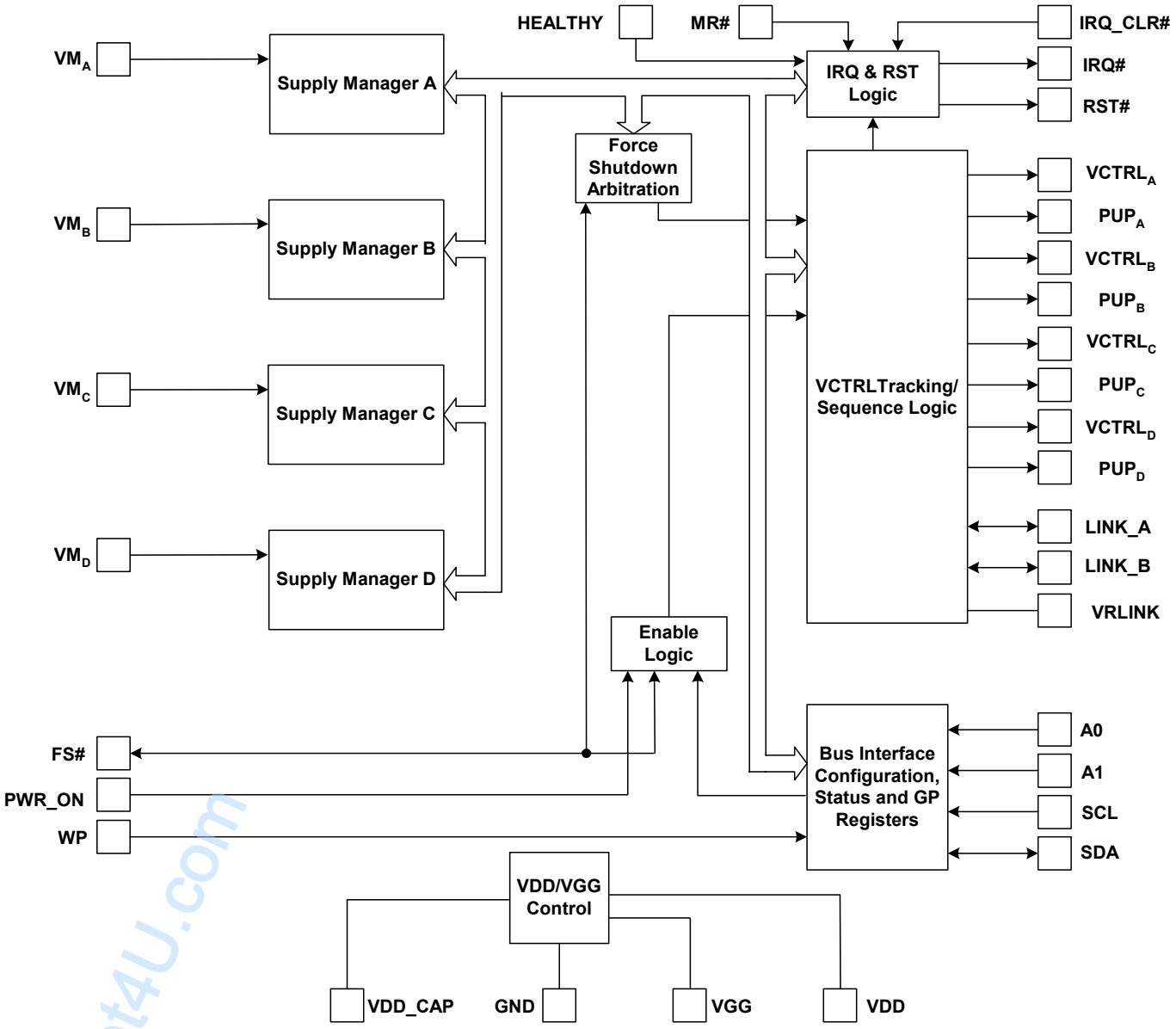


Figure 2B – Example Power Supply Tracking flexibility using the SMT4xx4 set to the same sequence position but different slew rates on each channel.

SIMPLIFIED BLOCK DIAGRAM



PIN DESCRIPTIONS

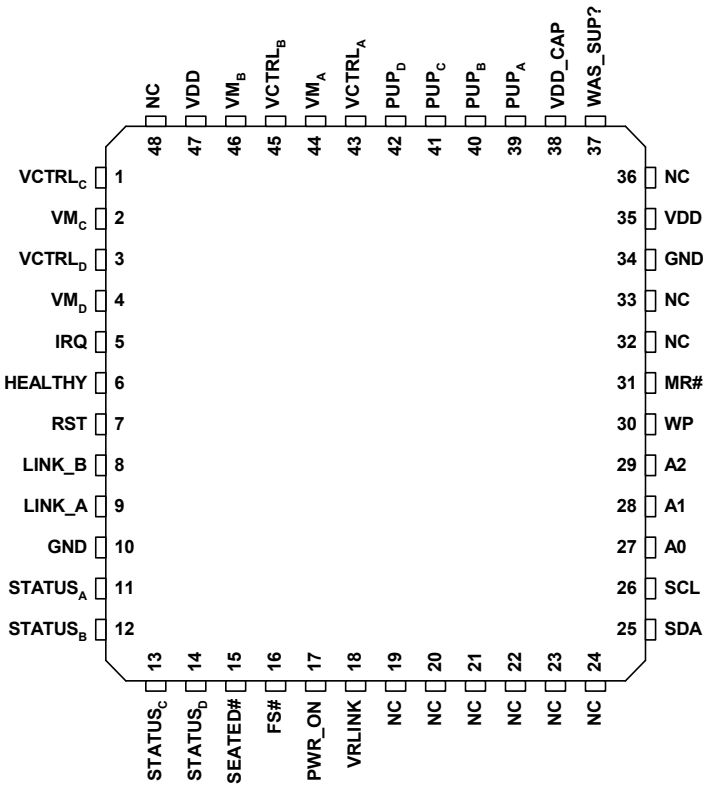
Pin Name	Type	Number	Function
$VCTRL_C$	OUT	1	Control voltage used to track/sequence the converters
VM_C	IN	2	Channel C converter output or sense+ line
$VCTRL_D$	OUT	3	Control voltage used to track/sequence the converters
VM_D	IN	4	Channel D converter output or sense+ line
IRQ	OUT	5	Programmable active high/low open drain latched output. Asserted when programmed power supply is in a fault condition.
HEALTHY	OUT	6	Programmable active high/low output asserted when all Fault conditions are clear
RST	OUT	7	Programmable active high/low open drain output signals when all programmed power supplies are within the monitored limits and the MR signal is inactive. RST has a programmable timeout period with options for 0.64/50/100/200ms.
LINK_B	I/O	8	Active low open drain I/O connected to LINK_B pin other SMT4504's for linked operation
LINK_A	I/O	9	Active low open drain I/O connected to LINK_A pin other SMT4504's for linked operation
GND	PWR	10	Ground of the part
$STATUS_A$	OUT	11	Active low open drain output. Asserted when the channel is tracking and between track off and track on.
$STATUS_B$	OUT	12	Active low open drain output. Asserted when the channel is tracking and between track off and track on.
$STATUS_C$	OUT	13	Active low open drain output. Asserted when the channel is tracking and between track off and track on.
$STATUS_D$	OUT	14	Active low open drain output. Asserted when the channel is tracking and between track off and track on.
SEATED#	IN	15	Active low input internally pulled up to VDD_CAP with 75k ohm resistor
FS#	I/O	16	Force shutdown active low I/O used to turn off all converter enable signals. Do not drive FS# high.
PWR_ON	I/O	17	Active high I/O signals the start of the power sequencing. When asserted the part will sequence the supplies on and when de-asserted the part will sequence the supplies off. Do not drive PWR_ON high.
VRLINK	I/O	18	External tracking ramp reference
SDA	DATA	25	Bi-directional I^2C Data line
SCL	CLK	26	I^2C Clock line
A0	IN	27	I^2C device bus address assignment pin.
A1	IN	28	I^2C device bus address assignment pin.
A2	IN	29	I^2C device bus address assignment pin.
WP	IN	30	Programmable active high/low write protect input. When asserted the configuration registers are write protected and the write protect volatile register is set.
MR#	IN	31	Active low input. When asserted the RST output will be allowed to de-assert after a reset timeout if there are no reset sources still active.
GND	PWR	34	Ground of the part
VDD	PWR	35	Power supply of the part

PIN DESCRIPTIONS (CONTINUED)

Pin Name	Type	Number	Function
VCTRL_SUP	PWR	37	Voltage supply input used for driving the $VCTRL_X$ outputs. Programmable for 5V, 8V or 12V.
VDD_CAP	CAP	38	External capacitor input used to filter the internal supply voltage
PUP_A	OUT	39	Programmable active high/low open drain converter enable output
PUP_B	OUT	40	Programmable active high/low open drain converter enable output
PUP_C	OUT	41	Programmable active high/low open drain converter enable output
PUP_D	OUT	42	Programmable active high/low open drain converter enable output
$VCTRL_A$	OUT	43	Control voltage used to track/sequence the converters
VM_A	IN	44	Channel A converter output or sense+ line
$VCTRL_B$	OUT	45	Control voltage used to track/sequence the converters
VM_B	IN	46	Channel B converter output or sense+ line
GND	PWR	47	Ground of the part
N/C	N/C	19-24, 32, 33, 36, 48	No Connect

PACKAGE AND PIN CONFIGURATION

48 LEAD TQFP



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to 125°C
Storage Temperature..... -65°C to 150°C
Terminal Voltage with Respect to GND:
VM_A, VM_B, VM_C, VM_D.....-0.3V to 6.0V
PUP_A, PUP_B, PUP_C, PUP_D 15V
All Others .....V_{DD} + 0.7V
Output Short Circuit Current 100mA
Lead Solder Temperature (10 secs)..... 300°C
Junction Temperature.....150°C
ESD Rating per JEDEC……..1000V
Latch-Up testing per JEDEC……±100mA

Stresses listed under Absolute Maximum Ratings may cause permanent to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Industrial).....–40°C to +85°C
(Commercial).....–5°C to +70°C

VDD Supply Voltage ..... 2.7V to 5.5V
12VIN Supply Voltage..... 8.0V to 15.0V
VIN ..... GND to VDD
VOUT ..... GND to 15.0V
Package Thermal Resistance (θ_{JA})
48 Lead TQFP……80°C/W

Moisture Classification Level 1 (MSL 1) per J-STD- 020

RELIABILITY CHARACTERISTICS
Data Retention……100 Years
Endurance……100,000 Cycles

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min.	Typ.	Max	Unit
VDD	Supply Voltage	3.3V aux supply	2.7		5.5	V
VCTRL_SUP	$VCTRL_X$ Supply Voltage		4.5		14	V
I_{DD}	Power Supply Current				TBD	mA
I_{GG}	Power Supply Current				TBD	mA
P_{VIT}	Programmable Threshold (VM_X Inputs)	X-bit resolution XXmV/bit	TBD		6.0	V
P_{VIT}	Programmable Threshold (VDD and VGG Inputs)	X-bit resolution XXmV/bit	TBD			V
PUP characteristics						
V_{OL}	Output Low Voltage	I_{SINK} = TBD	0		0.4	V
All other input and output characteristics						
V_{IH}	Input High Voltage (FS, PWR_ON/OFF, MR#)	VDD = 2.7V	0.9xVDD		VDD	V
		VDD = 5.0V	0.7xVDD		VDD	V
V_{IL}	Input Low Voltage (FS, PWR_ON, MR)	VDD = 2.7V	-0.1		0.1xVDD	V
		VDD = 5.0V	-0.1		0.3xVDD	V
V_{OL}	Programmable Open Drain Outputs (RST#, FS#, IRQ#)	I_{SINK} = TBD	0		0.4	V

PROGRAMMABLE AC SPECIFICATIONS

(Over recommended operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{DPON}	Programmable delay from PWR_ON to PUPs asserted and PUP to PUP delay		0.64		ms
			12.5		ms
			25		ms
			50		ms
$T_{TRACKER\_SLEW}$	Programmable internal tracking on/off slew rate		250		V/S
			500		V/S
			750		V/S
			1000		V/S
$T_{TRACKER\_SLEW}$	Programmable external tracking on/off slew rate step size (25V/S-250V/S)		25		V/S
t_{PRTO}	Programmable Reset Timeout Periods		0.64		mS
			50		mS
			100		mS
			200		mS
t_{ABORT}	Programmable Abort Power-On/Off Timer		OFF		
			100		ms
			200		ms
			400		ms

APPLICATIONS INFORMATION

SEQUENCING

The SMT4504 is a programmable controller for lossless (requires no pass MOSFETs) power supply sequencing/tracking. Up to four channels can be sequenced in any order with several delay options.

Before the SMT4504 begins the power-on sequencing, the UV sensors monitor the VDD and the VCTRL_SUP inputs. The power-on sequencing will not begin until both these inputs are above their UV threshold.

In order for a power supply to be sequenced it must first be enabled by a PUP output. This channel must also be programmed to participate in the sequence and be assigned a sequence position (one of 12). A sequence position is given to each channel as an order number in the sequence event. The sequence position assignments must begin at position 1 and must not skip positions. Also, multiple channels can be programmed into the same sequence position to enable voltage tracking of the supplies. Multiple corresponding channels sharing a common sequence position will have their voltages tracked during the power-on and power-off events only if each channel uses the $VCTRL_X$ pin on the converter. Otherwise the PUP output simply enables this power supply with no regard for closed loop voltage tracking.

Each channel selected for sequencing is given a power-on and power-off delay. The first power-on delay is a delay from assertion of the PWR_ON input to the assertion of all PUP outputs (sequence position 1). The power-off delay is the delay from the VM_X input of one channel turning off to the beginning of another VM_x output turning off. Tracking or sequencing down begins immediately when the PWR_ON pin is de-asserted.

Power-on sequencing can be initiated by asserting the PWR_ON/OFF input or by writing to the power-on bit of the command register. For automatic start-up the PWR_ON/OFF pin can be tied active. The power-on sequencing begins with the power-on delay time of the channel(s) in sequence position 1. Once this delay has timed out all PUP outputs assigned to this position will go active. At this point the supply connected to the VM input will begin to turn on via the action between the VCTRLX output and the supply's TRIM or other interface pin such as soft-start. When this supply reaches its programmed threshold (under-voltage) and the sequence delay timer is expired, the sequence position counter will change to position 1 and the power-on delay timer for the channel(s) in sequence position 2 will begin. This will repeat until all channels that were programmed for sequencing have turned on and are not in fault conditions. Power-on sequencing is considered complete when supplies assigned the last used sequence position go above their UV setting.

Power-off sequencing can be initiated by de-asserting the PWR_ON/OFF pin, by writing to the power-off bit of the command register, or triggered off of a selected fault condition. The SMT4504 is configured to sequence the supplies off in the reverse order of the power-on sequence. During the power-off sequence power-on commands as well as activity on the PWR_ON/OFF pin is ignored.

The power-off sequencing begins immediately with the channel(s) in the last sequence position of the power-on sequence (reverse order). Once the supplies in this sequence position have reached 100mV or less and the delay timer has timed out the PUP will turn off. At this point the supply connected to the next sequence position will begin to turn off. When this supply falls below the 100mV limit, the sequence position counter will change to the next position and the power-off delay timer for the channel(s) in current sequence position will begin.

This will repeat until all channels that were programmed for sequencing have turned off. At this point the SMT4504 will monitor the VDD and VCTRL_SUP inputs as precursor conditions to power-on sequencing.

During sequencing an abort timer is available. The abort timer starts each time a PUP output goes active. If the abort timer times out before the VM_X input goes out of fault, all channels are shut down and the abort bit is set in the status register. This is to avoid the case where one or more channels are not capable of reaching their minimum level. The abort timer is available for sequence up and sequence down. If the abort timer shuts the sequencing down the PWR_ON/OFF pin must be toggled to re-start. The timeout period of the abort timer is programmable.

APPLICATIONS INFORMATION (CONTINUED)

MONITORING

Once the power-on sequence is underway, the SMT4504 monitors VM_X inputs and the VDD and VCTRL_SUP supply voltages. The SMT4504 compares the voltages with the programmable low and high limits (UV/OV). Each of these limits can be programmed to trigger the RST, IRQ# or HEALTHY input as well as a force shutdown or power-off operation if exceeded.

FORCED SHUTDOWN

The Forced Shutdown function is used to immediately turn off all PUP outputs when there is not enough time to perform a power-off sequence. Forced Shutdown can be initiated by asserting the FS pin, by writing to the forced shutdown bit of the command register, or triggered by one or more channels going out of limits. Forced Shutdown cannot be triggered by a channel going out of limit until the power-on sequence has completed. Forced Shutdown will latch the PUP outputs in the off state until the FS pin is de-asserted and the PWR_ON pin is toggled. Input on the PWR_ON pin will be ignored until all supplies are below their OFF thresholds.

COMMUNICATING WITH THE SMT4504

All communication with the SMT4504 takes place over the I^2C bus. The part has several registers that contain information about the channels that are being controlled and the set point and limit information. The slave address for the configuration registers and the 4-k of memory is programmable. When accessing the configuration registers, [A1, A0] is used as the bus address. Write protection for the SMT4504 is located in a volatile register where the power-on state is defaulted to write protect.

SUMMARY OF DEVICE OPERATION

When the SMT4504 first receives power it will hold all PUP outputs and the HEALTHY output in their inactive state. The RST output will be held active. At this point, the $VCTRL_X$ outputs will be turned on to their respective programmed voltages. The device will then monitor the VDD and VCTRL_SUP inputs until both are in the appropriate range.

Once the PWR_ON/OFF signal goes active and the VDD and VCTRL_SUP input is within range, the PUP outputs of all channels in sequence position 1 will go active and the device will monitor those converter outputs. Once those converter outputs have gone above the UV settings, the PUP outputs of the channels in sequence position 2 will go active.

As the channels are powering on, the device will monitor the VDD and VCTRL_SUP inputs. The HEALTHY output will go active when all trigger sources are within their programmed limits. The RST output will go inactive a programmable timeout period after all trigger sources are within their programmed limits and the MR signal has gone inactive.

During the power-on sequence an abort timer will start as each PUP output goes active. The channel that is associated with that PUP must reach its lower limit before the abort timer expires. If it does not then all channels are shut down and the Abort Timer bit is set in Status Register1.

Once the power-on sequence is complete, the device will monitor all. The result of each monitor conversion will be compared against the preset high and low limits for that channel. If a voltage channel is found to be out of limits then HEALTHY will be de-asserted. In either case the UV/OV sensors will continue to monitor all channels. When the problem channel is back in limits the HEALTHY will be asserted again. The number of sequential conversions that must be completed in order to declare in or out of limit is set in Configuration Register 1. The state of the channels can be checked by reading the status registers.

When the PWR_ON/OFF pin is de-asserted the device will begin a power-off operation. First, HEALTHY will go inactive. Then the SMT4504 will de-assert the last $VCTRL_X$ (or PUP) output and monitor the corresponding voltage output. When the output has dropped below the “off” limit for a programmed number of consecutive conversions the next $VCTRL_X$ (or PUP) outputs will be de-asserted in the reverse sequence order as power-on (3-0). A power-off operation can also be initiated by a fault condition on any of the channels. During the power-off sequencing the abort timer is again used to ensure that the sequencing takes place properly. If the abort timer finishes before a channel drops below the off level, all channels will be shut down and the Abort Timer bit is set in Status Register 1.

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I2C serial bus format so that it can be directly downloaded to the SMT4504 via the programming Dongle and cable. An example of the connection interface is shown in Figure 4.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

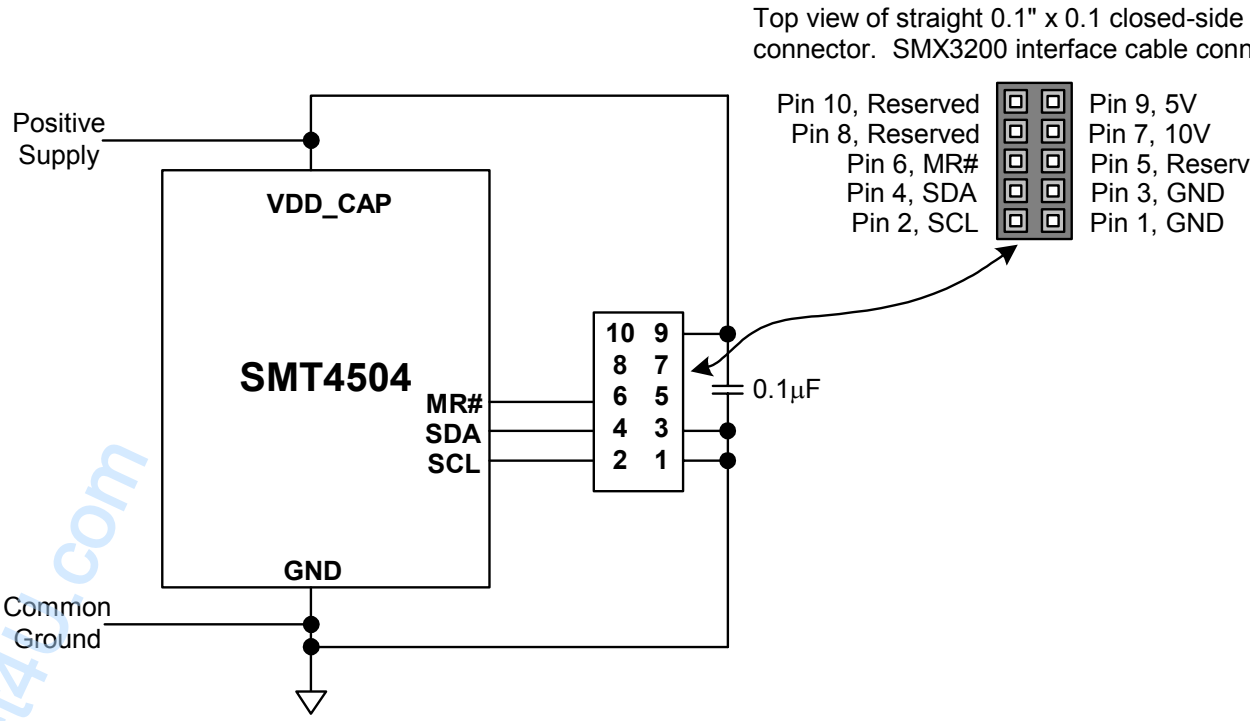


Figure 4 – SMX3200 Programmer I2C serial bus connections to program the SMT4504.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 4-bit device type identifier (slave address) and a 3-bit bus address. The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMM665.

The device type identifier for the memory array is generally set to 1010_{BIN} following the industry standard for a typical nonvolatile memory. There is an option to change the identifier to 1011_{BIN} allowing it to be used on a bus that may be occupied by other memory devices. The configuration registers are grouped with the memory array and thus use 1010_{BIN} or 1011_{BIN} as the device type identifier. The command and status registers as well as the 10-bit ADC are accessible with the separate device type identifier of 1001_{BIN}.

The bus address bits A[1:0] are programmed into the configuration registers. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin. The bus address accessed in the address byte of the serial data stream must match the setting in the SMM665 and on the A2 pin.

Any access to the SMM665 on the I2C bus will temporarily halt the monitoring function. This is true not only during the monitor mode, but also during Power-on and Power-off sequencing when the device is monitoring the channels to determine if they have turned on or turned off.

The SMM665 halts the monitor function from when it acknowledges the address byte until a valid stop is received.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 8, 9, 11, 13 and 14. A Start condition followed by the address byte is provided by the host; the SMM665 responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMM665 responds with an acknowledge; the host then clocks in on byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page. After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the configuration registers, memory, command and status registers and ADC registers must be set before data can be read from the SMM665. This is accomplished by a issuing a dummy write command, which is simply a write command that is not followed by a Stop condition. The dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figures 10, 12 and 15 for an illustration of the read sequence.

I²C PROGRAMMING INFORMATION (CONTINUED)

The SMM665 powers up into a write protected mode. Writing a code to the volatile write protection register can disable the write protection. The write protection register is located at address 87_{HEX} of slave address 1001_{BIN}.

Writing 0101_{BIN} to bits [7:4] of the write protection register allow writes to the general-purpose memory while writing 0101_{BIN} to bits [3:0] allow writes to the configuration registers. The write protection can re-enable by writing other codes (not 0101_{BIN}) to the write protection register. Writing to the write protection register is shown in Figure 7.

CONFIGURATION REGISTERS

The majority of the configuration registers are grouped with the general-purpose memory located at either slave address 1010_{BIN} or 1011_{BIN}. The bus address bits, A[1:0], used to differentiate the general-purpose memory from the configuration registers are set to 11_{BIN}. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin.

Two additional configuration registers are located at addresses 83_{HEX} and 84_{HEX} of slave address 1001_{BIN}.

Writing and reading the configuration registers is shown in Figures 8, 9, 10,11 and 12.

Note: Configuration writes or reads of registers 00_{HEX} to $0F_{HEX}$ should not be performed while the SMM665 is margining.

GENERAL-PURPOSE MEMORY

The 4k-bit general-purpose memory is located at either slave address 1010_{BIN} or 1011_{BIN}. The bus address bits, A[1:0], used to differentiate the general-purpose memory from the configuration registers are set to 00_{BIN} for the first 2k-bits and 01_{BIN} for the second 2k-bits. Bus address bit A[2] can be programmed as either 0 or biased by the A2 pin.

Figures 13, 14 and 15.

COMMAND AND STATUS REGISTERS

The command and status registers are located at slave address 1001_{BIN}. Writes and reads of the command and status registers are shown in Figures 16 and 17.

ADC CONVERSIONS

An ADC conversion on any monitored channel can be performed and read over the I²C bus using the ADC read command. The ADC read command, shown in Figure 18, starts with a dummy write to the 1001_{BIN} slave address. Bits [6:3] of the word address byte are used to address the desired monitored input. Once the device acknowledges the channel address, it begins the ADC conversion of the addressed input. This conversion requires 70µs to complete. During this conversion time, acknowledge polling can be used. The SMM665 will not acknowledge the address bytes until the conversion is complete. When the conversion has completed, the SMM665 will acknowledge the address byte and return the 10-bit conversion along with a 4-bit channel address echo.

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMM665 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet and Application Note 33, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMM665. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I²C bus protocol.

Slave Address	Bus Address	Register Type
1001_{BIN}	A2 A1 A0	Write Protection Register, Command and Status Registers, Two Configuration Registers, ADC Conversion Readout
1010_{BIN} or 1011_{BIN}	A2 0 0	1st 2-k Bits of General-Purpose Memory
	A2 0 1	2nd 2-k Bits of General-Purpose Memory
	A2 1 1	Configuration Registers

Table 1 - Address bytes used by the SMM665.

I²C PROGRAMMING INFORMATION (CONTINUED)

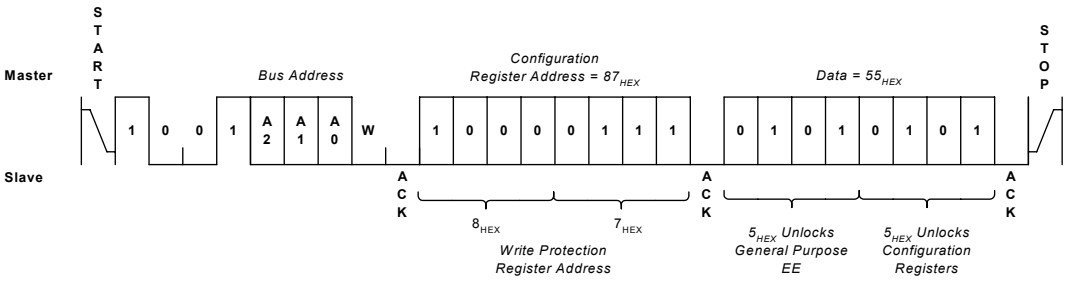


Figure 7 – Write Protection Register Write

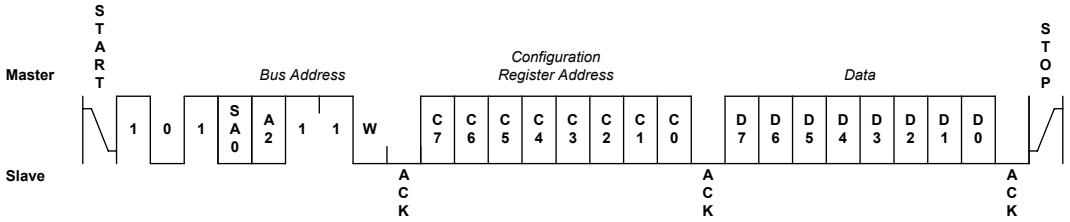


Figure 8 – Configuration Register Byte Write

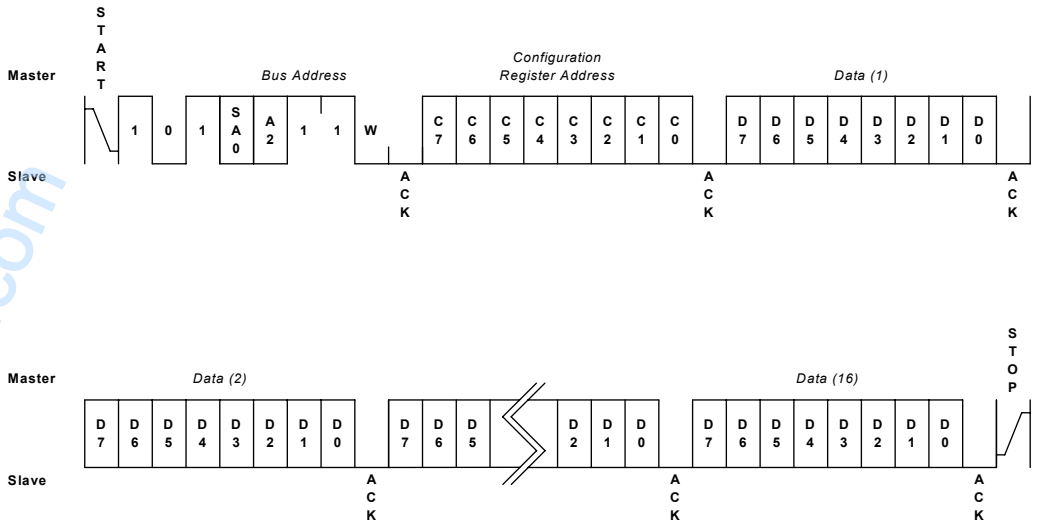


Figure 9 – Configuration Register Page Write

I²C PROGRAMMING INFORMATION (CONTINUED)

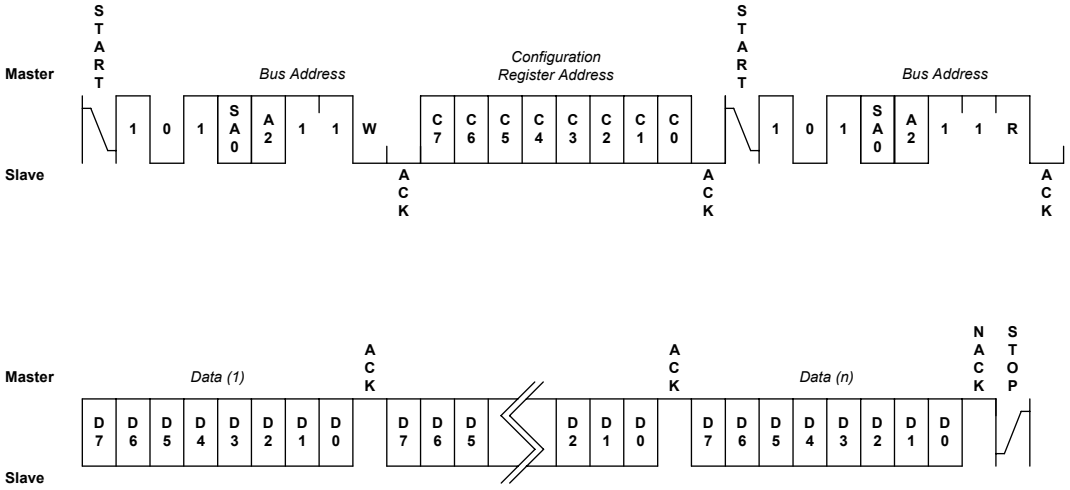


Figure 10 - Configuration Register Read

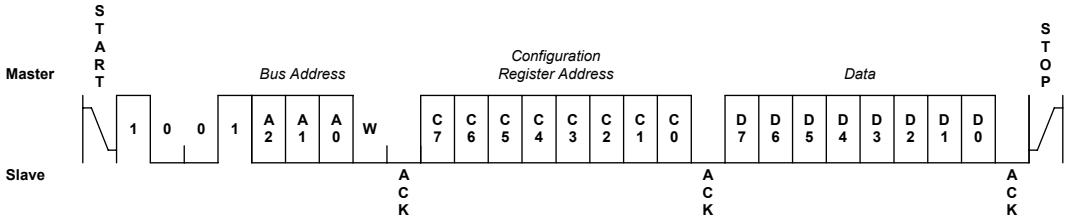


Figure 11 - Configuration Register with Slave Address 1001_{BIN} Write

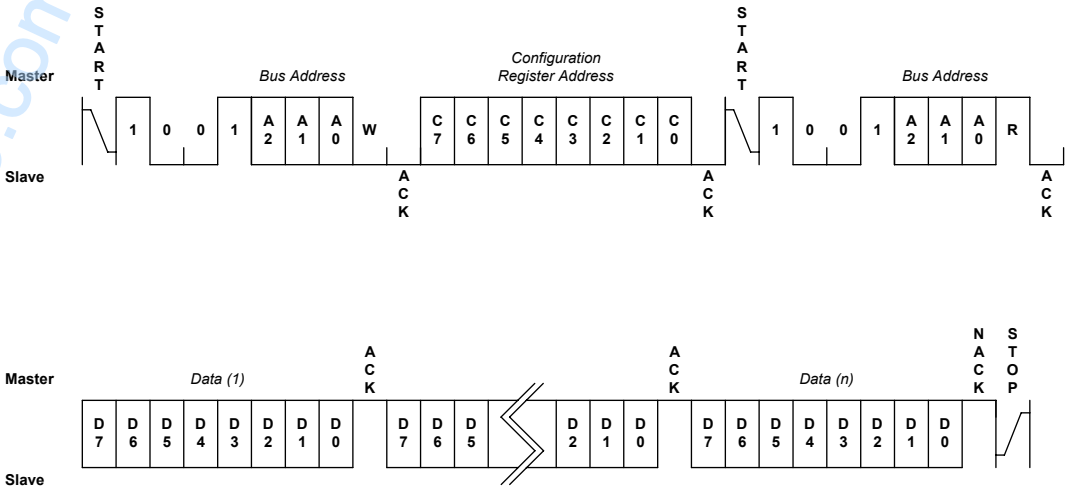


Figure 12 - Configuration Register with Slave Address 1001_{BIN} Read

I²C PROGRAMMING INFORMATION (CONTINUED)

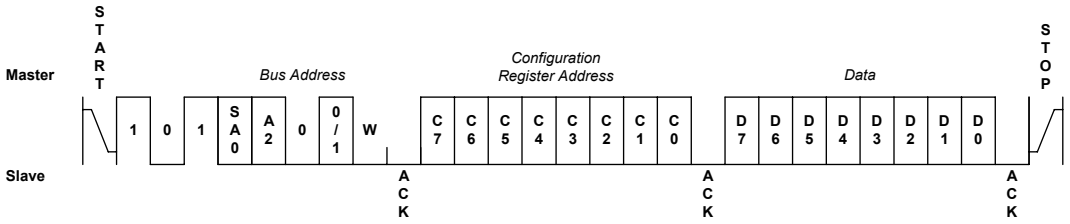


Figure 13 – General Purpose Memory Byte Write

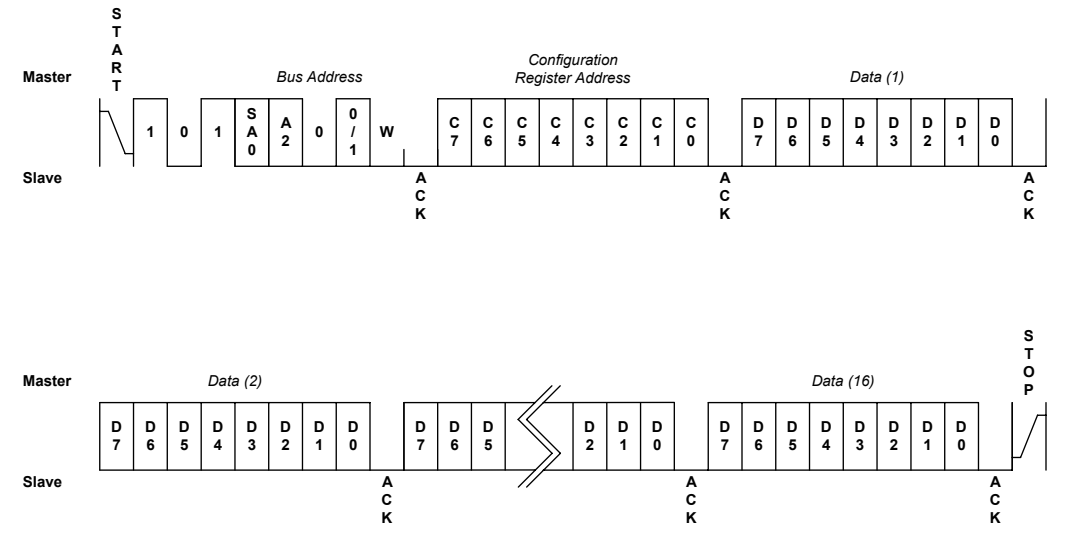


Figure 14 - General Purpose Memory Page Write

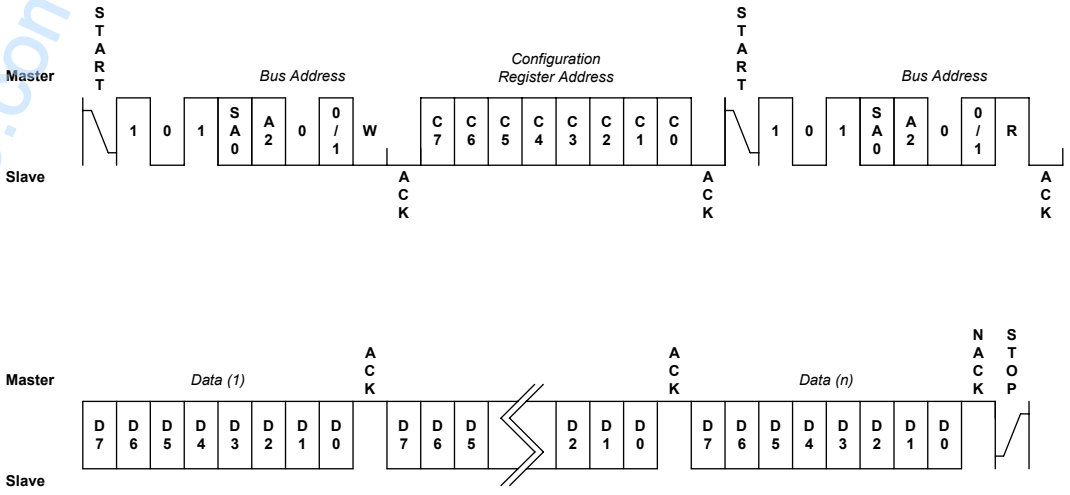


Figure 15 - General Purpose Memory Read

I²C PROGRAMMING INFORMATION (CONTINUED)

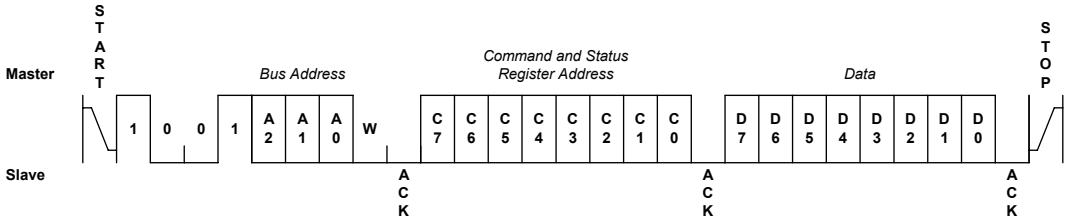
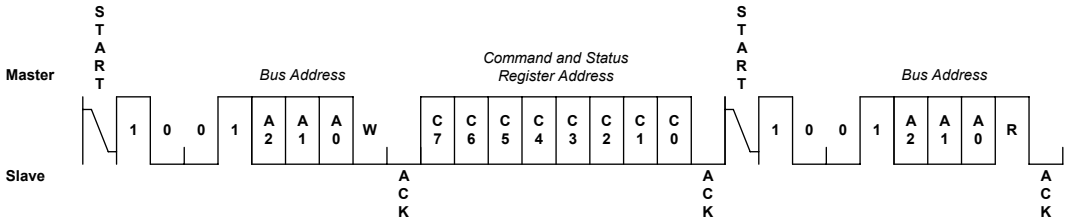


Figure 16 – Command and Status Register Write



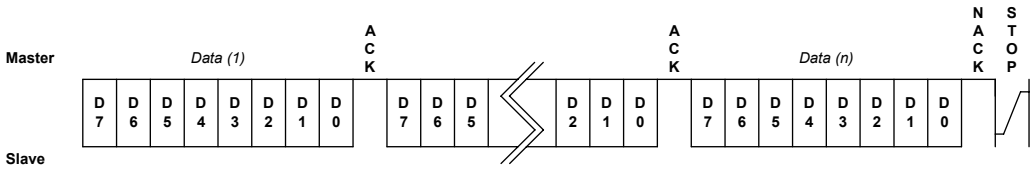


Figure 17 - Command and Status Register Read

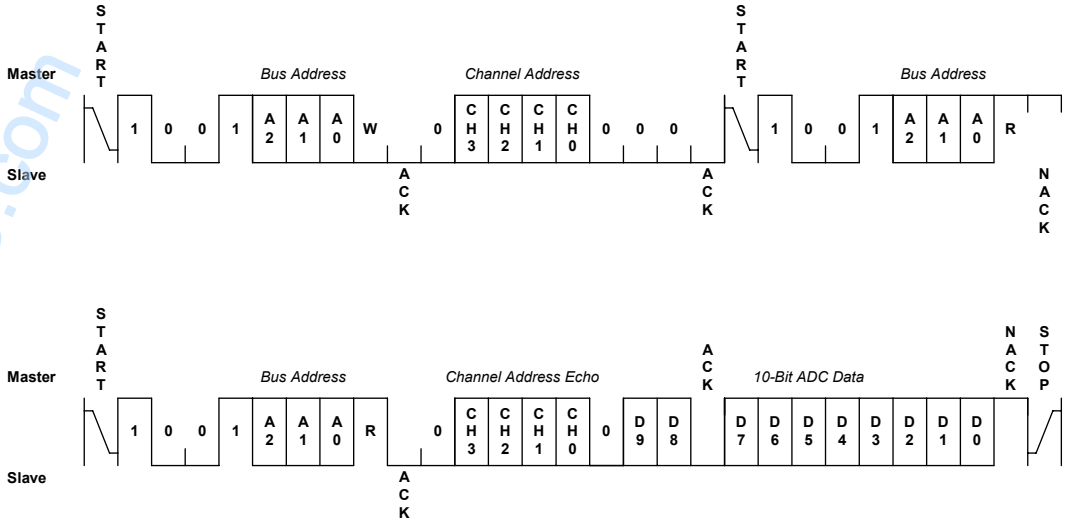


Figure 18 – ADC Conversion Read

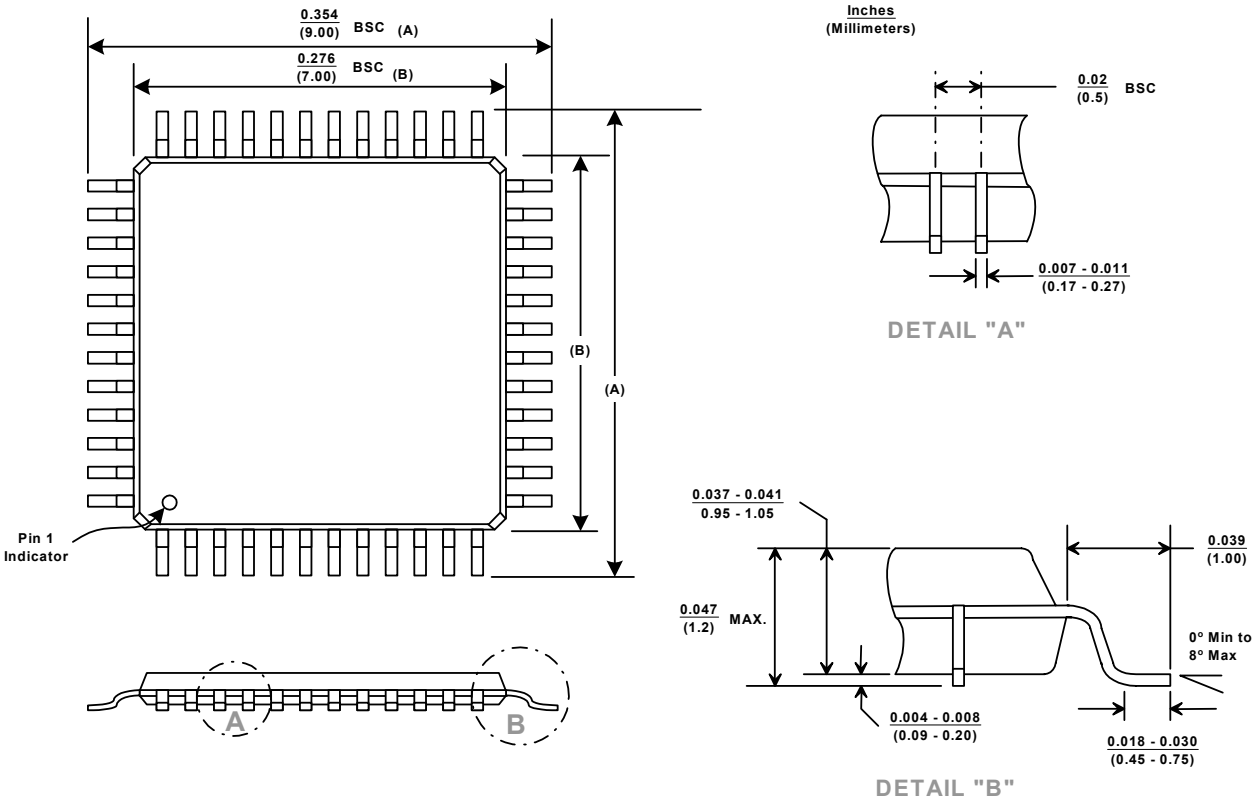
DEFAULT CONFIGURATION REGISTER SETTINGS – SMT4504-172

Register	Contents	Register	Contents	Register	Contents	Register	Contents
R0	0D	R42	0E	R9C	29	RC5	90
R1	83	R43	39	R9D	9A	RC6	09
R2	0D	R44	0E	R9E	11	RC7	90
R3	FF	R45	A4	R9F	AE	RC8	0C
R4	0E	R46	0F	RA0	41	RC9	00
R5	61	R47	16	RA1	0B	RCA	0C
R6	0E	R48	0F	RA2	80	RCB	00
R7	C7	R49	B4	RA3	F6	RCC	0F
R8	0F	R4A	06	RA4	29	RCD	FF
R9	54	R4B	7F	RA5	5D	RCE	0F
RA	0B	R4C	00	RA6	11	RCF	FF
RB	22	R4D	12	RA7	71	RD0	0C
RC	7F	R4E	48	RA8	40	RD1	00
RD	3F	R80	42	RA9	CE	RD2	0C
RE	03	R81	48	RAA	80	RD3	00
RF	01	R82	82	RAB	8F	RD4	0F
R10	8F	R83	3E	RAC	29	RD5	D8
R11	9F	R84	2A	RAD	1F	RD6	0F
R12	AF	R85	B8	RAE	11	RD7	D8
R13	BF	R86	12	RAF	33	RE0	00
R14	CF	R87	F6	RB0	2A	RE1	3D
R15	DF	R88	41	RB1	67	RE2	00
R18	00	R89	C8	RB2	0A	RE3	3D
R19	00	R8A	81	RB3	52	RE4	00
R30	0D	R8B	B9	RB4	03	RE5	3D
R31	60	R8C	2A	RB5	FF	RE6	00
R32	0D	R8D	34	RB6	03	RE7	3D
R33	DC	R8E	12	RB7	FF	RE8	00
R34	0E	R8F	49	RB8	0D	RE9	3D
R35	45	R90	49	RB9	9A	REA	00
R36	0E	R91	5C	RBA	0D	REB	3D
R37	A2	R92	81	RBB	56		
R38	0F	R93	52	RBC	0F		
R39	08	R94	29	RBD	E0		
R3A	0F	R95	D7	RBE	0F		
R3B	D6	R96	11	RBF	E0		
R3C	00	R97	EB	RC0	0B		
R3D	12	R98	41	RC1	38		
R3E	48	R99	3E	RC2	0B		
R40	0D	R9A	81	RC3	38		
R41	B9	R9B	33	RC4	09		

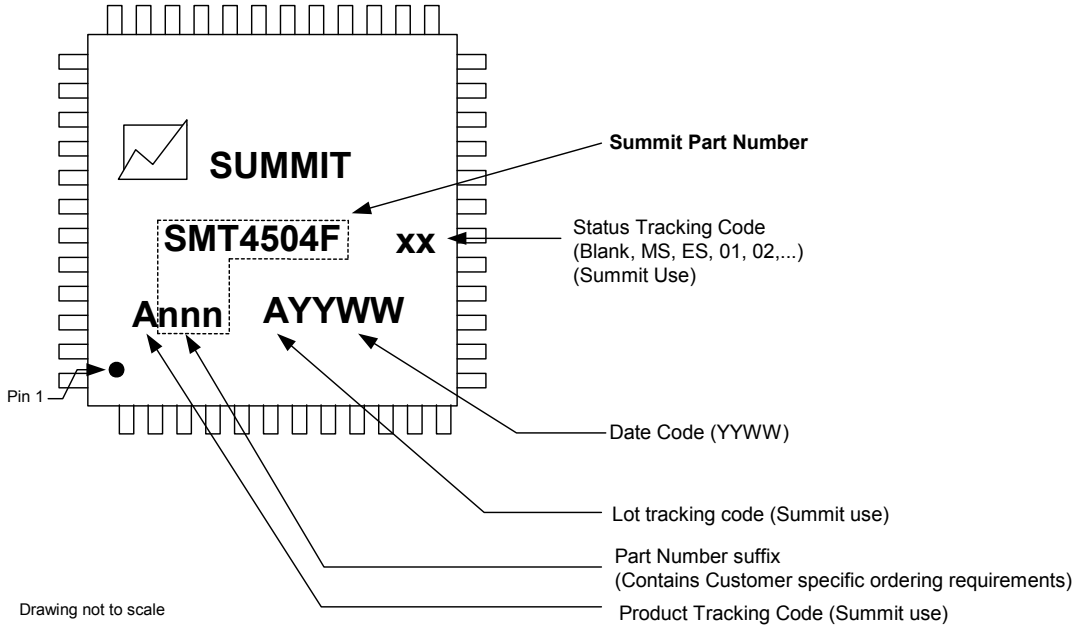
The default device ordering number is SMT4504F-172, is programmed as described above and tested over the commercial temperature range. Application Note 33 contains a complete description of the Windows GUI and the default settings of each of the 154 individual Configuration Registers.

PACKAGES

48 PIN TQFP PACKAGE



PART MARKING



ORDERING INFORMATION

SMT4504 F nnn

Summit Part Number

Package
F=48 Lead TQFP

Part Number Suffix (see page 18)
Specific requirements are contained in the suffix such as Commercial or Industrial Temp Range, Hex code, Hex code revision, etc.