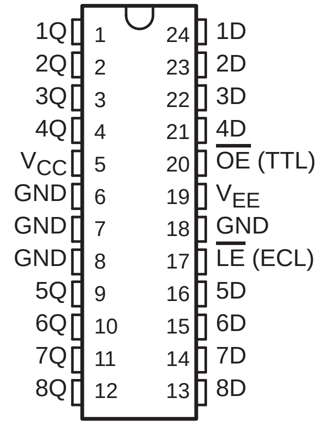
SN10KHT5573 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE TRANSPARENT LATCHES AND 3-STATE OUTPUTS

- **10KH Compatible**
- **ECL and TTL Control Inputs**
- **Noninverting Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE (T0P VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight latches of the SN10KHT5573 are transparent D-type latches. While latch enable ($\overline{LE}$) is low, the Q outputs follow the data (D) inputs. When $\overline{LE}$ is high, the Q outputs are latched at the levels that were set up at the D inputs.

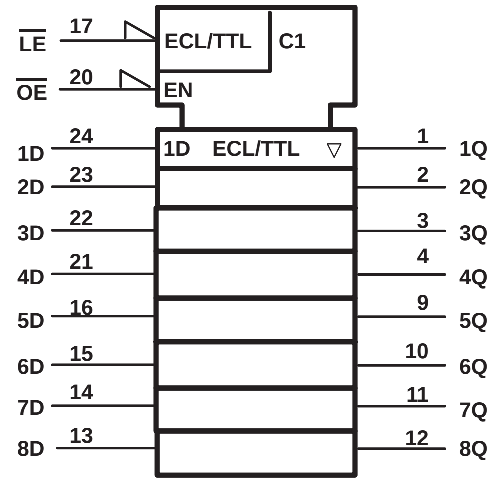
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components. Output-enable $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5573 is characterized for operation from 0° to 75°C.

FUNCTION TABLE

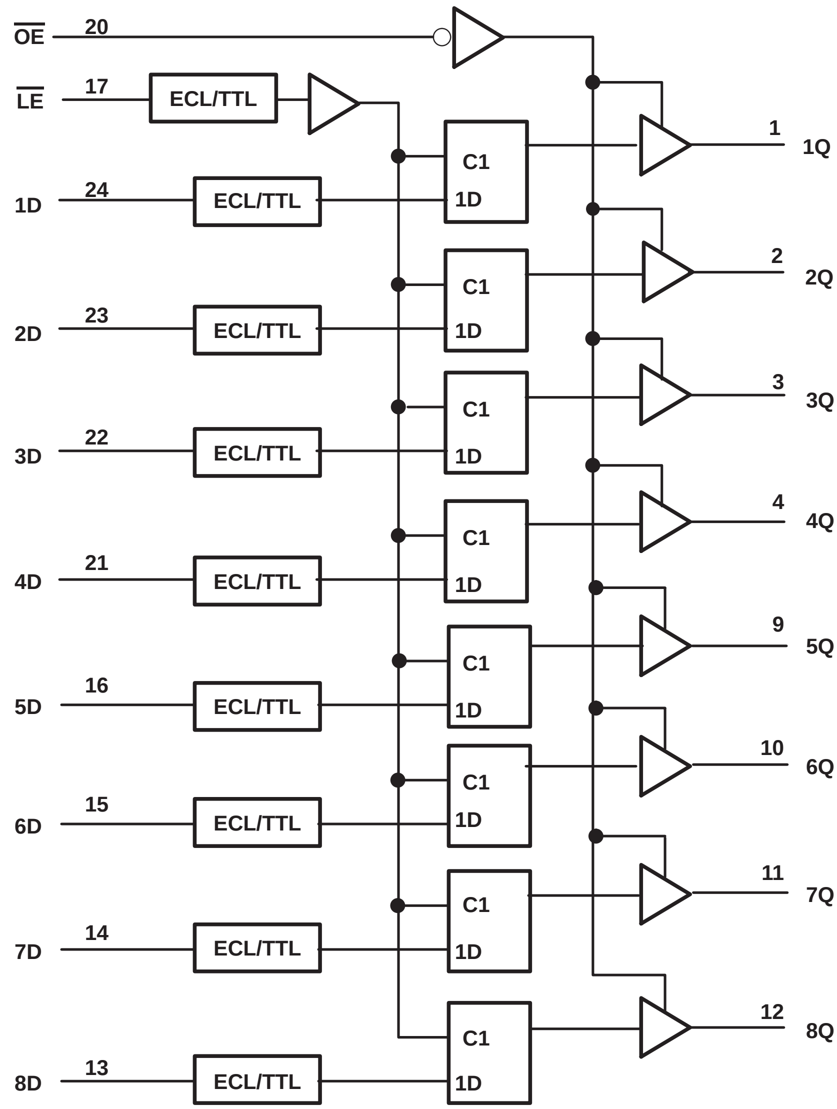
OUTPUT CONTROL		DATA INPUT	OUTPUT (TTL)
$\overline{OE}$	$\overline{LE}$	D	Q
L	L	L	L
L	L	H	H
L	H	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Supply voltage range, V_{EE} . . . . −8 V to 0 V
Input voltage range, TTL (see Note 1) . . . . −1.2 V to 7 V
Input voltage range, ECL . . . . V_{EE} to 0 V
Input current range, TTL . . . . −30 mA to 5 mA
Current into any output in the low state . . . . 96 mA
Voltage applied to any output in the disabled or power-off state . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . −0.5 V to V_{CC}
Operating free-air temperature range . . . . 0°C to 75°C
Storage temperature range . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
I_{IK}	TTL input clamp current				−18	mA
V_{IH}	ECL high-level input voltage (see Note 2)	0°C	−1170		−840	mV
		25°C	−1130		−810	
		75°C	−1070		−735	
V_{IL}	ECL low-level input voltage (see Note 2)	0°C	−1950		−1480	mV
		25°C	−1950		−1480	
		75°C	−1950		−1450	
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature		0		75	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}$ only	V_{CC} = 4.5 V, V_{EE} = −4.94 V, I_I = −18 mA				−1.2	V
I_I	$\overline{OE}$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 2.7 V				20	µA
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = 0.5 V				−0.5	mA
I_{IH}	Data inputs and $\overline{LE}$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −840 V	0°C			350	µA
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −810 V	25°C			350	
		V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −735 V	75°C			350	
I_{IL}	Data inputs and $\overline{LE}$	V_{CC} = 5.5 V, V_{EE} = −5.46 V, V_I = −1950 V	0°C	0.5			µA
			25°C	0.5			
			75°C	0.5			
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −3 mA, V_{EE} = −5.2 V ± 5%		2.4	3.3		V
		V_{CC} = 4.5 V, I_{OH} = −15 mA, V_{EE} = −5.2 V ± 5%		2	3.1		
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 48 mA, V_{EE} = −5.2 V ± 5%			0.38	0.55	V
I_{OZH}		V_{CC} = 5.5 V, V_O = 2.7 V, V_{EE} = −5.46 V				50	µA
I_{OZL}		V_{CC} = 5.5 V, V_O = 0.5 V, V_{EE} = −5.46 V				−50	µA
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0 V, V_{EE} = −5.46 V		−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			62	89	mA
I_{CCL}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			78	111	mA
I_{CCZ}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			75	108	mA
I_{EE}		V_{CC} = 5.5 V, V_{EE} = −5.46 V			−34	−48	mA
C_i		V_{CC} = 5 V, V_{EE} = −5.2 V			5		pF
C_o		V_{CC} = 5 V, V_{EE} = −5.2 V			7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, and T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements

		V_{CC} = 4.5 V to 5.5 V, V_{EE} = −4.94 V to −5.46 V, T_A = MIN to MAX§		UNIT
		MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ high	4		ns
t_{su}	Setup time, data before $\overline{LE}$↓	1		ns
t_h	Hold time, data after $\overline{LE}$↓	1		ns

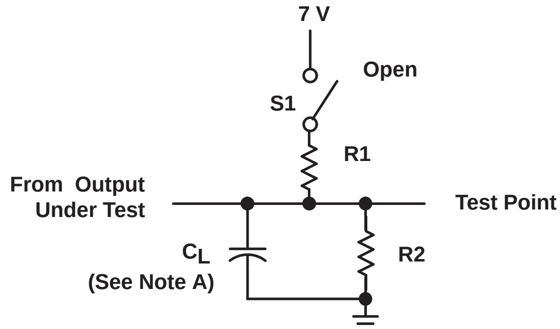
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			MIN	TYP†	MAX	
t_{PLH}	D	Q	1.9	3.9	6.4	ns
t_{PHL}			2.3	4.2	6.8	
t_{PLH}	$\overline{LE}$	Q	2.2	4	6.7	ns
t_{PHL}			2.6	4.5	7.2	
t_{PZH}	$\overline{OE}$	Q	1.1	3.2	5.9	ns
t_{PZL}			2.3	4.6	7.8	
t_{PHZ}	$\overline{OE}$	Q	1.8	4	5.9	ns
t_{PLZ}			0.6	3.4	6.5	

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, and T_A = 25°C.

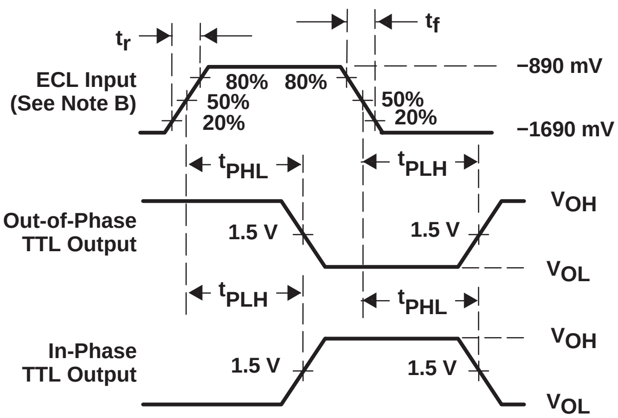
PARAMETER MEASUREMENT INFORMATION



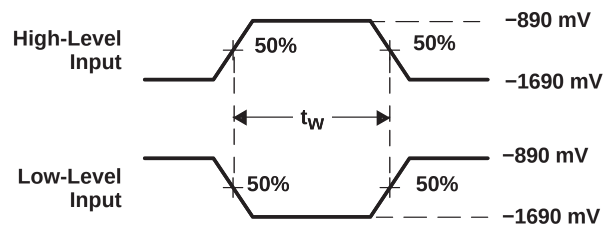
LOAD CIRCUIT

SWITCH POSITION TABLE

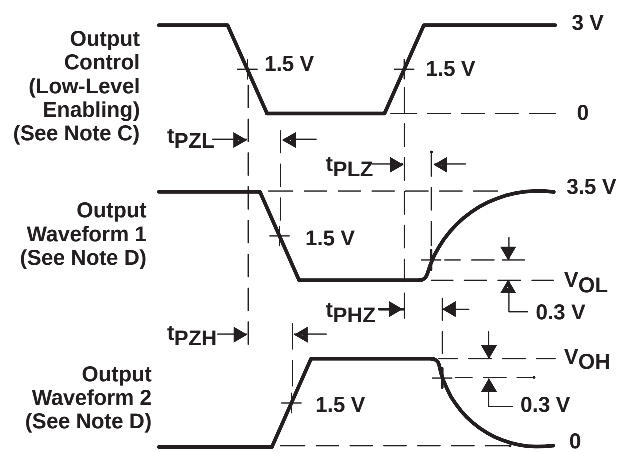
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



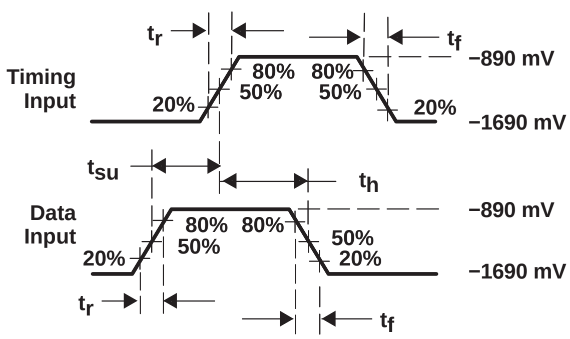
VOLTAGE WAVEFORMS
ECL-INPUT PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
TTL ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 1.5 ns.
C. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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