



SN1113 spec

SN1113

USB AUDIO CONTROLLER

Data Sheet

2003 March 5th, Version 1.01



I. Description

SONiX SN1113 is an USB audio controller. It supports 32KHz, 44.1KHz and 48KHz sampling rate in digital playback and recording; 44.1KHz and 48 KHz sampling rate in analog audio playback and recording.

In digital playback mode, it receives audio stream from PC via USB interface and transmits audio data according to the AES/EBU, IEC60958, S/PDIF consumer interface standards. In analog playback mode, it supports AC 97 Codec for analog playback.

In digital recording mode, it receives S/PDIF digital audio input and sends back to PC through USB. Three sampling rates; includes 32 KHz, 44.1 KHz, and 48 KHz; are automatically locked internally. In analog recording mode, 44.1KHz and 48 KHz sampling rate are supported by analog audio recording.

Totally one control pipe, two isochronous pipes, and one interrupt pipe are supported by SN1113.

II. Features

- Supports AES/EBU, IEC60958, S/PDIF consumer formats for stereo PCM data
- 32K, 44.1K and 48KHz sampling rate for 2 channel playback in digital mode
- Conveys AC-3 data stream by S/PDIF output
- 44.1K and 48KHz sampling rate for 2 channel playback in analog mode
- Supports digital recording function with 32KHz, 44.1KHz and 48KHz sampling rate
- Supports analog recording function with 44.1KHz and 48KHz sampling rate
- Supports SCMS (Serial Copy Management System) copy protection
- Full-duplex playback/ recording audio stream without sound card in PC
- Compatible with Win98 SE/ WinME/ Win2000/ WinXP and MacOS 9.2.1 / MacOS10.1 without additional driver
- Plug-and-Play operation with Microsoft OS or MacOS default drivers
- Compliant with USB specification v1.1
- Compliant with USB audio device class specification v1.0
- Supports USB full speed 12Mbits/s serial data transmission
- USB bus powered operation
- Supports suspend/resume and remote wake-up
- 6MHz crystal input with on-chip PLL and embedded transceiver for USB



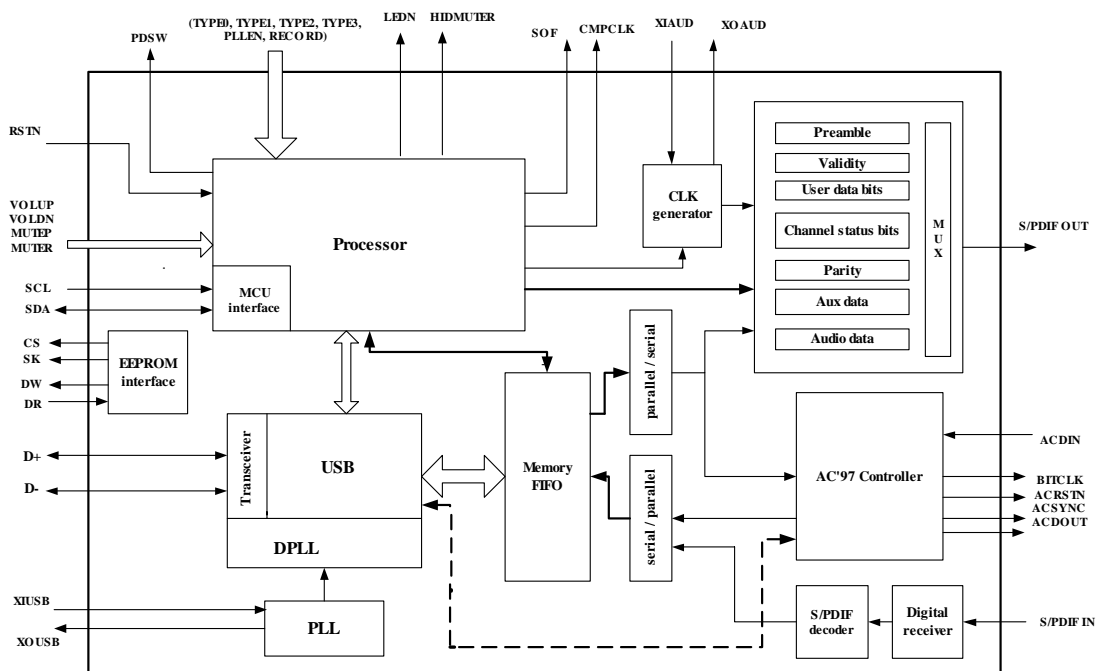
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- USB audio function topology has four input terminals, three output terminals, one selector unit, one mixer unit, and six feature units
- Alternate setting0 is a zero-bandwidth setting; used to release the claimed bandwidth on the bus when this device is inactive
- Isochronous transfer uses adaptive, synchronous and asynchronous synchronization
- Supports AC'97 component specification v2.1 and v2.2; AC link interface for external AC97 audio Codec
- Compliant with USB HID class specification v1.1; pin control for volume up / down, play mute, and record mute
- Supports two wire series bus interface; slave only interface with transfer speed up to 400Kbps(Fast-mode)
- EEPROM interface for customized USB IDs and Codec programming
- 3.3 V core operation and 5 V tolerant I/O
- Available in 64-pin LQFP(10x10 mm)
- System on chip solution: low cost and easy implementation without external memory
- LED indicator pins for playback and recording mute
- Features programmable by jumper pins

III. Ordering information

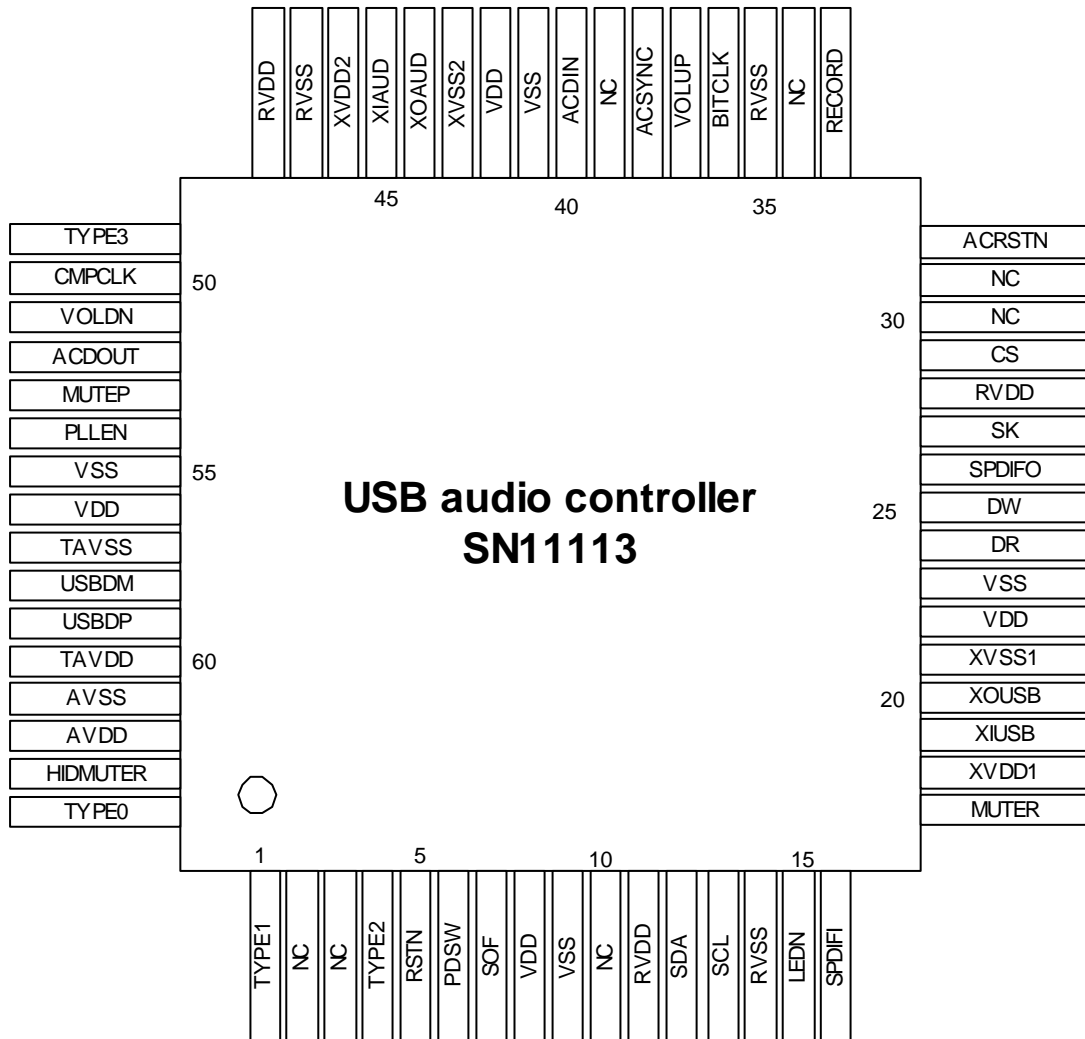
SN1113F : 64-pin LQFP (10x10x1.4 mm)

IV. Block diagram



V. Pin description

5.1 SN1113 pin chart (64-pin LQFP)



5.2 pin assignment and description (64-pin LQFP)

Pin No.	Pin Name	Pin Type	Description
1	TYPE1	I, ST	Product type setting pin1
2	NC		
3	NC		



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4	TYPE2	I, ST	Product type setting pin2
5	RSTN	I, ST, PU	System reset pin, pull low to reset
6	PDSW	O, 4mA, SR	Power down switch control -- 0: normal mode, 1: power down mode
7	SOF	O, 4mA, SR	USB SOF (Start of Frame) pin provides 1KHz signal
8	VDD	P	Power pin
9	VSS	P	Power pin
10	NC		
11	RVDD	P	Power pin for pad
12	SDA	I/O, 4mA, SR	IIC data pin for external MCU control
13	SCL	I, ST	IIC clock pin for external MCU control
14	RVSS	P	Power pin for pad
15	LEDN	O, 8mA, SR	LED indicator pin, output low after power on reset, toggle during operation
16	SPDIFI	I, ST	Input pin for SPDIF signal
17	MUTER	I, ST	Recording mute, edge trigger with 64ms de-bouncing circuit
18	XVDD1	P	Power pin for USB external crystal
19	XIUSB	I	6 MHz clock osc pin for USB PLL
20	XOUSB	O	6 MHz clock osc pin for USB PLL
21	XVSS1	P	Power pin for USB external crystal
22	VDD	P	Power pin
23	VSS	P	Power pin
24	DR	I, ST	EEPROM data input Fixing this pin to H or L sets USB vendor ID to SONiX USB vendor ID (hex 0C45); PU or PD is used for different product ID
25	DW	O, 4mA, SR	EEPROM data output
26	SPDIFO	O, 8mA, SR	SPDIF data output
27	SK	O, 4mA, SR	EEPROM clock pin
28	RVDD	P	Power pin for pad
29	CS	O, 4mA, SR	EEPROM chip select
30	NC		
31	NC		
32	ACRSTN	O, 4mA, SR	AC'97 Codec reset
33	RECORD	I, ST	Recording function enable (=1)
34	NC		
35	RVSS	P	Power pin for pad
36	BITCLK	O, 8mA, SR	AC'97 serial data clock
37	VOLUP	I, ST	Volume up control, edge trigger with 64ms de-bouncing circuit
38	ACSYNC	O, 4mA, SR	AC'97 Codec sync (48 kHz) signal
39	NC		
40	ACDIN	I, ST	AC'97 Codec serial data input
41	VSS	P	Power pin
42	VDD	P	Power pin
43	XVSS2	P	Power pin for external crystal
44	XOAUD	O	12.288 MHz Crystal output
45	XIAUD	I, ST	12.288 MHz Crystal input / connected to PLL VCO output
46	XVDD2	P	Power pin for external crystal
47	RVSS	P	Power pin for pad
48	RVDD	P	Power pin for pad
49	TYPE3	I, ST	Product type setting pin3



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50	CMPCLK	O, 4mA, SR	PLL comparator input
51	VOLDN	I, ST	Volume down control, edge trigger with 64ms de-bouncing circuit
52	ACDOUT	O, 4mA, SR	AC'97 Codec serial data
53	MUTE _P	I, ST	Playback mute control pin, edge trigger with 64ms de-bouncing circuit
54	PLEN	I, ST	Use PLL (=1) or Crystal at XIAUD pin
55	VSS	P	Power pin
56	VDD	P	Power pin
57	TAVSS	P	Power pin for USB transceiver
58	USBDM	I/O	USB data minus
59	USBDP	I/O	USB data plus
60	TAVDD	P	Power pin for USB transceiver
61	AVSS	P	Power pin for PLL
62	AVDD	P	Power pin for PLL
63	HIDMUTER	O, 8mA, SR	Playback mute led indicator
64	TYPE0	I, ST	Product type setting pin0

** All input pin are 5 volt tolerance, TTL level and Schmitt trigger

All output pins are slew rate control

I – input pin , O – output pin, P – power pin, ST – Schmitt trigger, SR – slew rate control,
PU/PD – pull up or pull down

VI. Operating rating and electrical characteristics

6.1 Absolute maximum rating

symbol	Parameter	value	unit
Dvmin	min digital supply voltage	DGND – 0.3	V
Dvmax	max digital supply voltage	DGND + 4.6	V
Avmin	min analog supply voltage	AGND – 0.3	V
Avmax	max analog supply voltage	AGND + 4.6	V
Dvinout	voltage on any digital input or output pin	DGND –0.3 to 5.5	V
Avinout	voltage on any analog input or output pin	AGND –0.3 to Avdd + 0.3	V
T _{stg}	storage temperature range	-40 to +125	°C
ESD (HBM)	ESD human body mode C=100pF, R=1.5KΩ	5000	V
ESD (MM)	ESD machine mode	200	V
I _{off}	Leakage current	10	uA
I _{latch}	minimum latch up current	100	mA

6.2 Operation conditions

symbol	Parameter	value	unit
DVdd	digital supply voltage	+3 to +3.6	V
Avdd	analog supply voltage	+3 to +3.6	V
T _A	operating ambient temperature range	0 to 70	°C
T _J	operating junction temperature range	0 to 115	°C

6.3 DC electrical characteristics

symbol	parameter	test condition	Value	unit
V _{DI}	differential input sensitivity	(D+) – (D-)	0.2 (min)	V
V _{CM}	differential common mode range	Included V _{DI} range	0.8 (min) 2.5 (max)	V
V _{SE}	single ended receiver threshold		0.8 (min) 2.0 (max)	V
V _{IH}	high level input voltage		2.0 (min)	V
V _{IL}	low level input voltage		0.8 (max)	V
V _{OH}	high level output voltage	I _{OH} = -4 mA	2.3 (min)	V
V _{OL}	low level output voltage	I _{OL} = 4 mA	0.5 (max)	V
I _{IL}	low level input current	V _I = 0 V	RSTN pin : - 50.0 (max) the other pins : - 3.0 (max)	μA



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I _{IH}	high level input current	V _I = 3.6 V	SPDIFI, XSDIN pins : 3.0 (max) the other pins : 3.0 (max)	μA
I _{DD}	input supply current		20 (max)	mA
I _{suspend}	supply current in suspend		20 (max)	μA

6.4 AC electrical characteristics

6.4.1 USB transceiver signal (full speed mode)

symbol	parameter	test condition	min	max	unit
Tr	transition rise time for DP or DM		4	20	ns
Tf	transition fall time for DP or DM		4	20	ns
Trfm	rise / fall time matching	(Tr / Tf) * 100	90	110	%
Vo(crs)	signal crossover voltage		1.3	2.0	V

6.4.2 Operation clocks

symbol	parameter	Value	unit
CLKin	XIAUD/XOAUD crystal value	12.288 (typ)	MHz
	BITCLK serial data clock		
	CLKin duty cycle	50 ± 2	%
USBCLKin	XIUSB/XOUSB crystal value	6 (typ)	MHz
	USBCLKin duty cycle	50 ± 2	%

6.4.3 External EEPROM interface

symbol	parameter	Value	unit
Fsk	SK pin clock frequency	200	kHz

6.4.4 AC'97 Audio Codec interface timing

Please refer to AC'97 component specification ver2.1, ver2.2

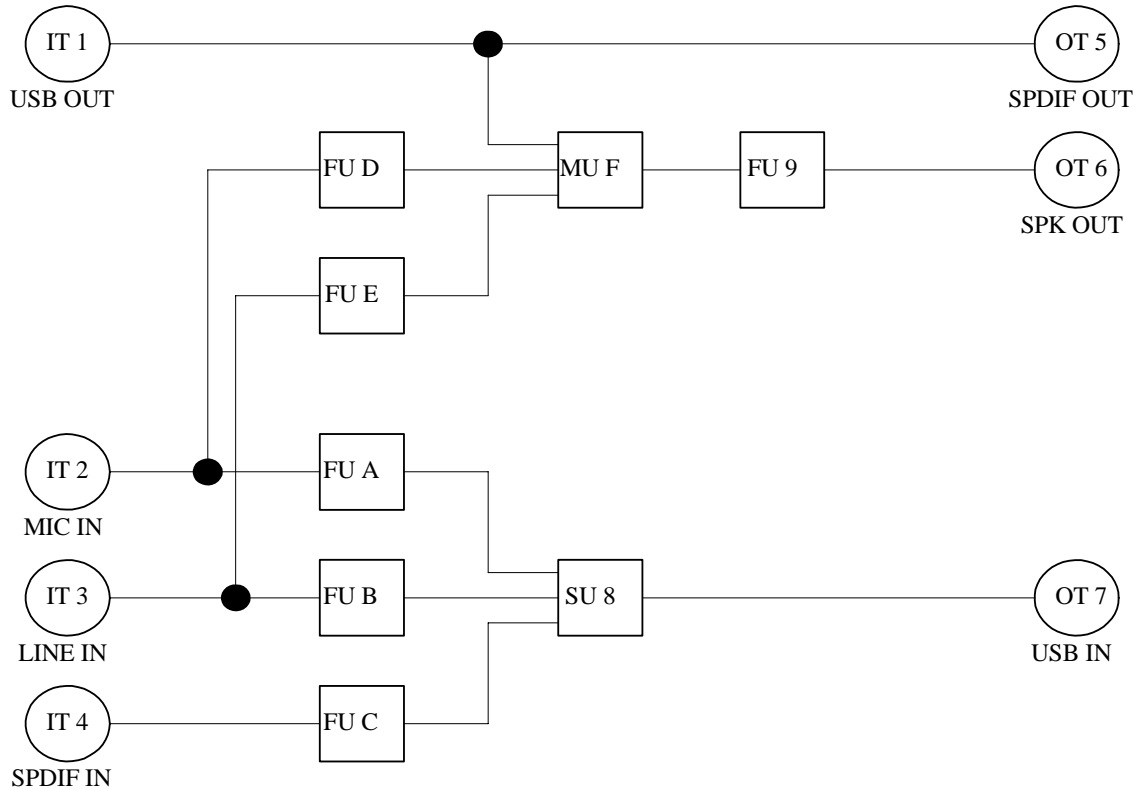
6.5 System level power consumption reference values

symbol	parameter	Value	unit
I _{sys_op}	USB device operation power consumption	100 (max)	mA
I _{sys_suspend}	USB device suspend power consumption	304 (max)	μA

VII. Function and control register description

7.1 Controller topology

AC-97 analog / digital playback and recording



7.2 Topology setting and button function

7.2.1 Topology setting

(a) Digital function only or analog function only

1. AC'97 D : only S/PDIF in/out
2. iMAC(44.1K) : only AC'97 analog out, 44.1KHz playback and recording without mixer
3. headset(44.1K & mixer) : only AC'97 analog out, 44.1KHz playback and recording with mixer
4. headset(44.1/48K & mixer) : only AC'97 analog out, 44.1KHz/48KHz playback and recording with mixer



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pin \ PD	AC'97 D	iMAC(44.1K)	Headset(44.1K & mixer)	headset(44.1/48K & mixer)
TYPE0	0	0	0	0
TYPE1	0	0	1	1
TYPE2	0	1	0	1
TYPE3	1: bused power (500mA)	1: bused power (500mA)	1: bused power (500mA)	1: bused power (500mA)
	0: bused power (100mA)	0: bused power (100mA)	0: bused power (100mA)	0: bused power (100mA)

Pllen	always use PLL	1: use PLL	1: use PLL	1: use PLL
		0: use Crystal	0: use Crystal	0: use Crystal

RECORD	1: D recording source, only SPDIF(def =SPDIF)	1: A recording source, only MIC (def = MIC)	1: A recording source, MIC & LINE(def = MIC)	1: A recording source, MIC & LINE(def = MIC)
	0: none	0: none	0: none	0: none

ROMOPT	(romopt, pllen) = (1,0) : 44.1K play/record rate & no HID, (1,1) : 44.1K play/record rate & HID	1: fit PC monitor & record Gain ctrl	1: fit PC monitor & record Gain ctrl MUTER button will mute monitor CH	0: MUTER button doesn't mute monitor CH
	(romopt, pllen) = (0,0) : 48K play rate, 32K/44.1K/48KHz record rate & HID (0,1) : 32K/44.1K/48KHz play rate, 32K/44.1K/48KHz record rate & HID	0: fit iMAC monitor & record Gain ctrl	0: fit iMAC monitor & record Gain ctrl MUTER button will mute monitor CH	1: MUTER button will mute monitor CH

‘ROMOPT’ value is set by ‘DR’ pin when no EEPROM is mounted on the board. Pulling high or pulling low at DR pin can set ‘ROMOPT’ value to be 1 or 0. When EEPROM is used on the board, ‘ROMOPT’ is defined by USB product ID bit1.

(b) Digital + analog function

1. AC'97 A+D+REC(A) : Digital and Analog playback, Analog recording only
2. AC'97 A+D+REC(A+D) : Digital and Analog playback, Digital and Analog recording
3. AC'97 A+D+H+REC(A) : Digital and Analog playback, Analog recording only, USB HID function enable
4. AC'97 A+D+H+REC(A+D) : Digital and Analog playback, Digital and Analog recording, USB HID function enable

pin \ PD	AC'97 A+D+REC(A)	AC'97 A+D+REC(A+D)	AC'97 A+D+H+REC(A)	AC'97 A+D+H+REC(A+D)
TYPE0	1	1	1	1
TYPE1	0	0	1	1
TYPE2	0	1	0	1



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TYPE3	1: bused power (500mA)	1: bused power (500mA)	1: bused power (500mA)	1: bused power (500mA)
	0: bused power (100mA)	0: bused power (100mA)	0: bused power (100mA)	0: bused power (100mA)

PLLEN	1: use PLL	1: use PLL	1: use PLL	1: use PLL
	0: use Crystal	0: use Crystal	0: use Crystal	0: use Crystal

RECORD	1: A recording source, MIC & LINE (def = MIC)	1: A+D recording sources, MIC & LINE & SPDIF (def = MIC)	1: A recording source, MIC & LINE (def = MIC)	1: A+D recording sources, MIC & LINE & SPDIF (def = MIC)
	0: none	0: none	0: none	0: none

ROMOPT	0: MUTER button doesn't mute monitor CH	0: MUTER button doesn't mute monitor CH	0: MUTER button doesn't mute monitor CH	0: MUTER button doesn't mute monitor CH
	1: MUTER button will mute monitor CH	1: MUTER button will mute monitor CH	1: MUTER button will mute monitor CH	1: MUTER button will mute monitor CH

‘ROMOPT’ value is set by ‘DR’ pin when no EEPROM is mounted on the board. Pulling high or pulling low at DR pin can set ‘ROMOPT’ value to be 1 or 0. When EEPROM is used on the board, ‘ROMOPT’ is defined by USB product ID bit1.

SN1113 can adopt two type clock sources for internal logic. One is using external PLL and the other is using external crystal. ‘PLLEN’ pin is used to define clock source. When using external PLL, it can synchronize to the USB frame rate. If the USB audio device uses PLL as clock source and enables USB HID function, it can convey AC-3 data stream by vendor specific software when playing DVD on PC.

‘RECORD’ pin is used to enable recording function. When the USB audio device having recording function is plugged into PC, there is a default recording source defined above table. If ‘RECORD’ pin is pulled down, then the USB audio device has no recording function.

7.2.2 button function

The SN1113 has four buttons to control playback and recording volume. It supports volume up, volume down, play mute, and recording mute. Button function is only effective in analog terminal. 1M pull-up resistors connected to 3.3V are recommended for these pins. It supports remote wakeup from device. A device in the resume state may respond to pressing button event by signaling a wakeup to PC via the USB.

7.2.3 LED indicator

There are two LED pins used to indicate the operation condition. ‘LEDN’ is flashing in a 256ms period during playback and recording. ‘HIDMUTER’ lights up when pressing ‘MUTER’ button to enable recording mute function.

7.3 Playback / recording sample rate under different product configuration

Product	Playback	Recording	notes
AC'97 A+D+REC(A), AC'97 A+D+REC(A+D), AC'97 A+D+H+REC(A), AC'97 A+D+H+REC(A+D)	D : 48KHz , A : 48KHz	D : 48KHz/ 44.1KHz , A : 48KHz/ 44.1KHz	when playing AC3 data stream to Digital output, mute Analog output
headset(44.1/48K & mixer)	44.1KHz/ 48KHz	44.1KHz/ 48KHz	when playing 44.1KHz , mute Digital output
iMAC(44.1K), headset(44.1K & mixer)	44.1KHz	44.1KHz	when playing 44.1KHz , mute Digital output
AC'97 D	44.1KHz (ROMOPT=1'b1, PLEN=1'b1 / 1'b0)	44.1KHz	
	48KHz (ROMOPT=1'b0 & PLEN=1'b0)	32K/ 44.1K/ 48KHz	
	32K/44.1K/48KHz (ROMOPT=1'b0 & PLEN=1'b1)	32K/ 44.1K/ 48KHz	

7.4 Audio output

SN1113 supports 16-bit stereo PCM audio data output at 32K, 44.1K and 48KHz sample rate. The audio data sent from USB is sent to both SPDIF out terminal (digital out) and Speaker out terminal (analog out). AC'97 Codec can be used at the Speaker out terminal to get analog audio sound. If the device uses external PLL and enable USB HID function, it can convey AC-3 data stream to S/PDIF out terminal (digital out).

7.5 Audio input

SN1113 can record 16~24 bits stereo PCM audio data at 32, 44.1 and 48KHz sample rate via S/PDIF input. It converts incoming audio data format to 16 bits PCM data. In digital recording,



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SN1113 supports SCMS (serial copy management system); if incoming digital audio data has copyright protection enabled, it will not record this audio data and send silent audio data to PC.

Because the digital audio data has its original data format (16~24bits) and sample rate, sample rate in recording software on PC should be set as the same rate when user wants to record this digital audio data. For analog audio data recording, it supports two sampling rate : 44.1KHz and 48KHz.

7.6 EEPROM data storage pattern

EEPROM address	High byte (MSB to LSB)	Low byte (MSB to LSB)	Notes
0	idVendor high byte	idVendor low byte	
1	idProduct high byte	idProduct low byte	
2	Control word high byte	Control word low byte	Refer to the next table
3	Reg address	X	Programming AC'97 reg address
4	Reg dataH	Reg dataL	Programming reg data
5	Reg address	X	Programming AC'97 reg address
6	Reg dataH	Reg dataL	Programming reg data
.	Reg address	X	Programming AC'97 reg address
.	Reg dataH	Reg dataL	Programming reg data

* 16 bit per word at each address

control word (address 02)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	cdcreg	outsw	regcnt3	regcnt2	Regcnt1	regcnt0	Chk7	Chk6	Chk5	Chk4	Chk3	Chk2	Chk1	Chk0

bit 15 – bit 14 R – reserved

bit 13 cdcreg – 0 : programming with EEPROM values

 1: programming with SN1113 built-in values

bit 12 outsw – 0 : volume control Aux. Line Out (0x04) 1 : Volume control Stereo Line Out (0x02)

bit11 – bit 8 regcnt [3:0] – total number of programming AC'97 Codec registers

bit 7 – bit 0 Chk [7:0] – EEPROM magic code (Hex AB), used to check EEPROM existence

programming example:

bit 13 = 1, ignore setting in bit 11 to bit8 , using SN1113 built-in programming values

bit 13 = 0, regcnt [3:0] ≠ 0 – using programming values stored in EEPROM

bit 13 = 0, regcnt [3:0] = 0 – inhibition



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AC'97 Codec registers default values

(1) iMAC mode

Address (HEX)	Name	Setting value
04	Alt. line output vol.	0000
2A	Ext. audio stat/control	0001
2C	PCM front DAC rate	AC44
1A	Record select	0000
1C	Record gain	0000
18	PCM out volume	0808
32	PCM LR ADC rate	AC44
10	Line in volume	8808
0E	Mic in volume	8008

(2) Headset (44.1K & Mixer) mode

Address (HEX)	Name	Setting value
04	Alt. line output vol.	0000
2A	Ext. audio stat/control	0001
2C	PCM front DAC rate	AC44
1A	Record select	0000
1C	Record gain	0000
18	PCM out volume	0808
32	PCM LR ADC rate	AC44
10	Line in volume	8808
0E	Mic in volume	0008

(3) The other modes

Address (HEX)	Name	Setting value
04	Alt. line output vol.	0000
2A	Ext. audio stat/control	0001
10	Line in volume	8808
1A	Record select	0000
1C	Record gain	0000
18	PCM out volume	0808
0E	Mic in volume	0008

EEPROM read sequence:

idVendor (MSB to LSB) → idProduct (MSB to LSB) → Control word → Programming reg address →
Programming reg data ...

7.7 SPDIF

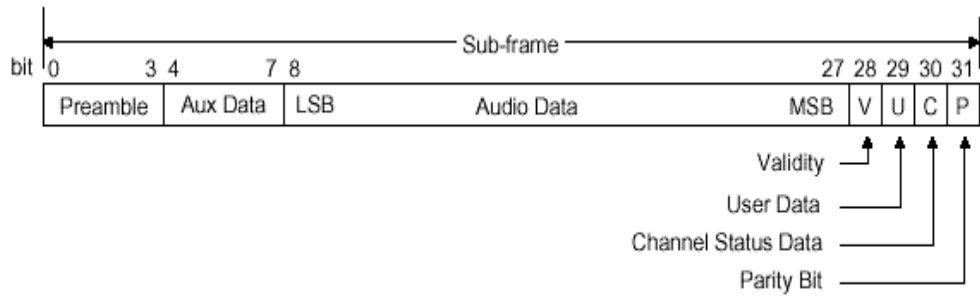


Figure 1. Sub-frame Format

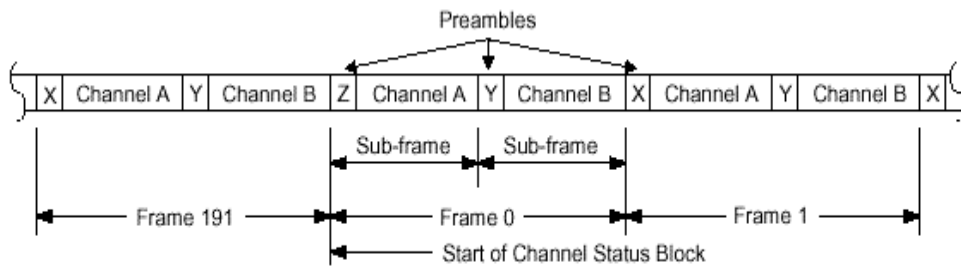


Figure 2. Frame/Block Format

SPDIF Channel Status Block Structure –consumer format

	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
byte0	consumer	audio/data	copyright	emphasis			mode	
default	0	0(W)	1(W)	0	0	0	0	0

byte1	category code							L
default	0(W)	0(W)	0(W)	0(W)	0(W)	0(W)	0(W)	0(W)

byte2	source number				channel number			
default	1	0	0	0	1	0	0	0
					0	1	0	0

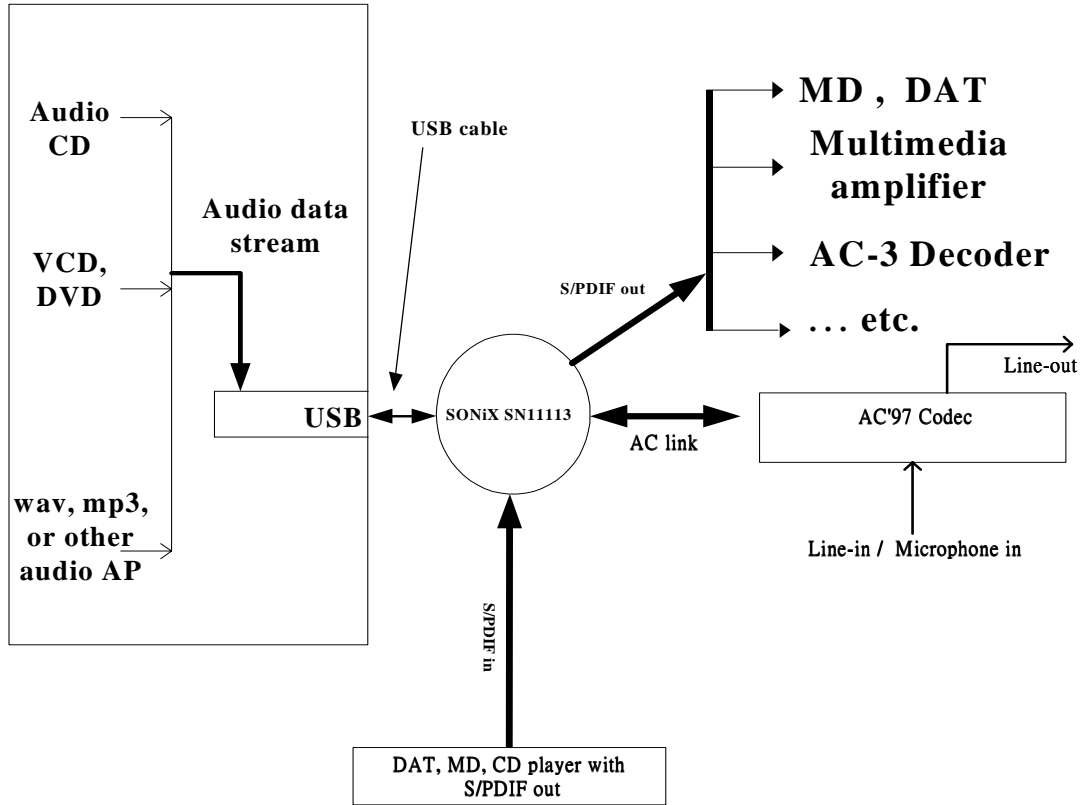
byte3	sampling frequency				clock accuracy		reserved	
default	32KHz	1	1	0	0	0	0	0
	44.1KHz	0	0	0	0			
	48KHz	0	1	0	0			

W : These bits can be programmed by vendor specific driver via USB.

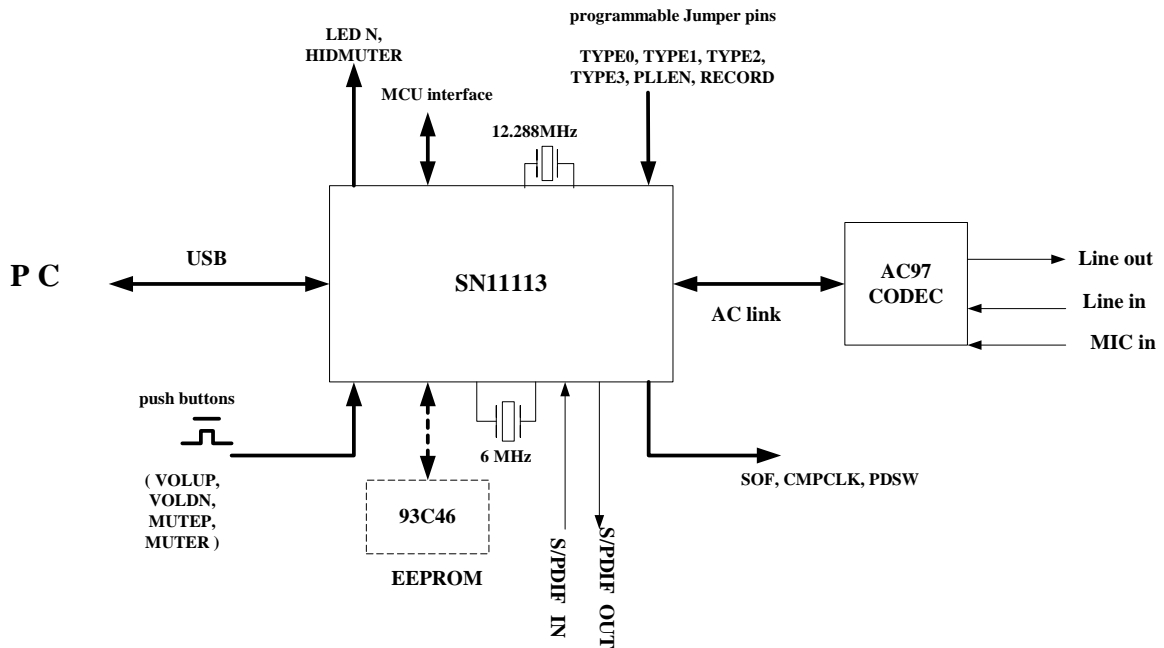
VIII. Application

8.1 Application example

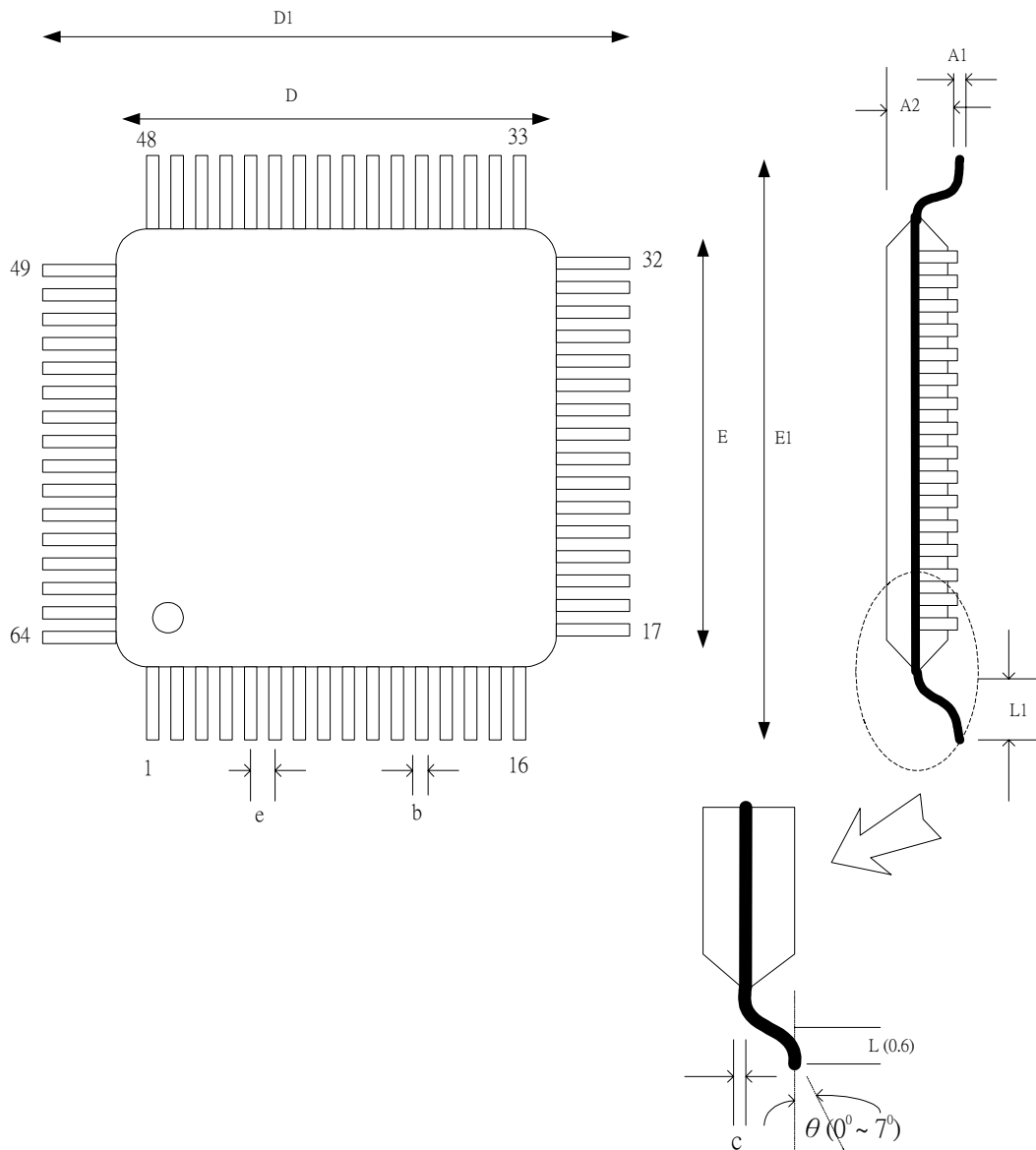
PC or NoteBook



8.2 Brief application circuit chart



* detail application circuit is available by customer request

IX. Package Specification

64-pin LQFP package

Lead Count	Body Size			
	D	E	D1	E1
64	10.00	10.00	12.00	12.00

Stand-off	Body Thk	Lead Length	Lead Width	Lead Thk	Lead Pitch
A1	A2	L1	b	c	e
0.10	1.40	1.00	0.24	0.125	0.50

Unit : mm

Appendix A

Two wire series bus in SN1113

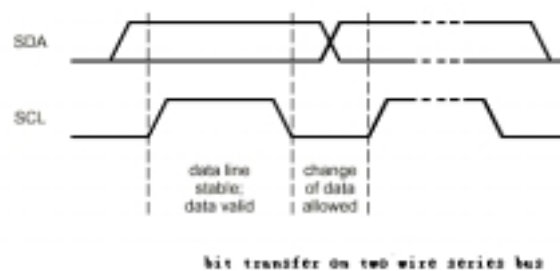
To provide extension capability, SN1113 contains a two wire series bus circuitry as an interface to MCU. The two wire series bus serves as a slave device with bit rate up to 400Kbps (fast mode). MCU can write two bytes to SN1113 with 8-bit register address $8'bxxxxxx0$ and $8'bxxxxxx1$; where 'x' means either '0' or '1'. MCU can also read one byte from SN1113 by any register address. The 7-bit slave address of SN1113 is assigned as $7'b0111000$.

With 'HIDEN' activated, SN1113 will transfer the two bytes to the USB host via an additional interrupt pipe when any byte is written to it by MCU. Accompany with the two bytes two wire series bus data, SN1113 will also send one byte of button status. The sequence of the upward HID report is the button status first (LSB), then register with address $8'bxxxxxx0$, then register with address $8'bxxxxxx1$ (MSB). The USB host will keep polling the upward HID report every 32mS. When there is any button pressed or released, or two wire series bus data coming, SN1113 will transfer the three bytes of HID report to the USB host.

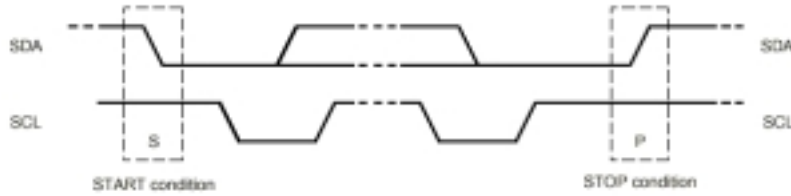
SN1113 can also transfer one byte data from the USB host to its register when 'HIDEN' is active. This is accomplished by a 'Set Output Report' HID class request via default control pipe. MCU can get this downward byte by polling. That is, MCU should read the byte at its favorite rate.

This document just provides simple description of the two wire series bus. User can get more detailed explanation from the specification.

SN1113 has one input pin 'SCL' where it gets two wire series bus clock from MCU, and one open-drain output pin 'SDA' where it sends or receives serial signal to/from MCU. As shown below, 'SDA' should be stable when 'SCL' is high, and can have transition only when 'SCL' is low.

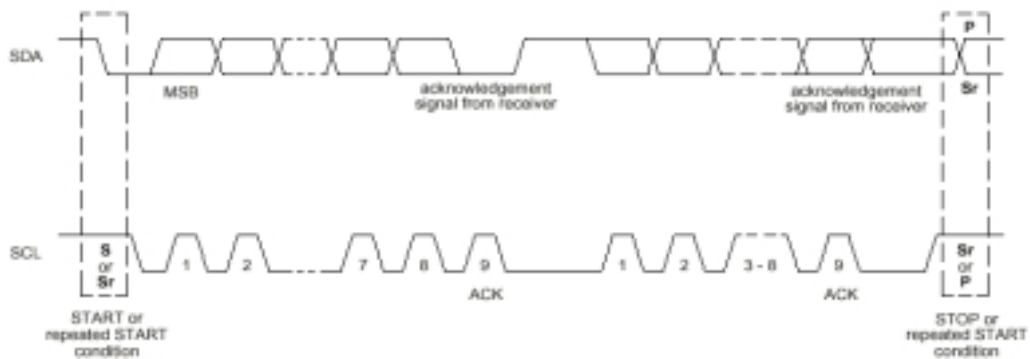


START and STOP conditions shown below are the exception. Every two wire series bus transaction begins from a START, and ends with a STOP, or another START (repeated START).

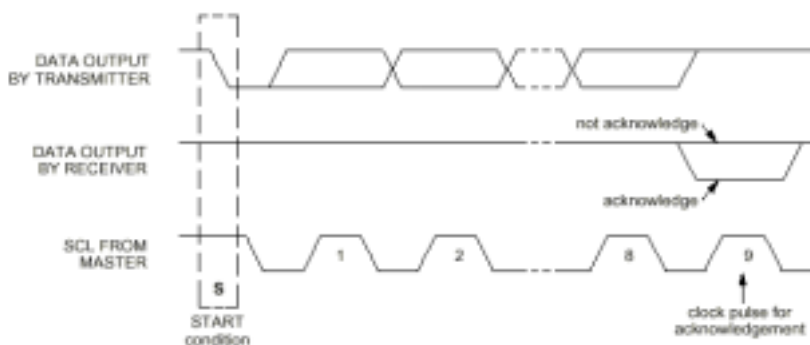


START and STOP conditions.

The figure below demonstrates a typical two wire series bus transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more detailed about acknowledgement bit. Note that 'SCL' is always driven by the master.

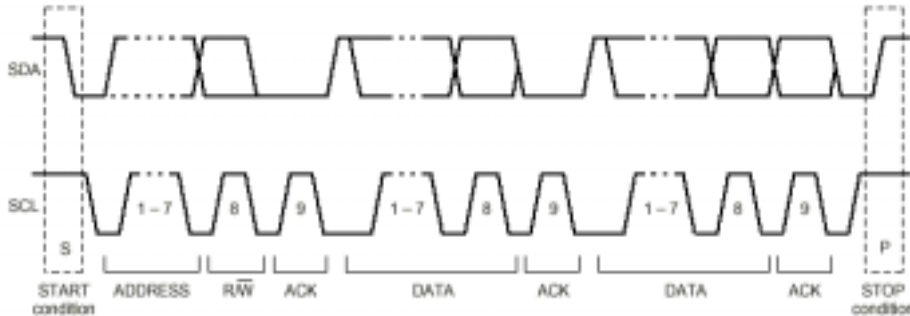


data transfer on two wire series bus



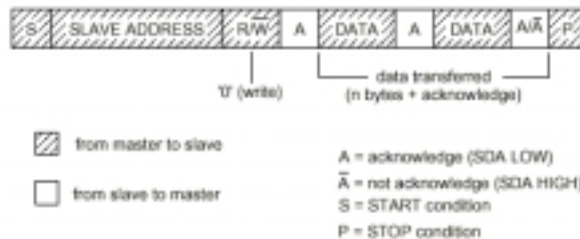
acknowledge on two wire series bus

The figure below shows a complete data transfer. After a START, MCU should send 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low. The first acknowledgement is always a duty of SN1113.



A complete data transfer.

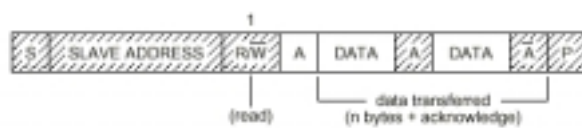
In the write transfer, MCU keep acting as the master and the transfer direction is not changed. The following figure gives an example of one byte write transfer.



A master-transmitter addressing a slave receiver with a 7-bit address. The transfer direction is not changed.

SN1113 regards the first DATA byte as the register address. The second DATA byte is the content that MCU would like to write at the register address. If there is the third DATA byte, SN1113 will record this byte to the other register address. Note that the register address is auto-increment.

The figure below shows an example of two bytes read transfer. Because SN1113 has only one byte register to be read, the second DATA byte will be the same as the first one.



A master reads a slave immediately after the first byte.

Please note that the USB host try to get new HID data every 32mS. It's quite slow. If the continuous two wire series bus write transfers are too close in time, the former transfer may have no effect.



SN11113 spec

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