



USB Audio Controller

Data Sheet

SN11220ACF

DATA SHEET

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SN11220ACF

USB Audio Controller

V1.01

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I. Description

SONiX SN11220ACF is an USB audio controller designed especially for voice-band and DECT phone CODEC. It supports 8 different sampling rates, 8KHz, 11.025KHz, 16KHz, 22.05KHz, 24KHz, 32KHz, 44.1KHz and 48KHz in playback and recording. These 8 frequencies are selectable by setting the three external pins.

II. Features

- 8KHz, 11.025KHz, 16KHz, 22.05KHz, 24KHz, 32KHz, 44.1KHz and 48KHz sampling rates for 2 channels playback and recording
- Full-duplex playback/ recording audio stream without sound card in PC
- Compatible with Win98 SE/ WinME/ Win2000/ WinXP and MacOS 9.2.1/MacOS10.2/MacOS10.4 without additional driver
- Plug-and-Play operation with Microsoft OS or MacOS default drivers
- Compliant with USB specification v1.1
- Compliant with USB audio device class specification v1.0
- Supports USB full speed 12Mbps/s serial data transmission
- USB bus power or self power option
- Supports suspend/resume and remote wake-up
- 6MHz crystal input with on-chip PLL and embedded transceiver for USB
- On-chip PLL for synchronized with USB host for CODEC interface
- USB audio function topology has four input terminals, three output terminals, one selector unit, one mixer unit and six feature units
- USB alternate setting0 is a zero-bandwidth setting; used to release the claimed bandwidth on the bus when this device is inactive
- Isochronous transfer uses adaptive, synchronous synchronization
- Supports 2ch CODEC with I²S, Left-justified serial interface format
- Embedded Digital Volume Control of Line out / in for I²S interface mode
- Compliant with USB HID class specification v1.1; pin control for volume up / down, play mute, and record mute
- Supports two wire series bus interface; slave only interface with transfer speed up to 400Kbps(Fast-mode)
- EEPROM interface for customized USB IDs and strings; CODEC registers programming



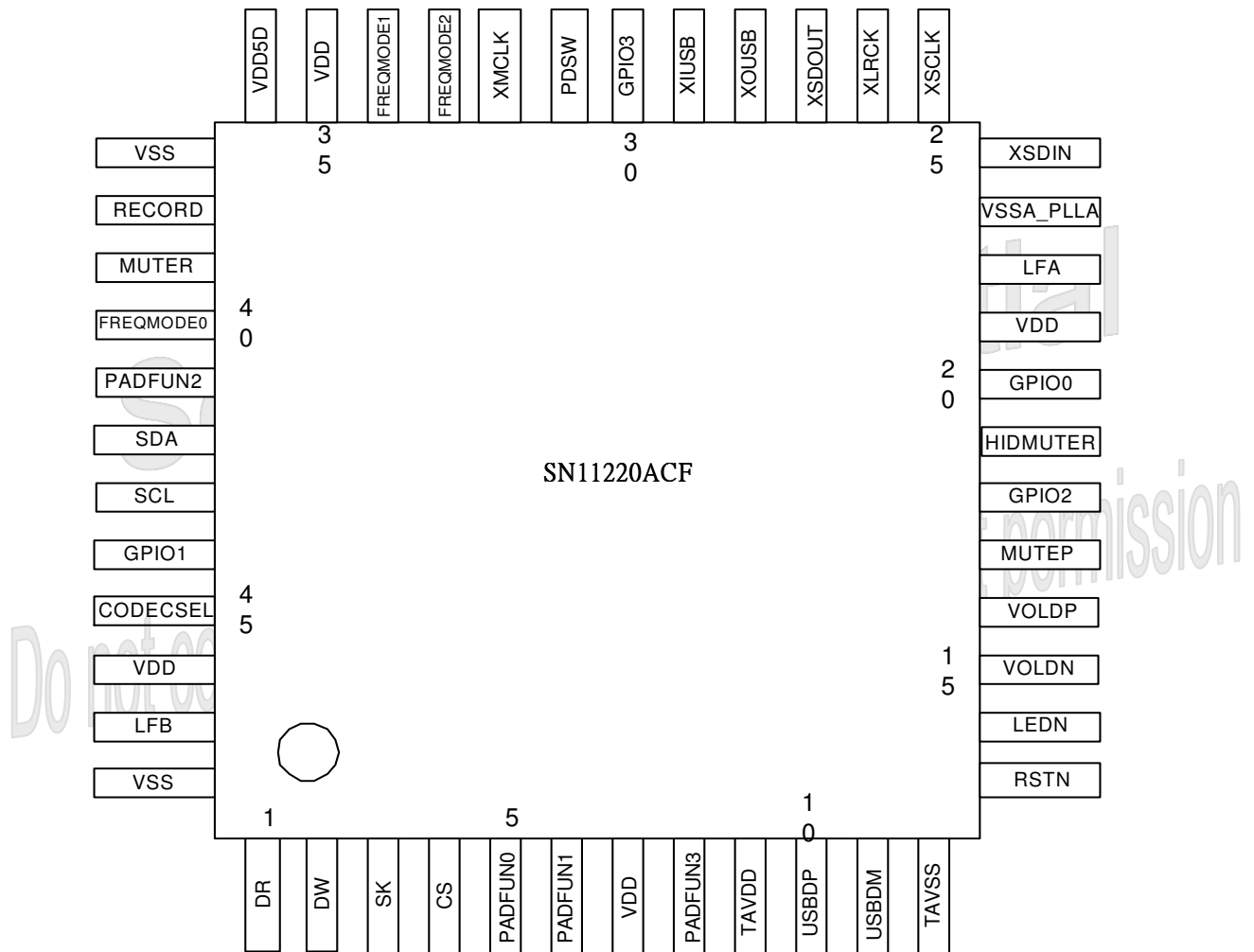
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- 3.3 V core operation and 5 V tolerant I/O
- Available in 48-pin LQFP (7x7 mm)
- System on chip solution: low cost and easy implementation without external memory
- LED indicator pins for playback and recording mute
- 4 GPIO pins controlled via USB HID
- Claim variable max packet size for saving USB bandwidth; according to sampling rate under
- HID interrupt interval can be modified via EEPROM
- EEPROM content can be read from HID pipe
- Transferring length up to each 16 bytes among PC to device and device to PC by USB HID
- MCU can write particular register address (0x0b) to activate device to upload update data to PC when MCU has written new data through two wire series bus interface (section VIII)
- Embedded 5V to 3.3V regulator
- Features programmable by jumper pins and EEPROM values
- Support voiceband CODEC PCM interface in master/slave operation
- A-law and μ -law translation

III. Ordering information

SN11220ACF: 48-pin LQFP (7x7x1.4 mm)





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IV. Pin assignment and description (48-pin LQFP)

PIN No.	Pad Name	Pin Type	Description
1	DR(EEPROM_DO)	I, ST	EEPROM data output
2	DW(EEPROM_DI)	O, 4mA, SR	EEPROM data input
3	SK(EEPROM_SK)	O, 4mA, SR	EEPROM clock pin
4	CS(EEPROM_CS)	O, 4mA, SR	EEPROM chip select
5	PADFUN 0	I, ST	CODEC function configuration pin 0 (page 11)
6	PADFUN 1	I, ST	CODEC function configuration pin 1 (page 11)
7	VDD	P	3.3V power pin
8	PADFUN 3	I, ST	CODEC function configuration pin 3 (page 11)
9	TAVDD	P	Power pin for USB transceiver
10	USBDP	I/O	USB data plus (D+)
11	USBDM	I/O	USB data minus (D-)
12	TAVSS	P	Power pin for USB transceiver
13	RSTN	I, ST, PU	System reset pin, low enable. Pull-high this pin.
14	LEDN	O, 8mA, SR	LED indicator pin, output low after power on reset, toggle during operation
15	VOLDN	I, ST	Volume down control, edge trigger with 64ms de-bouncing circuit
16	VOLUP	I, ST	Volume up control, edge trigger with 64ms de-bouncing circuit
17	MUTEP	I, ST	Playback mute control pin, edge trigger with 64ms de-bouncing circuit
18	GPIO2	I/O	General Purpose I/O 2
19	HIDMUTER	O, 8mA, SR	Playback mute led indicator
20	GPIO0	I/O	General Purpose I/O 0



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21	VDD	P	3.3V power pin
22	LFA	I/O	Filter for internal PLL
23	VSSA_PLLA	P	GND pin
24	XSDIN/PCM_DIN	I, ST	I ² S Din / PCM_Din
25	XSCLK/PCM_CLK	O, 4mA, SR	I ² S SCLK for play/PCM_CLK (Master out/Slave in)
26	XLRCK/PCM_FS	O, 4mA, SR	I ² S L/R frame for play /PCM_FS (Master out/Slave in)
27	XSDOUT/ PCM_DOUT	O, 4mA, SR	I ² S Dout/PCM_Dout
28	XOUSB	O	6 MHz clock osc pin for USB PLL
29	XIUSB	I	6 MHz clock osc pin for USB PLL
30	GPIO3	I/O	General Purpose I/O 3
31	PDSW	O, 4mA, SR	Power down switch control -- 0: normal mode, 1: power down mode. This pin is in power down mode when the device is in suspending mode.
32	XMCLK/BITCLK	O, 8mA, SR	I ² S CODEC master clock for play
33	FREQMODE2	I, ST	Frequency mode select 2. {freqmode 2, 1, 0}: 011: 48K, 010: 44.1K, 001: 11.025K, 000: 8K, 111: 32K, 110: 24.1K, 101: 22.05K, 100: 16K
34	FREQMODE1	I, ST	Frequency mode select 1. {freqmode 2, 1, 0}: 011: 48K, 010: 44.1K, 001: 11.025K, 000: 8K, 111: 32K, 110: 24.1K, 101: 22.05K, 100: 16K
35	VDD	P	3.3V power pin / regulator 3.3V out
36	VDD5D	P	5V power pin
37	VSS	P	GND pin
38	RECORD	I, ST	Recording function enable (1) / disable (0)
39	MUTER	I, ST	Recording mute, edge trigger with 64ms de-bouncing circuit
40	FREQMODE0	I, ST	Frequency mode select 1. {freqmode 2, 1, 0}: 011: 48K, 010: 44.1K, 001: 11.025K, 000: 8K, 111: 32K, 110: 24.1K, 101: 22.05K, 100: 16K



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41	PADFUN 2	I, ST	CODEC function configuration pin 2 (Page11)
42	SDA	I/O,4mA, SR	data pin of two-wire serial port for external MCU control. This pin must be UP by resister..
43	SCL	I, ST	clock pin of two-wire serial port for external MCU control. This pin must be UP by resister.
44	GPIO1	I/O	General Purpose I/O 1
45	CODECSEL	I, ST	CODEC interface selection, it should be tied to 3.3V in the type of ACF.
46	VDD	P	3.3V Power pin
47	LFB	I/O	Filter for internal PLL
48	VSSA_PLLB	P	GND pin

** All input pin are 5 volt tolerance, TTL level and Schmitt trigger

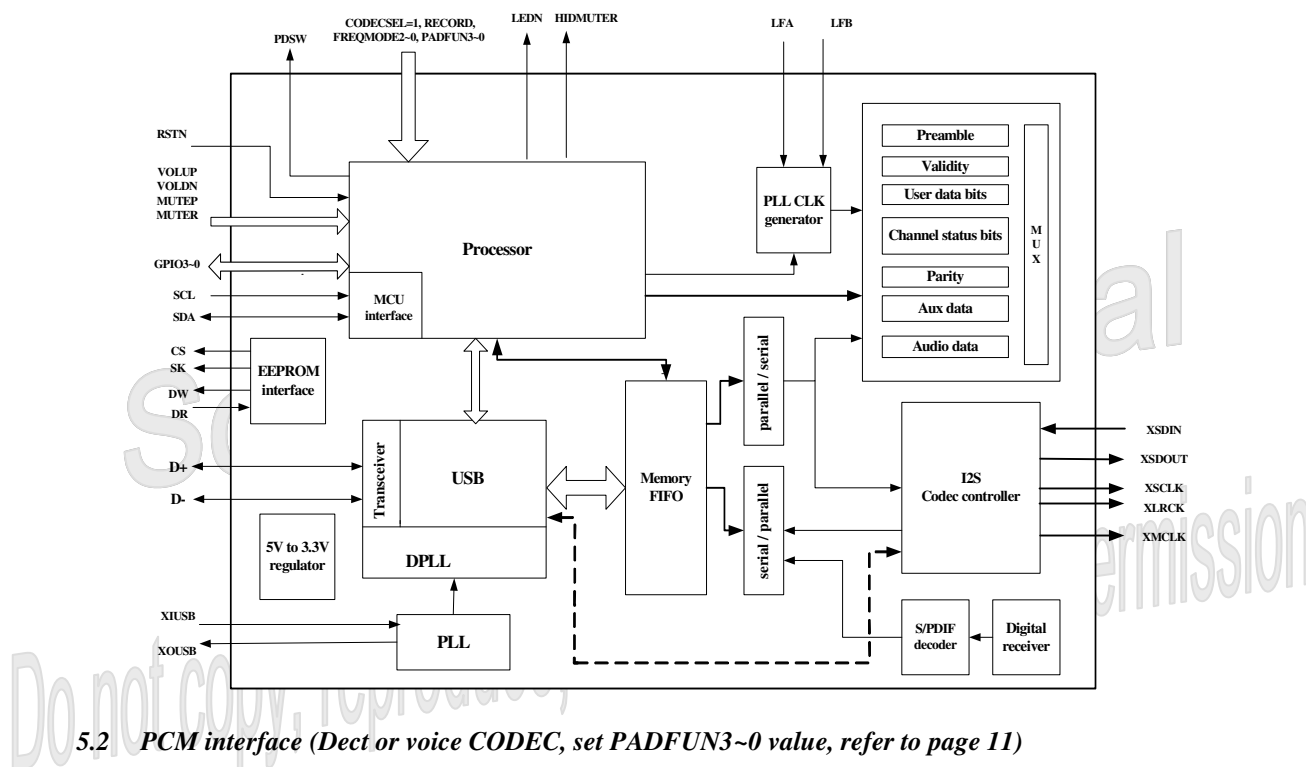
All output pins are slew rate control

I – input pin, O – output pin, P – power pin, ST – Schmitt trigger, SR – slew rate control,

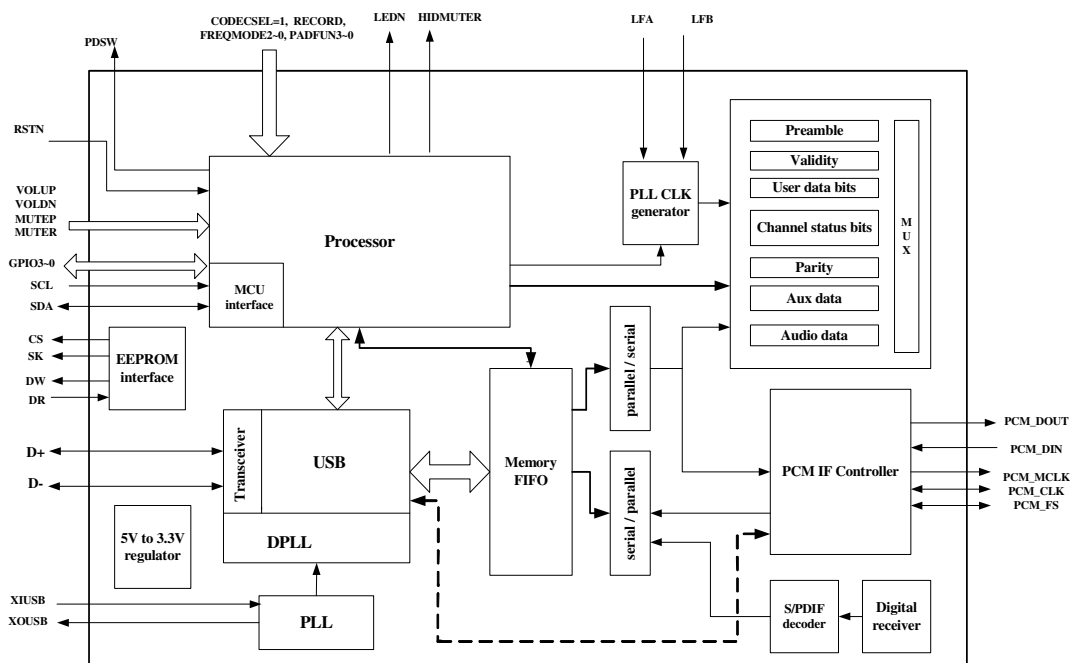
PU/PD – pull up or pull down

V. Block diagram

5.1 I²S interface (PADFUN3~0 = 0)



5.2 PCM interface (Dect or voice CODEC, set PADFUN3~0 value, refer to page 11)





VI. EEPROM contents arrangement

The SN11220ACF supports an external EEPROM (93C46) to be installed for the system manufacturers to customize the USB VID, PID and the vendor/product strings being displayed in the OS to differentiate their own products with the others. The maximum length of the vendor and product string is 16 ASCII characters each. Some of the features supported by the chip can also be programmed through setting proper values in the EEPROM. The table below shows the format of the EEPROM. The detail is described in the following sub-section.

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Address	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0x00	Vendor ID (VID)															
0x01	Product ID (PID)															
0x02	Manufacture string 15								Manufacture string 14							
0x03	Manufacture string 13								Manufacture string 12							
0x04	Manufacture string 11								Manufacture string 10							
0x05	Manufacture string 9								Manufacture string 8							
0x06	Manufacture string 7								Manufacture string 6							
0x07	Manufacture string 5								Manufacture string 4							
0x08	Manufacture string 3								Manufacture string 2							
0x09	Manufacture string 1								Manufacture string 0							
0x0A	Product string 15								Product string 14							
0x0B	Product string 13								Product string 12							
0x0C	Product string 11								Product string 10							
0x0D	Product string 9								Product string 8							
0x0E	Product string 7								Product string 6							
0x0F	Product string 5								Product string 4							
0x10	Product string 3								Product string 2							
0x11	Product string 1								Product string 0							
0x12	Control word 1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LEFT JSEL	Reserved ➔ set to 0					REM OTE WE	SELF POW	Manufacture string #				Product string #			
0x13	Control word 2															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			Config	FUN3	FUN2	FUN1	FUN0	HID interval							
0x14	Control word 3															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	FS_ 512	0	0	Reserved ➔ set to 0											

USB VID and PID :

The default USB VID of SN11220ACF is 0x0C45. The default PID is composed by the configurations as below {0, 0, 0, 1, 1, 1, 0, 1, 1, 0, 1, 1, 1, RECORD, POWER_BIT, 1}. If pin38 tie to high, RECORD will equal “1”. The POWER_BIT is



used to indicate that the MaxPower in USB descriptor(“1” is 100mA, “0” is 500mA). The VID and PID can be changed by using EEPROM. Word address 0x00 is the VID value. Word address 0x01 is the PID value. The bit1 (POWER_BIT) of the PID value will affect the MaxPower in USB descriptor. It should be noted that forbids the VID and PID values cannot be set to 0x0000 or 0xFFFF.

Manufacturer and Product String :

The default manufacturer string is “GENERIC”. It can be changed by programming word 0x02 to 0x09 in EEPROM and set the length of it in word 0x12, bit 4 to 7. Manufacturer string length = manufacturer string # + 1 (manufacturer string # = 0x0F means manufacturer string length = 16 bytes) .

There are total of two default product strings in SN11220ACF, depending on the features selected. They are listed in the table below.

RECORD	Product String
0	USB Speaker
1	USB Headset

The product string can be changed by programming words 0x0A to 0x11 in EEPROM and set the length of it in word 0x12, bit 0 to 3. Product string length = product string # + 1 (product string # = 0x0F means product string length = 16 bytes) .

Control word 1 :

The control word 1 is located in word 0x12 of EEPROM.

Bit 0 to 7 is the length of USB strings and has been explained in previous paragraphs.

Bit 8 is used to set the self-power bit in the USB descriptor.

Bit 9 is used to enable remote wake feature in USB. The remote wakeup keys are VOLP/VOLD/MUTEP/MUTER.

Bit 10 to 14 is reserved in SN11220ACF.

Bit 15 is to enable the left-justify format in I²S mode.

Control word 2 :

The control word 2 is located in word 0x13 of EEPROM.

Bit 0 to 7 is the interval of USB HID Report IN. For example, bit 0 to 7 = 0x0A

means that the interval of USB HID Report IN is 10ms and this is default value.

Bit 13 to 15 are reserved for future using and influence no function of SN11220ACF.

Bit 12 is used to enable the EEPROM setting for configure the source of CODEC. If bit 12 is “0”, PCM configuration is defined by pin PADFUN3~0.

PCM configuration bit = 1'b1	Defined by PCM setting3~0
PCM configuration bit = 1'b0	Defined by pin (PADFUN3~0)

Bit 11 to 8 is the configuration of CODEC if Bit 12 is set to 1.

Voice CODEC	Function (Transfer interface / data format)	
4'b0000	Use normal CODEC (I ² S) / linear PCM	
4'b0001	PCM IF / Long frame μ -law	
4'b0010	PCM IF / Short frame μ -law	
4'b0100	Echo cancellation IF / linear PCM	
4'b0011	PCM IF / Long frame a-law	
4'b0110	PCM IF / Short frame a-law	
DECT chip	Type	Function (Transfer interface / data format)
4'b1000	Philips	Slave mode ^{*1} / linear PCM
4'b1010	Philips	Slave mode / μ -law
4'b1011	Philips	Slave mode / a-law
4'b1001	Philips	Master mode ^{*2} / linear PCM
4'b0111	Philips	Master mode / μ -law
4'b0101	Philips	Master mode / a-law
4'b1100	NS	Slave mode / linear PCM
4'b1101	NS	Slave mode / μ -law
4'b1110	NS	Slave mode / a-law
4'b1111	NS	Master mode / linear PCM

^{*1}. Slave mode: PCM_CLK & PCM_FS from Dect chip to SN11220.

^{*2}. Master mode: PCM_CLK & PCM_FS from SN11220 to Dect chip.

Control word 3 :

The control word 3 is located in word 0x14 of EEPROM.

Bit 0 to 11 is reserved in SN11220ACF.

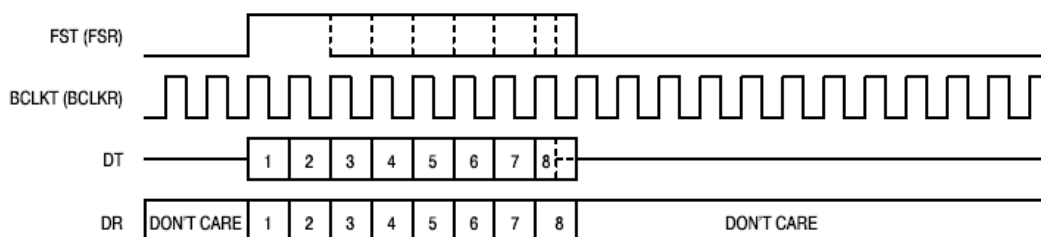
Bit 12 be set to “0”.

Bit 13 be set to “0”.

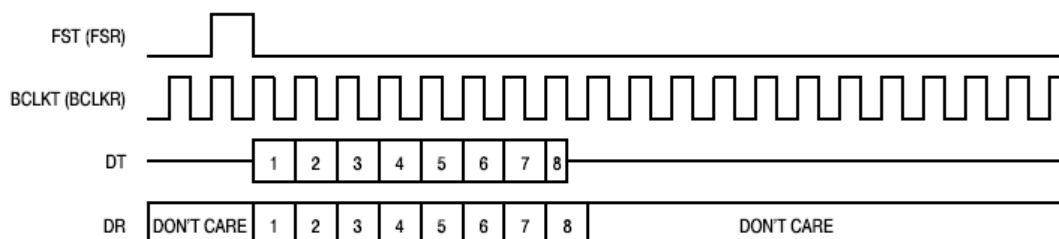
Bit 14 selects 512 times sampling rate for I²S interface.

Bit 15 be set to “0”.

PCM IF Long-frame



PCM IF Short-frame



VII. HID bytes arrangement :

The SN11220ACF is equipped with a special feature to let the host software to communicate with the USB downstream devices via the HID pipe. Using this feature, the system manufacturers can easily upgrade or increase the functions of their product by just updating the software installed on the PC. There are 16 bytes each for HID in and HID out. They will be explained in the paragraphs below separately.

To receive the data from two-wire serial port and button/GPIO status from the SN11220ACF, there are two ways. The first is to receive the HID report of the HID pipe regularly. If any button/GPIO value changes or data received from the two-wire serial port, the new values will be sent to the host every HID interval time (defined in word 0x13 bit 0 to 7 and default is 10ms) . The second way is to issue a HID class

request “Get Report” to get the input report.

To send data to the USB audio controller, the host software should issue a HID class request “Set Report” to send the output report. There are total of 16 bytes of both output report and input report. The format of them is described as below.

Report In Bytes

Byte 0	Buttons	Bit 0	Vol up
		Bit 1	Vol down
		Bit 2	Mute play
		Bit 3	Mute record (host can't do this)
		Bit 4	GPIO0 state (low=“0”, high=“1”)
		Bit 5	GPIO1 state (low=“0”, high=“1”)
		Bit 6	GPIO2 state (low=“0”, high=“1”)
		Bit 7	GPIO3 state (low=“0”, high=“1”)
Byte 1	MCU byte 0	Bit 7~0	Two-wire serial port input register 0
Byte 2	MCU byte 1	Bit 7~0	Two-wire serial port input register 1
Byte 3	ACF reserved	Bit 7~0	Can be ignored
Byte 4	ACF reserved	Bit 7~0	Can be ignored
Byte 5	ACF reserved	Bit 7~0	Can be ignored
Byte 6	ACF reserved	Bit 7~0	Can be ignored
Byte 7	MCU byte 2	Bit 7~0	Two-wire serial port input register 2
Byte 8	MCU byte 3	Bit 7~0	Two-wire serial port input register 3
Byte 9	MCU byte 4	Bit 7~0	Two-wire serial port input register 4
Byte A	MCU byte 5	Bit 7~0	Two-wire serial port input register 5
Byte B	MCU byte 6	Bit 7~0	Two-wire serial port input register 6
Byte C	MCU byte 7	Bit 7~0	Two-wire serial port input register 7
Byte D	MCU byte 8	Bit 7~0	Two-wire serial port input register 8
Byte E	MCU byte 9	Bit 7~0	Two-wire serial port input register 9
Byte F	Used by SONiX	Bit 7~0	Fixed 0x00

Byte 0 :

Byte 0 is used to report the button and GPIO status of the USB device.



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Bit 0 and 1 are linked to the master volume control bar of the audio control panel in the OS.

Bit 2 is linked to the master playback mute checkbox of the audio control panel in the OS.

Bit 3 is used to mute the recording. But there is no this command in OS. SONiX design this function in the SN11220.

Bit 4 to 7 is corresponding to the value of GPIO 0 to 3.

Byte 1 :

Byte 1 is used to return the register 0 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte 2 :

Byte 2 is used to return the register 1 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte 3 :

Byte 3 can be ignored for SN11220ACF.

Byte 4 :

Byte 4 can be ignored for SN11220ACF.

Byte 5 :

Byte 5 can be ignored for SN11220ACF.

Byte 6 :

Byte 6 can be ignored for SN11220ACF.

Byte 7 :

Byte 7 is used to return the register 2 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte 8 :

Byte 8 is used to return the register 3 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte 9 :

Byte 9 is used to return the register 4 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte A :

Byte A is used to return the register 5 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte B :

Byte B is used to return the register 6 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte C :

Byte C is used to return the register 7 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte D :

Byte D is used to return the register 8 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte E :

Byte E is used to return the register 9 value received by the two-wire serial port of SN11220ACF. Please refer to section VIII.

Byte F :

Byte F is used by SONiX for the special purpose. In SN11220ACF, it will be set to 0x00 at any time.

Report Out Bytes

Byte 0	Setting	Bit 3~0	Can be ignored
		Bit 4	GPIO 0 Out/In select
		Bit 5	GPIO 1 Out/In select
		Bit 6	GPIO 2 Out/In select



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		Bit 7	GPIO 3 Out/In select
Byte 1	ACF reserved	Bit 7~0	Can be ignored
Byte 2	MCU byte 0	Bit 7~0	Two-wire serial port output register 0
Byte 3	GPIO out	Bit 0	GPIO 0 (set “1” to high, set “0” to low)
		Bit 1	GPIO 1 (set “1” to high, set “0” to low)
		Bit 2	GPIO 2 (set “1” to high, set “0” to low)
		Bit 3	GPIO 3 (set “1” to high, set “0” to low)
	Mode setting	Bit 6~4	HID control mode setting
	Volume control setting	Bit 7	Digital volume control enable (0) / disable (1)
Byte 4	ACF reserved	Bit 7~0	Can be ignored
Byte 5	ACF reserved	Bit 7~0	Can be ignored
Byte 6	ACF reserved	Bit 7~0	Can be ignored
Byte 7	MCU byte 1	Bit 7~0	Two-wire serial port output register 1
Byte 8	MCU byte 2	Bit 7~0	Two-wire serial port output register 2
Byte 9	MCU byte 3	Bit 7~0	Two-wire serial port output register 3
Byte A	MCU byte 4	Bit 7~0	Two-wire serial port output register 4
Byte B	MCU byte 5	Bit 7~0	Two-wire serial port output register 5
Byte C	MCU byte 6	Bit 7~0	Two-wire serial port output register 6
Byte D	MCU byte 7	Bit 7~0	Two-wire serial port output register 7
Byte E	MCU byte 8	Bit 7~0	Two-wire serial port output register 8
Byte F	MCU byte 9	Bit 7~0	Two-wire serial port output register 9

Byte 0 :

Bit 0 to 3 can be ignored for SN11220ACF.

Bit 4 to 7 when the HID is used to control the GPIOs, they select the directions of GPIO pins. For example, if bit4 is “1”, the GPIO0 is defined to input pin. If bit4 is “0”, the GPIO0 is defined to output pin. The USB host read GPIO input from ‘Report In’ bit4 to 7 of byte0. USB host output GPIO value is set from ‘Report Out’ bit0 to 3 of byte3.

Byte 1 :

Byte 1 can be ignored for SN11220ACF.

Byte 2 :

Byte 2 is used to set data to the register 0 of the two-wire serial port of SN11220ACF. For detail about how to access the register of the two-wire serial port of SN11220ACF, please refer to the section “Two-wire serial port definition”.

Byte 3 :

Considering together with byte 0, byte 3 is used to control the GPIO ports.

Bit 0 to 3 is used to set the values of GPIO ports if this GPIO is output pin.

Bit 4 to 6 is used to set the control mode of HID. As bellow,

Bit 6 ~ 4	HID mode setting
000	SN11220ACF don't use
001	HID program EEPROM
010	Don't use
011	Don't use
100	HID read EEPROM
101	Byte 0 bit 4 to 7 means GPIO Out/In select
110	SN11220ACF don't use
111	SN11220ACF don't use

Bit 7 is used to disable the internal digital volume control feature of SN11220ACF. The internal digital volume control is used to regulate the volume in SN11220ACF. If it is enabled, SN11220ACF will receive OS volume command to regulate audio data. If it is disabled, SN11220ACF will ignore OS volume command.

Byte 4 :

Byte 4 is reserved in SN11220ACF.

Byte 5 :

Byte 5 is reserved in SN11220ACF.

Byte 6 :

Byte 6 is reserved in SN11220ACF.



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Byte 7 :

Byte 7 is used to set data to the register 1 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

Byte 8 :

Byte 8 is used to set data to the register 2 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

Byte 9 :

Byte 9 is used to set data to the register 3 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

Byte A :

Byte A is used to set data to the register 4 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

Byte B :

Byte B is used to set data to the register 5 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

Byte C :

Byte C is used to set data to the register 6 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

Byte D :

Byte D is used to set data to the register 7 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

Byte E :

Byte E is used to set data to the register 8 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

Byte F :

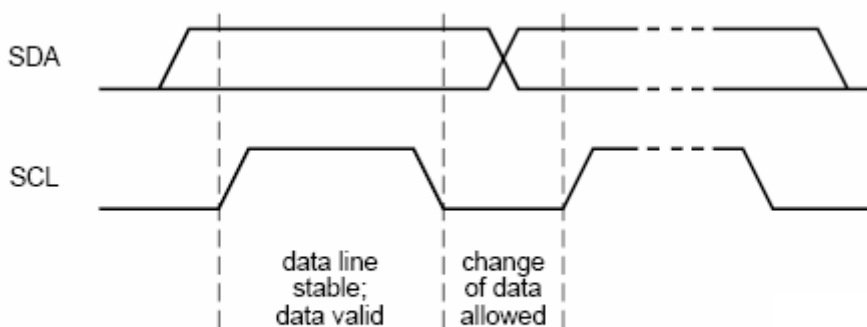
Byte F is used to set data to the register 9 of the two-wire serial port of SN11220ACF.
Please refer to section VIII.

VIII. Two-wire serial port definition

To provide extension capability, SN11220ACF contains a two-wire series bus circuitry as an interface to MCU. The two wire series bus serves as a slave device with bit rate up to 400Kbps (fast mode) . MCU can write ten bytes to the SN11220ACF with 8-bit register address 0x38. MCU can also read ten bytes from SN11220ACF with 8-bit register address 0x39.

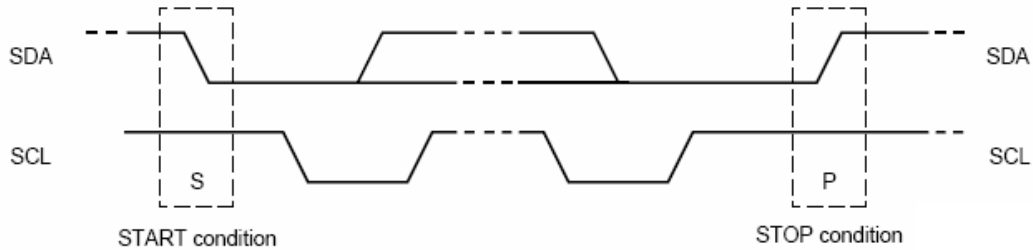
This section just provides simple description of the two-wire series bus. It is compatible with the I²C slave mode. User can get more detail explanation from the I²C specification.

The input pin “SCL” is used to get the two wire series bus clock from MCU, and the open-drain output pin “SDA” is used to send or receive serial signal to/from MCU. As shown below, “SDA” should be stable when “SCL” is high, and can have transition only when “SCL” is low.



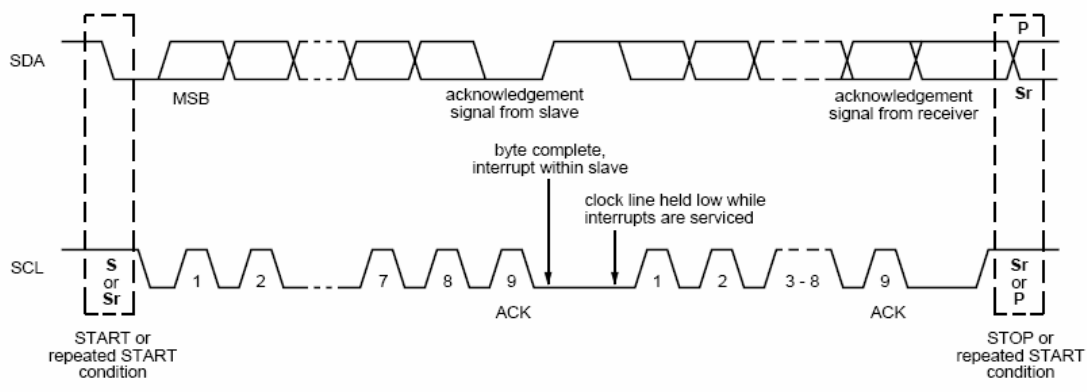
Bit transfer on the I²C-bus.

START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START) .

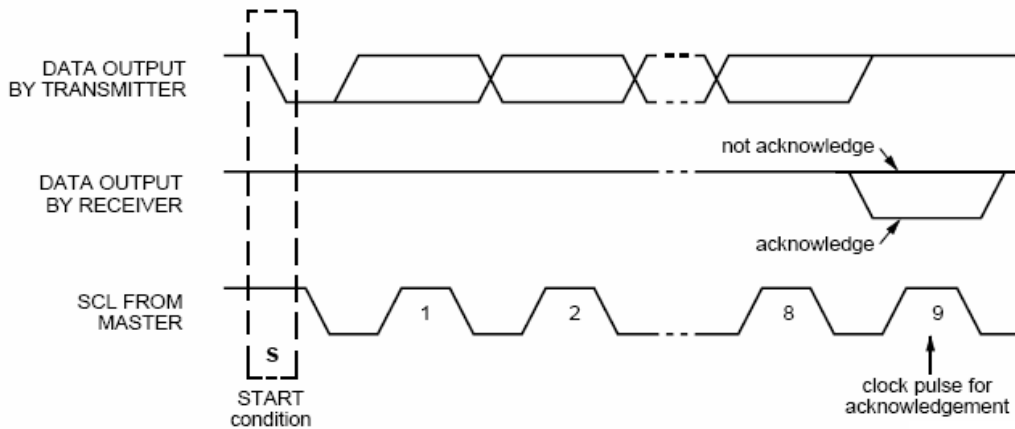


START and STOP conditions.

The figure below demonstrates a typical two-wire serial bus transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement; a STOP or repeated START should follow. The next figure shows more detailed about acknowledgement bit. Note that “SCL” is always driven by the master.



Data transfer on the I²C-bus.

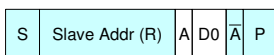


Acknowledge on the I²C-bus.

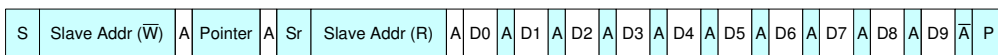
The figure below shows a complete data transfer. After a STRAT, MCU should send 7-bit slave address (7'b0011100) first, and then the 8th bit denotes a read transfer when it's 1 ; or a write transfer when it's 0.

Note that address 0x0b is the indicator to notice SN11220ACF to update the data written by MCU to PC via USB HID. Writing any thing to address 0x0b means the SN11220ACF can transfer all the data to PC. Before address 0x0b be written, SN11220ACF will transfer the last data which the last indicator launched.

Old READ :



New READ :

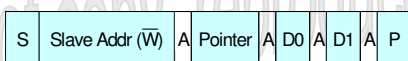


NOTE:

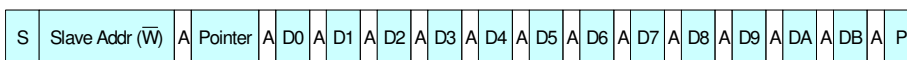
1. S : START
2. Sr : Repeated START
3. Slave Addr (\bar{W}) : Slave Address (Write) = 0x38
4. Slave Addr (R) : Slave Address (Read) = 0x39
5. Pointer : Register0 Pointer = 0x00
6. A : Acknowledge
7. \bar{A} : Not Acknowledge
8. D0 : Data Length (Byte0)
9. D1 ~ D8 : Data (Byte1 ~ Byte8)
10. D9 : Rolling Code (Byte9)
11. P : STOP
12. ☒ : From Master to Slave
13. ☐ : From Slave to Master

READ

Old WRITE :



New WRITE :



NOTE:

1. S : START
2. Slave Addr (\bar{W}) : Slave Address (Write) = 0x38
3. Pointer : Register0 Pointer = 0x00
4. D0 : Data Length (Byte0)
5. D1 ~ D8 : Data (Byte1 ~ Byte8)
6. D9 : Rolling Code (Byte9)
7. DA ~ DB : Dummy Byte (ByteA ~ ByteB)
8. A : Acknowledge
9. P : STOP
10. ☒ : From Master to Slave
11. ☐ : From Slave to Master

WRITE



IX. Operating rating and electrical characteristics

9.1 Absolute maximum rating

Symbol	Parameter	value	unit
Dvmin	min digital supply voltage	DGND – 0.3	V
Dvmax	max digital supply voltage	DGND + 3.6	V
Avmin	min analog supply voltage	AGND – 0.3	V
Avmax	max analog supply voltage	AGND + 3.6	V
Dvinout	voltage on any digital input or output pin	DGND –0.3 to 3.6	V
Avinout	voltage on any analog input or output pin	AGND –0.3 to Avdd + 0.3	V
T _{stg}	storage temperature range	-40 to +125	°C
ESD (HBM)	ESD human body mode	2000	V
ESD (MM)	ESD machine mode	200	V
I _{latch}	minimum latch up current	200	mA

9.2 Operation conditions

Symbol	Parameter	value	unit
DVdd	digital supply voltage	+3.3 (typ)	V
Avdd	analog supply voltage	+3.3 (typ)	V
T _A	operating ambient temperature range	25 (typ)	°C

9.3 DC electrical characteristics

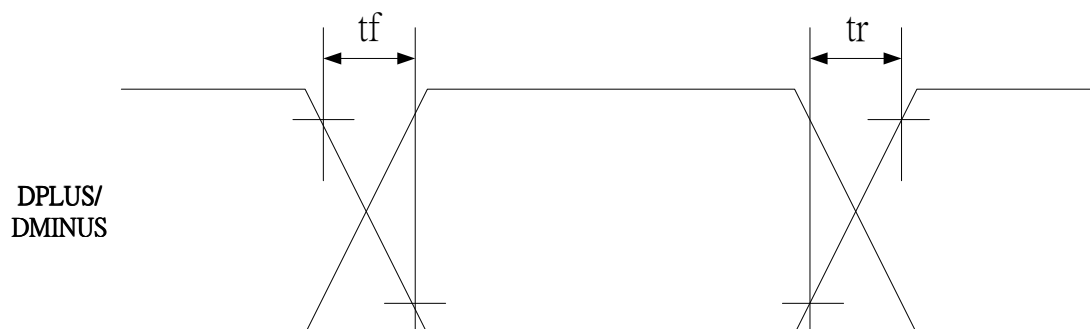
Symbol	parameter	test condition	Value	unit
V_{DI}	differential input sensitivity	$ (D+) - (D-) $	0.2 (min)	V
V_{CM}	differential common mode range	Included V_{DI} range	0.8 (min) 2.5 (max)	V
V_{SE}	single ended receiver threshold		0.8 (min) 2.0 (max)	V
V_{IH}	high level input voltage		2.0 (min)	V
V_{IL}	low level input voltage		0.8 (max)	V
I_{OH}	drive current	$V_{OH} = 2.3V$	4 (typ) for 4mA pads 8 (typ) for 8mA pads	mA
I_{OL}	sink current	$V_{OL} = 0.5V$	4 (typ) for 4mA pads 8 (typ) for 8mA pads	mA
I_{DD}	input supply current		30 (max)	mA
$I_{suspend}$	supply current in suspend		300 (max)	μA

9.4 AC electrical characteristics

9.4.1 Operation clocks

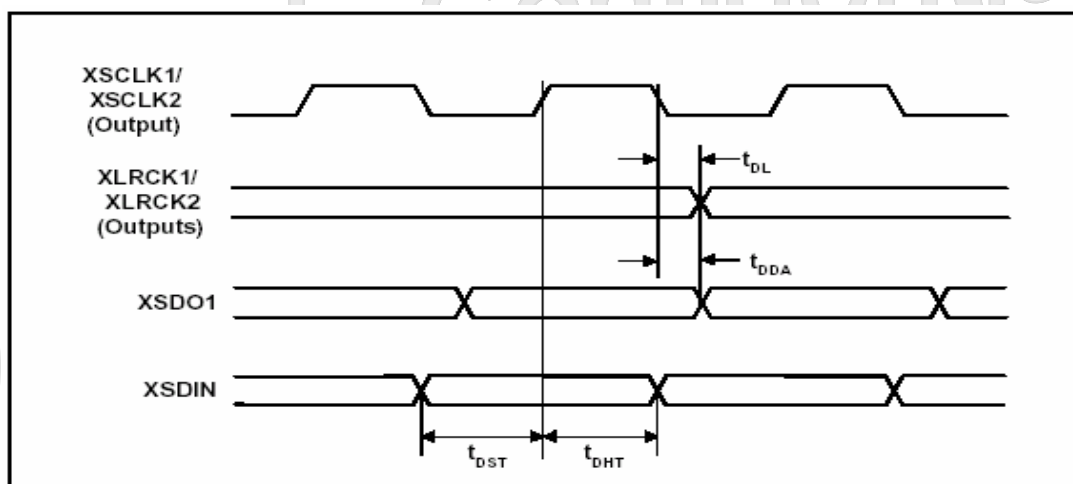
symbol	parameter	value	unit
CLKin	system clock input to PLL	6 (typ)	MHz
	CLKin duty cycle	50 ± 2	%

9.4.2 USB transceiver signal (full speed mode)



symbol	parameter	test condition	Min	max	unit
Tr	transition rise time for USBDP or USBDM		4	20	ns
Tf	transition fall time for USBDP or USBDM		4	20	ns
Trfm	rise / fall time matching	$(Tr / Tf) * 100$	90	110	%
Vo(crs)	signal crossover voltage		1.3	2.0	V

9.4.3 I²S CODEC interface timing



$F_s = 48\text{kHz}$, $XMCLK = 256\text{fs}$, $XSCLK = 64\text{fs}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
XLRCK1/XLRCK2 propagation delay from XSCLK1/XSCLK2 falling edge	t_{DL}		0		10	ns
XSDO1 propagation delay from XSCLK1 falling edge	t_{DDA}		0		10	ns
XSDIN setup time to XSCLK2 rising edge	t_{DST}		10			ns
XSDIN hold time from XSCLK2 rising edge	t_{DHT}		10			ns



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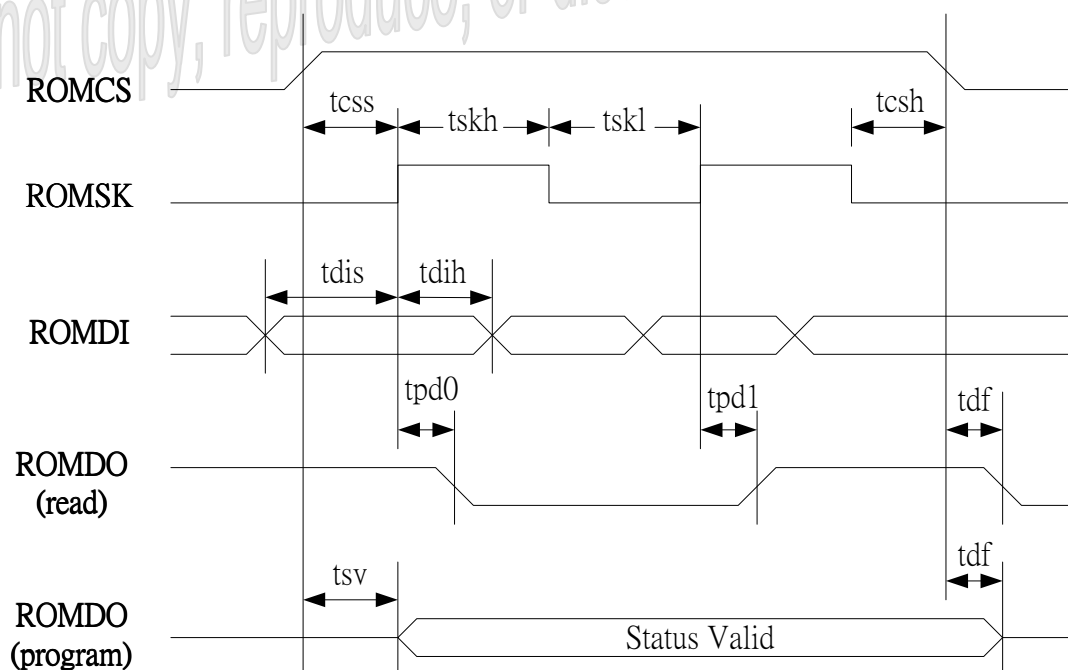
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9.4.4 Embedded Regulator

$T_A=25^{\circ}\text{C}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		4.5	5.0	5.5	V
V_{OUT}	Output Voltage		3.0	3.3	3.6	V
I_{MAX}	Maximum Load Current	VDD=5V	120			mA
I_Q	Ground Pin Current	VDD=5V		80	150	μA
V_{DROP}	Dropout Voltage	VDD=5V, 120mA Loading		30	80	mV
R_{PL}	Pull Low Resistance for ENLDO_	VDD=5V	40K	100K	250K	mV

9.4.5 EEPROM Interface





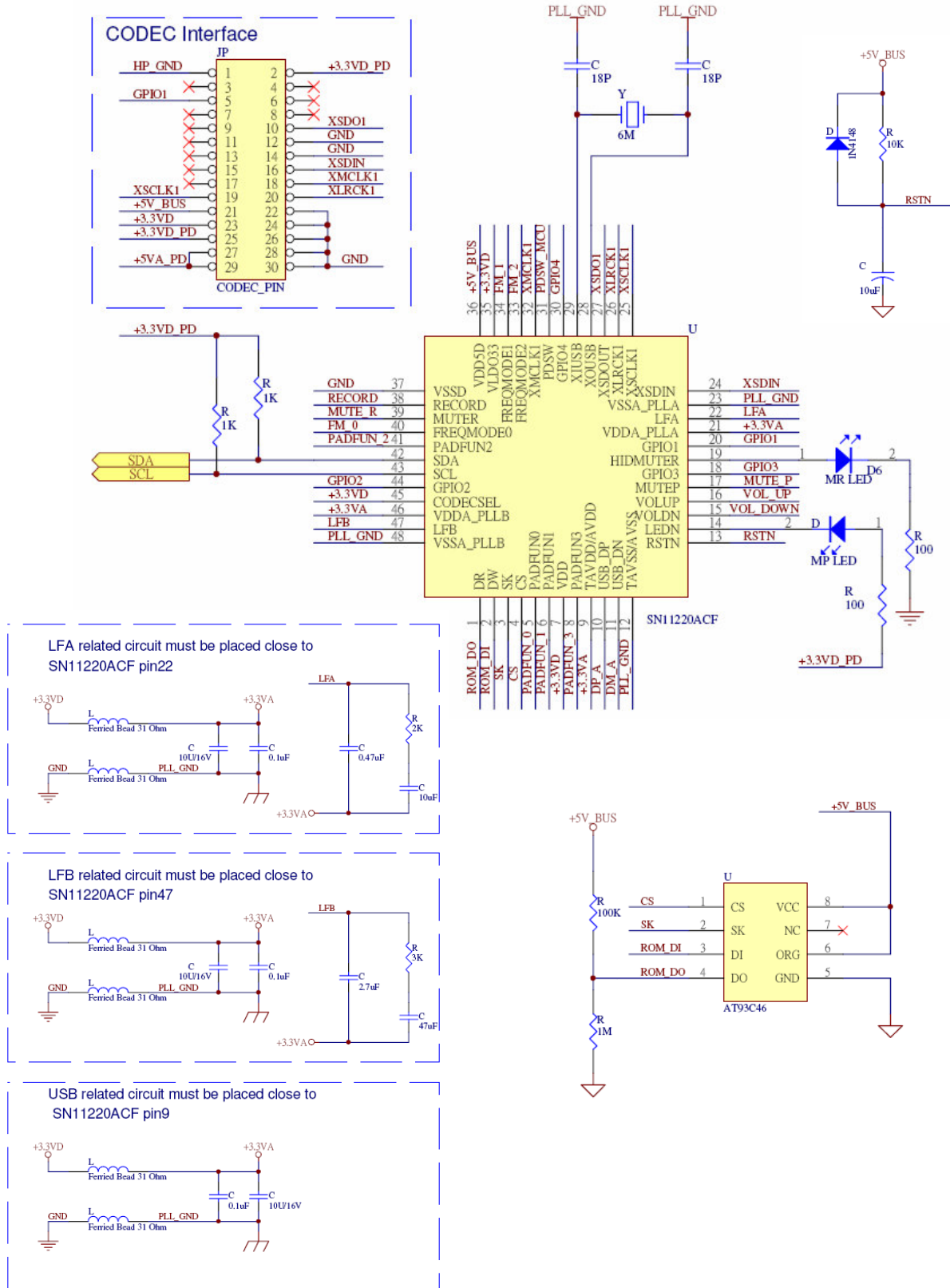
USB Audio Controller

Data Sheet SN11220ACF

symbol	parameter	min	typ	max	unit
tsk	ROMSK clock frequency	-	400	-	kHz
tskh	ROMSK high time		1200		ns
tskl	ROMSK low time		1200		ns
tcs	Minimum ROMCS low time		2400		ns
tcss	ROMCS setup time		2400		ns
tdis	ROMDI setup time		1200		ns
tcsh	ROMCS hold time		1200		ns
tdih	ROMDI hold time		1200		ns
tpd1	ROMDO delay to "1"			250	ns
tpd0	ROMDO delay to "0"			250	ns
tsv	ROMCS to status valid			250	ns
tdf	ROMCS to ROMDO high impedance			250	ns

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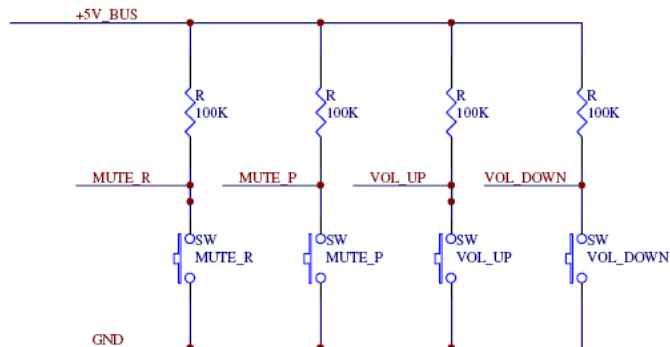
X. Reference design:



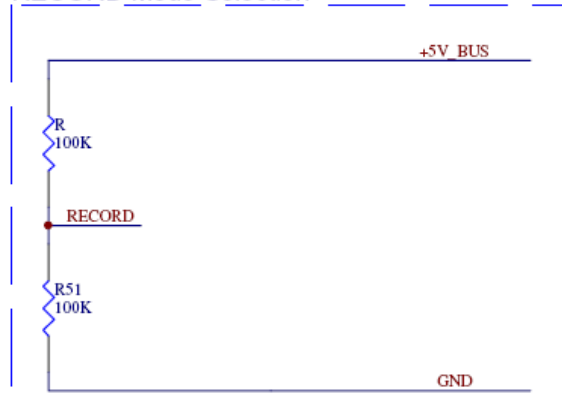


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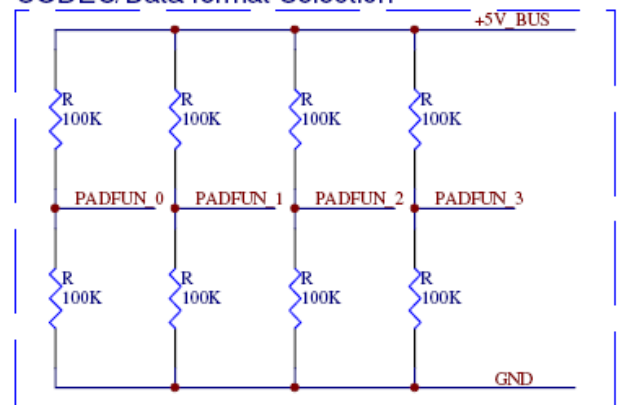
Data Sheet SN11220ACF



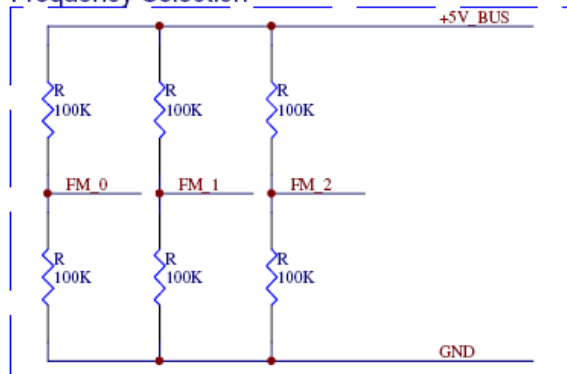
RECORD Mode Selection



CODEC/Data format Selection



Frequency Selection





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XI. Naming rule

(1)		(2)					(3)	(4)	(5)	(6)
S	N	1	1	2	2	0	A	C	F	

(1) SONiX chip

(2) USB audio controller 11220 series

(3) Hardware version

A: The first version, B: The second version, C: The third version, etc.

(4) Series code

Series Code	Name	Description
C	Dect	I ² S, PCM interface and for Dect solution. No 3-wire control pin. One frequency mode.
P	Public	I ² S, AC'97 and S/PDIF. Support different sampling rate to playback and recording.
R	RF	I ² S, AC'97 and S/PDIF. One frequency mode.

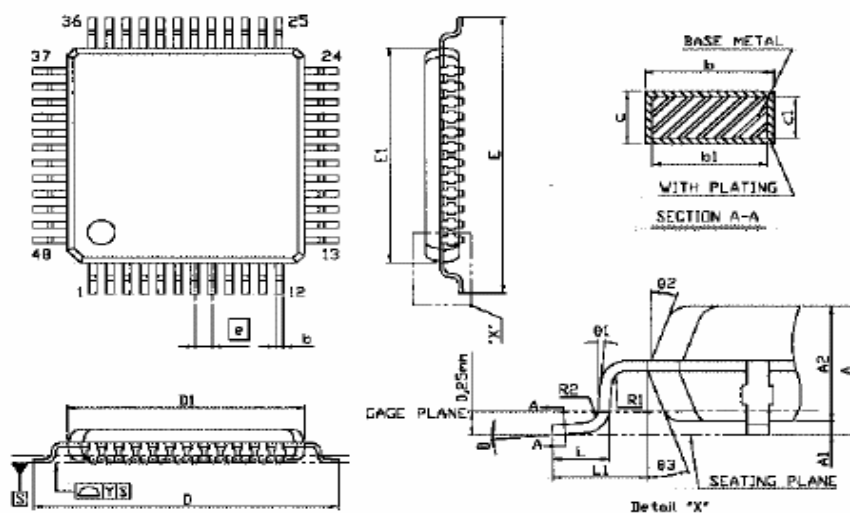
(5) Package type

Package type	Description
F	LQFP

(6) Green Package

Green Package	Description
G	It achieve the requirement of SS-00259 (level-3)
R	It achieve the requirement of SS-00259 (level-3)
	Non-green package

XII. Package dimension



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
Ø	0.50 BSC			20 BSC		
L	0.45	0.60	0.73	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:

1. REFER TO JEDEC MS-026/BBC
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION, INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4. ALL DIMENSIONS IN MILLIMETERS.



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XIII. Revision History

<i>Revision</i>	<i>Revision Date</i>	<i>Description of changes</i>
Preliminary	Dec 20, 2005	Preliminary
V1.0	July 20, 2006	Detail description Add section 10 Add section 11
V1.01	Aug 10, 2006	PCM master and slave clock

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